

The MPC94551 is a CMOS 1:4 fanout buffer. The MPC94551 is ideal for applications requiring lower voltage.

Features

- 1:4 CMOS fanout buffer
- 300 ps output to output skew
- I/O frequency up to 160 MHz operation
- Non-inverting output clock
- 3.3 V supply voltage
- Output Enable mode tri-states outputs
- -40°C to 85°C industrial temperature range
- 8-lead SOIC package, Pb-free

MPC94551

1:4 LVC MOS CLOCK BUFFER



EF SUFFIX
8-LEAD SOIC PACKAGE
Pb-FREE PACKAGE
CASE 751-06

ORDERING INFORMATION

| Device | Package |
|--------------|----------------|
| MPC94551EF | SO-8 (Pb-FREE) |
| MPC94551EFR2 | SO-8 (Pb-FREE) |

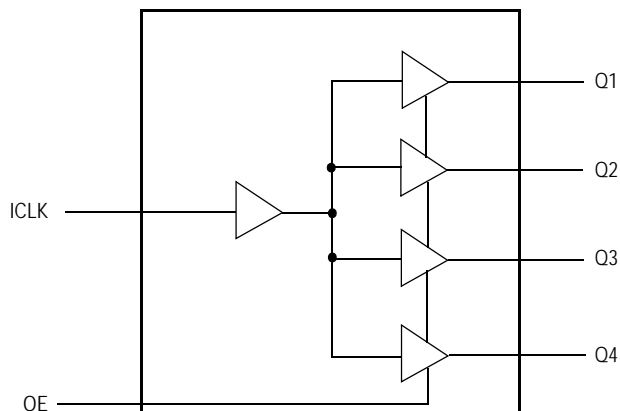


Figure 1. Logic Diagram

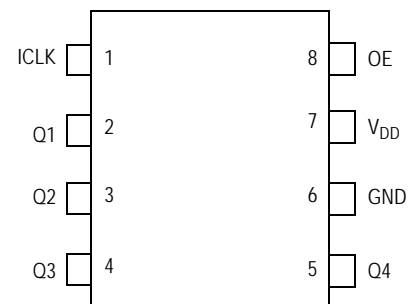


Figure 2. Pin Assignment

Table 1. Pin Description

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|-----------------|----------|---|
| 1 | ICLK | Input | Clock input, internal pull-up resistor |
| 2 | Q1 | Output | Clock output ⁽¹⁾ |
| 3 | Q2 | Output | Clock output ⁽¹⁾ |
| 4 | Q3 | Output | Clock output ⁽¹⁾ |
| 5 | Q4 | Output | Clock output ⁽¹⁾ |
| 6 | GND | Power | Connect to ground ⁽²⁾ |
| 7 | V _{DD} | Power | Connect to 3.3 V ⁽²⁾ |
| 8 | OE | Input | Output enable, tri-states outputs when low, internal pull-up resistor |

1. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

2. A decoupling capacitor of 0.01 μ F should be connected between V_{DD} on pin 7 and GND on pin 6, as close to the device as possible.

Table 2. Absolute Maximum Ratings⁽¹⁾

| Parameter | Rating | Unit |
|---------------------------------------|------------------------------|------|
| Power Supply Voltage, V _{DD} | 3.9 | V |
| All Inputs and Outputs | -0.5 to V _{DD} +0.5 | V |
| Ambient Operating Temperature | -40 to +85 | °C |
| Storage Temperature | -65 to +150 | °C |
| Junction Temperature | 175 | °C |
| Soldering Temperature | 260 | °C |

1. Stresses above the ratings listed below can cause permanent damage to the device. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 3. DC Characteristics (V_{DD} = 3.3 V \pm 5%; Ambient Temperature = -40°C to 85°C)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|-----------------|--------------------------|--------------------------|----------|--------------------------|------------|
| Operating Voltage | V _{DD} | | 3.15 | | 3.45 | V |
| Input High Voltage ⁽¹⁾ , ICLK | V _{IH} | | V _{DD} /2 + 0.7 | | 3.8 | V |
| Input Low Voltage ⁽¹⁾ , ICLK | V _{IL} | | | | V _{DD} /2 - 0.7 | V |
| Input High Voltage, OE | V _{IH} | | 2 | | V _{DD} | V |
| Input Low Voltage, OE | V _{IL} | | | | 0.8 | V |
| Output Low Voltage | V _{OL} | I _{OL} = 12 mA | | | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -12 mA | 2.4 | | | V |
| Operating Supply Current | I _{DD} | No load, 135 MHz | | 30 | | mA |
| Nominal Output Impedance | Z _O | | | 27 | | Ω |
| Internal Pull-up Resistor | R _{PU} | ICLK | | 31 | | k Ω |
| Input Capacitance | C _{IN} | OE pin | | 5 | | pF |
| | C _{IN} | ICLK | | 1 | | pF |
| Short Circuit Current | I _{OS} | | | \pm 50 | | mA |

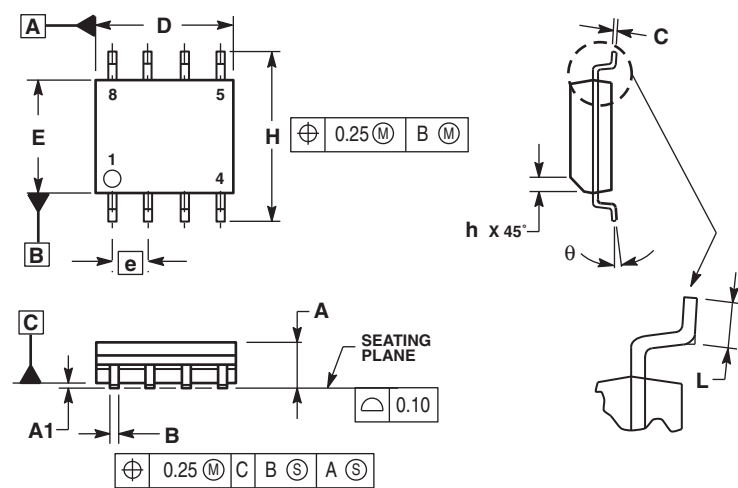
1. Nominal switching threshold is V_{DD}/2.

Table 4. AC Characteristics ($V_{DD} = 3.3\text{ V} \pm 5\%$; Ambient Temperature = -40°C to 85°C)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--------------------------------------|----------|----------------------------|-----|-----|-----|------|
| Input Frequency | | | 0 | | 160 | MHz |
| Output Frequency ⁽¹⁾ | | 15 pF load | | | 160 | MHz |
| Output Clock Rise Time | t_{OR} | 0.8 V to 2.0 V | | | 1.5 | ns |
| Output Clock Fall Time | t_{OF} | 2.0 V to 0.8 V | | | 1.5 | ns |
| Propagation Delay ⁽²⁾ | | 135 MHz | 1.5 | 4 | 5 | ns |
| Output to Output Skew ⁽³⁾ | | Rising edges at $V_{DD}/2$ | | | 300 | ps |

1. Measured with an external series resistor of 33Ω positioned close to each output pin
2. Measured with rail to rail input clock
3. Measured between any 2 outputs with equal loading

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.25 |
| θ | 0° | 7° |

D/EF SUFFIX
SOIC PACKAGE
CASE 751-06
ISSUE T

Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|-------|------|--------------------------------------|----------|
| 4 | | 1 | NRND – Not Recommend for New Designs | 12/21/12 |
| 4 | | 1 | Removed NRND | 5/5/15 |

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