Product Discontinuance Notice – Last Time Buy Expires on (12/7/2013) **DATA SHEET**

The MC100ES6030 is a triple master-slave D flip-flop with differential outputs. When the clock input is low, data enters the master latch and transfers to the slave during a positive transition on the clock input.

Each flip-flop has individual Reset inputs while the Set input is shared. The Set and Reset inputs are asynchronous and override the clock inputs.

Features

- 1.2 GHz minimum toggle frequency
- LVPECL operating range: V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V
- LVECL operating range: V_{CC} = 0 V, V_{EE} = –3.135 V to –3.8 V
- 20-lead SOIC package
- Ambient temperature range –40°C to +85°C

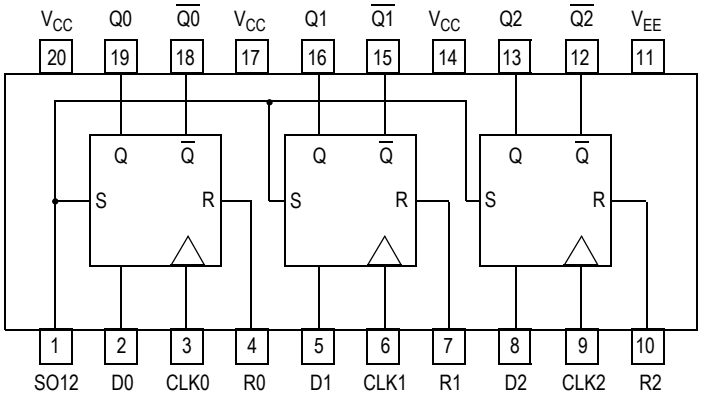


Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

MC100ES6030

DW SUFFIX
20-LEAD SOIC PACKAGE
CASE 751D-07

ORDERING INFORMATION

Device	Package
MC100ES6030DW	SO-20
MC100ES6030DWR2	SO-20
MC100ES6030EG	SO-20, PB-Free

PIN DESCRIPTION

Pin	Function
D0–D2	ECL Data Inputs
R0–R2	ECL Reset Inputs
CLK0–CLK2	ECL Clock Inputs
SO12	ECL Common Set Input
$\overline{Q0}$–Q2, Q0–$\overline{Q2}$	ECL Differential Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

R	S	D	CLK	Q	$\overline{Q}$
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	4000 V 400 V 200 mA
θ_{JA} Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 SOIC 500 LFPM, 20 SOIC	90°C/W 60°C/W
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

Table 2. Absolute Maximum Ratings(1)

Symbol	Rating	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{stg}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 V to –3.135 V; V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)

		-40°C			0°C to 85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		32	57		32	57	mA
V_{OH}	Output HIGH Voltage(1)	V_{CC}–1150		V_{CC}–760	V_{CC}–1150		V_{CC}–760	mV
V_{OL}	Output LOW Voltage(1)	V_{CC}–1950		V_{CC}–1500	V_{CC}–1950		V_{CC}–1500	mV
V_{IH}	Input HIGH Voltage	V_{CC}–1165		V_{CC}–880	V_{CC}–1165		V_{CC}–880	mV
V_{IL}	Input LOW Voltage	V_{CC}–1810		V_{CC}–1475	V_{CC}–1810		V_{CC}–1475	mV
I_{IN}	Input Current			±150			±150	µV

1. Outputs are terminated through a 50Ω resistor to V_{CC} – 2 volts. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported, but the power consumption of the device will increase.

Table 4. AC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 V to –3.135 V; V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	1.2			1.2			1.2			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK S, R	350 550		600 800	350 550		600 800	350 550		600 800	ps ps
t_s t_h	Setup Time Hold Time	250 400	50 100		250 400	50 100		250 400	50 100		ps ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK S, R	300 500			300 500			300 500			ps ps
t_{JITTER}	Cycle-to-Cycle Jitter (RMS 1σ)			1			1			1	ps
t_r / t_f	Output Rise/Fall Time (20%–80%)	60		250	60		250	60		250	ps

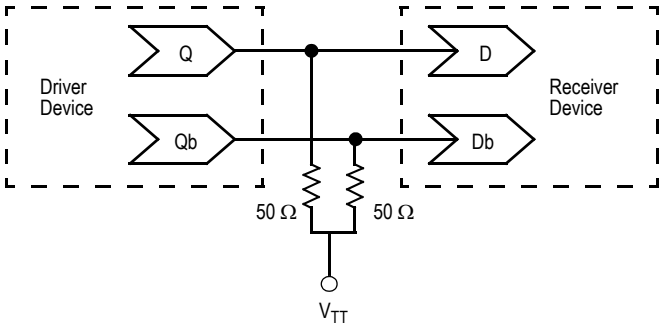
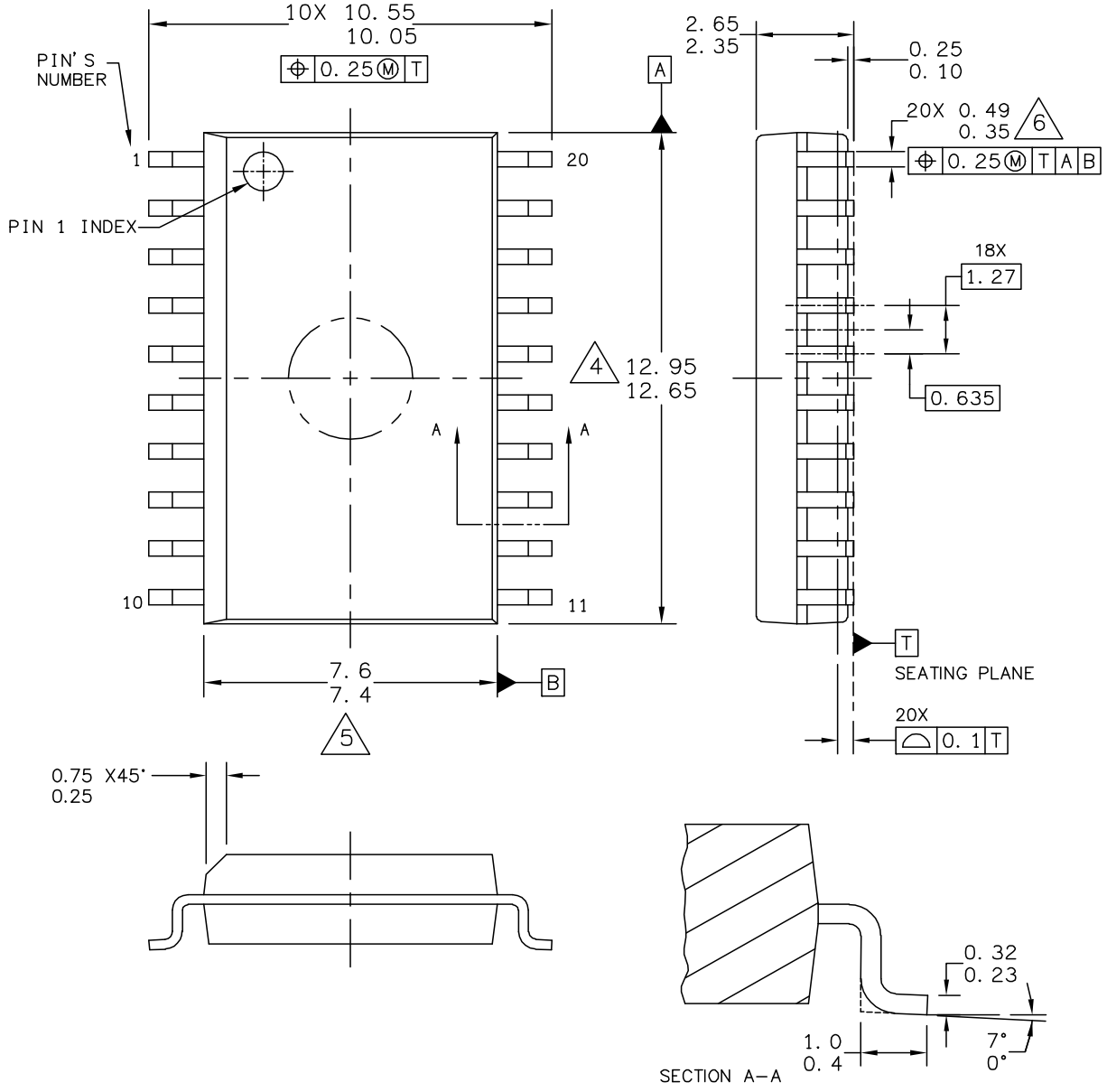


Figure 2. Typical Termination for Output Driver and Device Evaluation

PACKAGE DIMENSIONS



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TITLE: 20LD SOIC W/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42343B	REV: J
	CASE NUMBER: 751D-07	23 MAR 2005
	STANDARD: JEDEC MS-013AC	

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CASE 751D-07
ISSUE J
20-LEAD SOIC PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 mm.

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20-LEAD SOIC PACKAGE

Revision History Sheet

Rev	Table	Page	Description of Change	Date
2		1	Product Discontinuance Notice – Last Time Buy Expires on (12/7/2013)	2/5/13

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