DUAL CHANNEL DDRII/III ZERO DELAY BUFFER

9P960

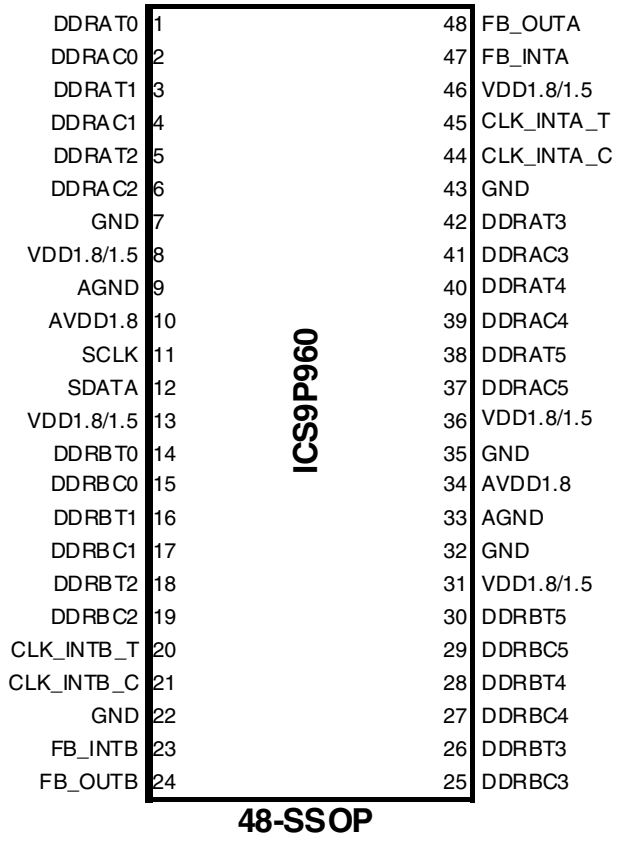
Recommended Application

Dual DDR zero delay buffer

Features/Benefits

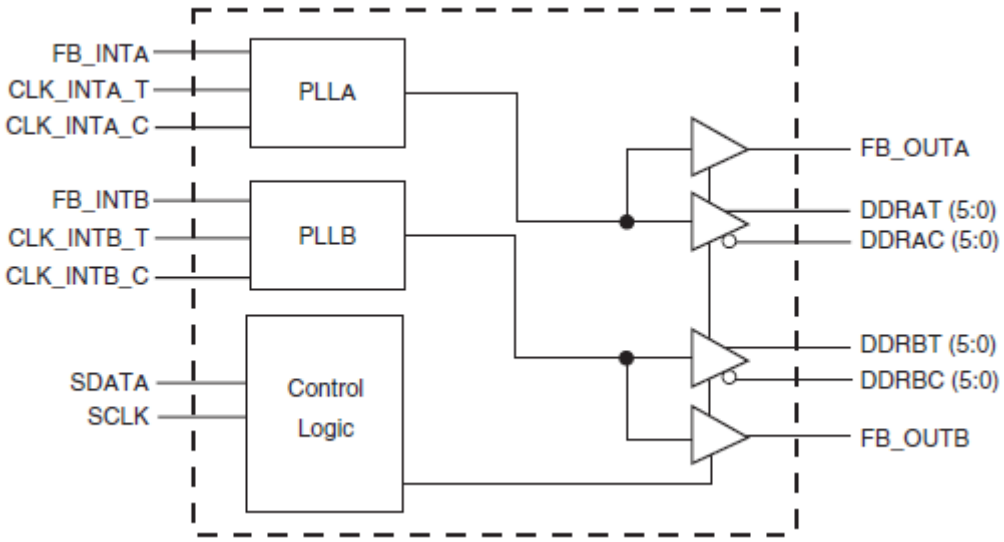
- High performance, low jitter zero delay buffer
- I^2C for functional and output control
- Dual bank 1-6 differential clock distribution
- 2 separate feedback in & out for input to output synchronization for each bank
- Supports up to 4 DDR DIMMs
- Supports up to DDRII - 1066MHz
- Supports up to DDRIII (1.8V core) - 1333MHz
- Output-to-output skew: <100ps

Pin Configuration



48-SSOP

Block Diagram



Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	DDRAT0	OUT	"True" Clock of differential pair output.
2	DDRAC0	OUT	"Complementary" Clock of differential pair output.
3	DDRAT1	OUT	"True" Clock of differential pair output.
4	DDRAC1	OUT	"Complementary" Clock of differential pair output.
5	DDRAT2	OUT	"True" Clock of differential pair output.
6	DDRAC2	OUT	"Complementary" Clock of differential pair output.
7	GND	PWR	Ground pin.
8	VDD1.8/1.5	PWR	Power supply, nominal 1.8V or 1.5V
9	AGND	PWR	Analog Ground pin for Core PLL
10	AVDD1.8	PWR	1.8V Analog Power pin for Core PLL
11	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
12	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
13	VDD1.8/1.5	PWR	Power supply, nominal 1.8V or 1.5V
14	DDRBT0	OUT	"True" Clock of differential pair output.
15	DDRBC0	OUT	"Complementary" Clock of differential pair output.
16	DDRBT1	OUT	"True" Clock of differential pair output.
17	DDRBC1	OUT	"Complementary" Clock of differential pair output.
18	DDRBT2	OUT	"True" Clock of differential pair output.
19	DDRBC2	OUT	"Complementary" Clock of differential pair output.
20	CLK_INTB_T	IN	True' reference clock input for bank B.
21	CLK_INTB_C	IN	Complementary' reference clock input for bank B.
22	GND	PWR	Ground pin.
23	FB_INTB	IN	True single-ended feedback input, provides feedback signal to internal PLL for synchronization with CLK_INTB to eliminate phase error on bank B.
24	FB_OUTB	OUT	Feedback output, dedicated external feedback for bank B outputs.
25	DDRBC3	OUT	"Complementary" Clock of differential pair output.
26	DDRBT3	OUT	"True" Clock of differential pair output.
27	DDRBC4	OUT	"Complementary" Clock of differential pair output.
28	DDRBT4	OUT	"True" Clock of differential pair output.
29	DDRBC5	OUT	"Complementary" Clock of differential pair output.
30	DDRBT5	OUT	"True" Clock of differential pair output.
31	VDD1.8/1.5	PWR	Power supply, nominal 1.8V or 1.5V
32	GND	PWR	Ground pin.
33	AGND	PWR	Analog Ground pin for Core PLL
34	AVDD1.8	PWR	1.8V Analog Power pin for Core PLL
35	GND	PWR	Ground pin.
36	VDD1.8/1.5	PWR	Power supply, nominal 1.8V or 1.5V
37	DDRAC5	OUT	"Complementary" Clock of differential pair output.
38	DDRAT5	OUT	"True" Clock of differential pair output.
39	DDRAC4	OUT	"Complementary" Clock of differential pair output.
40	DDRAT4	OUT	"True" Clock of differential pair output.
41	DDRAC3	OUT	"Complementary" Clock of differential pair output.
42	DDRAT3	OUT	"True" Clock of differential pair output.
43	GND	PWR	Ground pin.
44	CLK_INTA_C	IN	Complementary' reference clock input for bank A.
45	CLK_INTA_T	IN	True' reference clock input for bank A.
46	VDD1.8/1.5	PWR	Power supply, nominal 1.8V or 1.5V
47	FB_INTA	IN	True single-ended feedback input, provides feedback signal to internal PLL for synchronization with CLK_INTA to elimate phase error on bank A.
48	FB_OUTA	OUT	Feedback output, dedicated external feedback for bank A outputs.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9P960. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1.8/1.5V Core Voltage	AVDD1.8	With respect to GND	-0.5		2.3	V
1.8/1.5V Logic Voltage	VDD1.8/1.5	With respect to GND	-0.5		2.3	V
Storage Temperature	Ts	-	-65		150	°C
Ambient Operating Temp	Tambient	-	0		70	°C
	Tcase	-			95	°C
Input ESD protection HBM	ESD prot	-	2000			V

1. Guaranteed by design and characterization, not 100% tested in production.
2. Operation under these conditions is neither implied nor guaranteed.

DDRII Specifications

Recommended Operating Conditions

T_A = 0 - 70°C; Supply Voltage AVDD1.8, VDD1.8/1.5 = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD1.8/1.5}$		1.7	1.8	1.9	V
	$A_{VDD1.8}$		1.7	1.8	1.9	V
Low level input voltage	V_{IL}	CLK_INT, CLK_INC, FB_IN			$0.35V_{DD}$	V
High level input voltage	V_{IH}	CLK_INT, CLK_INC, FB_IN	$0.65V_{DD}$			V
Operating free-air temperature	T_A		0		70	°C

Notes:
1. Unused inputs must be held high or low to prevent them from floating.

Electrical Characteristics–Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage AVDD1.8, VDD1.8/1.5 = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND			10	µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			-10	µA
Output Disabled Low Current	I_{ODL}	OE = L, V_{ODL} = 100mV	100			µA
Operating Supply Current	I_{DDA}	AVDD1.8 @ 400MHz		34	45	mA
	$I_{DD1.8}$	VDD1.8/1.5 @ 400MHz		436	500	mA
	I_{DDLD}	C_L = 0pf			500	µA
Input Clamp Voltage	V_{IK}	V_{DDQ} = 1.8V Iin = -18mA			-1.2	V
High-level output voltage	V_{OH}	I_{OH} = -100µA	V_{DD}-0.2			V
		I_{OH} = -9mA	1.1			V
Low-level output voltage	V_{OL}	I_{OL}=100µA			0.1	V
		I_{OL}=9mA			0.6	V
Input Capacitance	C_{IN}	V_I = GND or V_{DD}	2	3	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = GND or V_{DD}	2	3	5	pF

Timing

T_A = 0 - 70°C; Supply Voltage AVDD1.8, VDD1.8/1.5 = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Max clock frequency	$freq_{op}$	1.8V±0.1V @ 25°C	150		600	MHz
Application Frequency Range	$freq_{App}$	1.8V+0.1V @ 25°C	160		533	MHz
Input clock duty cycle	d_{tin}		40		60	%
CLK stabilization	T_{STAB}				15	µs

Switching Characteristics[1]

T_A = 0 - 70°C; Supply Voltage AVDD1.8, VDD1.8/1.5 = 1.8 V +/- 0.1V (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output enable time	t_{en}	OE to any output			8	ns
Output disable time	t_{dis}	OE to any output			8	ns
Period jitter	$t_{jit(per)}$		-30		30	ps
Half-period jitter	$t_{jit(hper)}$		-40		40	ps
Input slew rate	$SLr1(i)$	Input Clock	1	2.5	4	v/ns
		Output Enable (OE), (OS)	0.5			v/ns
Output clock slew rate	$SLr1(o)$		1.5	2.5	3	v/ns
Cycle-to-cycle jitter	$t_{jit(cc+)}$				40	ps
	$t_{jit(cc-)}$				-40	ps
Dynamic Phase Offset	$t_{(\ )dyn}$		-20		20	ps
Static Phase Offset	$t_{(spo)}$		-60	0	60	ps
Output to Output Skew	t_{skew}				100	ps
SSC modulation frequency	f_{SSCMOD}	PLL will track SSC and meet dynamic phase offset in the specified range.	30.00		33	kHz
SSC clock input frequency deviation	$f_{SSC\%}$		0.00		-0.50	%

Notes:
1. Switching characteristics guaranteed for application frequency range.

DDRIII Specifications

Recommended Operating Conditions

T_A = 0 - 70°C; Supply Voltage AVDD = 1.8V+/- 0.1V, VDD = 1.5 V +/- 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD1.8/1.5}$		1.425	1.5	1.575	V
	$A_{VDD1.8}$		1.7	1.8	1.9	V
Low level input voltage	V_{IL}	CLK_INT, CLK_INC, FB_IN			$0.35V_{DD}$	V
High level input voltage	V_{IH}	CLK_INT, CLK_INC, FB_IN	$0.65V_{DD}$			V
Operating free-air temperature	T_A		0		70	°C

Notes:
1. Unused inputs must be held high or low to prevent them from floating.

Electrical Characteristics–Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage AVDD = 1.8V+/- 0.1V, VDD = 1.5 V +/- 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Current	I_{IH}	$V_I = V_{DD}$ or GND			10	µA
Input Low Current	I_{IL}	$V_I = V_{DD}$ or GND			-10	µA
Output Disabled Low Current	I_{ODL}	OE = L, V_{ODL} = 100mV	100			µA
Operating Supply Current	I_{DDA}	AVDD1.8 @ 400MHz		34	45	mA
	$I_{DD1.5}$	VDD1.8/1.5 @ 400MHz		331	375	mA
	I_{DDLD}	C_L = 0pf			500	µA
Input Clamp Current	V_{IK}	$V_I < 0$ or $V_I > V_{DD}$			-50	mA
Differential output clock swing	V_{OD}	I_{OH} = -11mA	500		VDD1.8/1.5	mV
Input Capacitance[1]	C_{IN}	V_I = GND or V_{DD}	2		5	pF
Output Capacitance[1]	C_{OUT}	V_{OUT} = GND or V_{DD}	2		5	pF

Timing

T_A = 0 - 70°C; Supply Voltage AVDD = 1.8V+/- 0.1V, VDD = 1.5 V +/- 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Max clock frequency	$freq_{op}$	1.5V±5% @ 25°C	300		700	MHz
Application Frequency Range	$freq_{App}$	1.5V+5% @ 25°C	300		670	MHz
Input clock duty cycle	d_{tin}		40		60	%
CLK stabilization	T_{STAB}				15	µs

Switching Characteristics[1]

T_A = 0 - 70°C; Supply Voltage AVDD = 1.8V+/- 0.1V, VDD = 1.5 V +/- 5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output enable time	t_{en}	OE to any output			8	ns
Output disable time	t_{dis}	OE to any output			8	ns
Period jitter	$t_{jit(per)}$		-30		30	ps
Half-period jitter	$t_{jit(hper)}$		-40		40	ps
Input slew rate	$SLr1(i)$	Input Clock	1	2.5	4	v/ns
		Output Enable (OE), (OS)	0.5			v/ns
Output clock slew rate	$SLr1(o)$		2	2.3	5.5	v/ns
Cycle-to-cycle jitter	$t_{jit(cc+)}$		0		40	ps
	$t_{jit(cc-)}$		0		-40	ps
Dynamic Phase Offset	$t_{(\ )dyn}$		-20		20	ps
Static Phase Offset	$t_{(spo)}$		-60	0	60	ps
Output to Output Skew	t_{skew}				100	ps
SSC modulation frequency	f_{SSCMOD}	PLL will track SSC and meet dynamic phase offset in the specified range.	30.00		33	kHz
SSC clock input frequency deviation	$f_{SSC\%}$		0.00		-0.50	%

Notes:
1. Switching characteristics guaranteed for application frequency range.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Read Address	Write Address
$D5_{(H)}$	$D4_{(H)}$

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

I2C Table: Output Control Register

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Freq Detect A	Low Frequency Detect PLLA OFF Control	RW	OFF	ON	1
Bit 6	FB_IN/OUTA	FB_OUTA Control	RW	Disable	Enable	1
Bit 5	DDRA_T5/C5	Output Control	RW	Disable	Enable	1
Bit 4	DDRA_T4/C4	Output Control	RW	Disable	Enable	1
Bit 3	DDRA_T3/C3	Output Control	RW	Disable	Enable	1
Bit 2	DDRA_T2/C2	Output Control	RW	Disable	Enable	1
Bit 1	DDRA_T1/C1	Output Control	RW	Disable	Enable	1
Bit 0	DDRA_T0/C0	Output Control	RW	Disable	Enable	1

I2C Table: Output Control Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Freq Detect B	Low Frequency Detect PLLB OFF Control	RW	OFF	ON	1
Bit 6	FB_IN/OUTB	FB_OUTB Control	RW	Disable	Enable	1
Bit 5	DDRB_T5/C5	Output Control	RW	Disable	Enable	1
Bit 4	DDRB_T4/C4	Output Control	RW	Disable	Enable	1
Bit 3	DDRB_T3/C3	Output Control	RW	Disable	Enable	1
Bit 2	DDRB_T2/C2	Output Control	RW	Disable	Enable	1
Bit 1	DDRB_T1/C1	Output Control	RW	Disable	Enable	1
Bit 0	DDRB_T0/C0	Output Control	RW	Disable	Enable	1

I2C Table: Group Skew Control Register

Byte 8	Name	Control Function	Type	0	1	Default
Bit 7	CLKINA Skw3	CLKINA Skew Control	RW	See Table 1: 7-Step Skew Programming Table		0
Bit 6	CLKINA Skw2		RW			0
Bit 5	CLKINA Skw1		RW			0
Bit 4	CLKINA Skw0		RW			0
Bit 3	FB_INTA Skw3	FB_INTA Skew Control	RW	See Table 1: 7-Step Skew Programming Table		0
Bit 2	FB_INTA Skw2		RW			0
Bit 1	FB_INTA Skw1		RW			0
Bit 0	FB_INTA Skw0		RW			0

I2C Table: Group Skew Control Register

Byte 9	Name	Control Function	Type	0	1	Default
Bit 7	CLKINB Skw3	CLKINB Skew Control	RW	See Table 1: 7-Step Skew Programming Table		0
Bit 6	CLKINB Skw2		RW			0
Bit 5	CLKINB Skw1		RW			0
Bit 4	CLKINB Skw0		RW			0
Bit 3	FB_INTB Skw3	FB_INTB Skew Control	RW	See Table 1: 7-Step Skew Programming Table		0
Bit 2	FB_INTB Skw2		RW			0
Bit 1	FB_INTB Skw1		RW			0
Bit 0	FB_INTB Skw0		RW			0

I2C Table: Revision ID and Vendor ID Register

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	Revision_ID bit 3	Rev ID	RW	-	-	0
Bit 6	Revision_ID bit 2		RW	-	-	0
Bit 5	Revision_ID bit 1		RW	-	-	0
Bit 4	Revision_ID bit 0		RW	-	-	0
Bit 3	Vendor_ID bit3	Vendor ID	RW	-	-	0
Bit 2	Vendor_ID bit2		RW	-	-	0
Bit 1	Vendor_ID bit1		RW	-	-	0
Bit 0	Vendor_ID bit0		RW	-	-	1

I2C Table: Byte Count Register

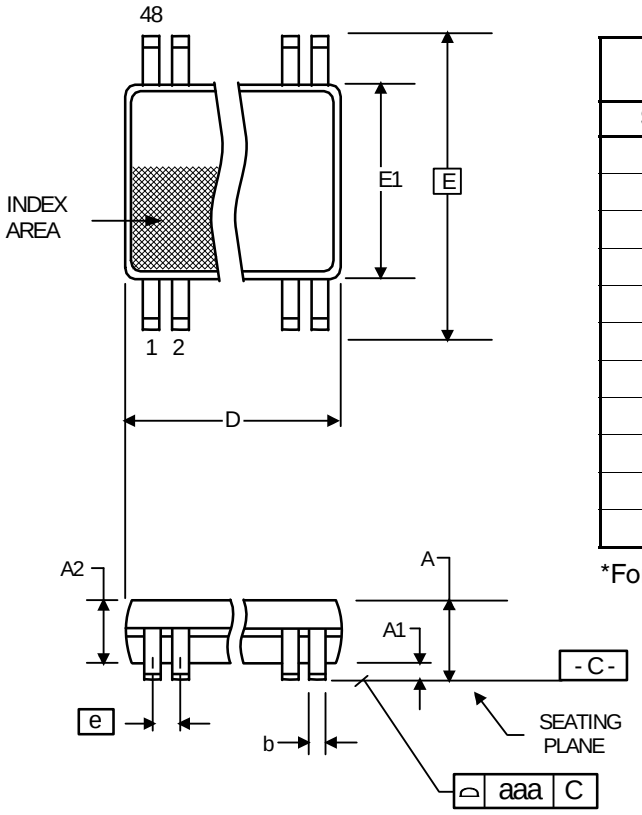
Byte 15	Name	Control Function	Type	0	1	Default
Bit 7	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 0F = 15 bytes		0
Bit 6	BC6		RW			0
Bit 5	BC5		RW			0
Bit 4	BC4		RW			0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			1
Bit 1	BC1		RW			1
Bit 0	BC0		RW			1

Table 1: 7-Steps Skew Programming Table

7 Step	11	10	01	00	LSB
11	900 ps	750 ps	600 ps	450 ps	
10	N/A	N/A	N/A	300 ps	
01	N/A	N/A	N/A	150 ps	
00	N/A	N/A	N/A	0.0 ps	
MSB					

Package Outline and Package Dimensions (48-pin SSOP, 300 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	15.75	16.00	.620	.630
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
α	0°	8°	0°	8°

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9P960AFLF	Tubes	48-pin SSOP	0 to +70° C
9P960AFLFT	Tape and Reel	48-pin SSOP	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issue Date	Description	Page #
0.1	5/17/2007	Initial Release	-
0.2	7/1/2007	Updated Product description and Pinout	Various
0.3	9/9/2008	Updated Max Frequency for DDR2 (1.8V) setting	8
0.4	10/19/2009	Updated pin description table	2
A	5/18/2011	1. Removed advance information water marks from electrical tables. 2. Udpated ordering information 3. Updated electrical tables 4. Updated SMBus tables 5. Updated to current datasheet template	Various

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