

Four Output Differential Buffer for PCI Express

Recommended Application:

DB800 Version 2.0 Yellow Cover part with PCI Express support with extended bypass mode frequency range.

Output Features:

- 4 - 0.7V current-mode differential output pairs
- Supports zero delay buffer mode and fanout mode
- Bandwidth programming available

Key Specifications:

- Outputs cycle-cycle jitter: < 50ps
- Outputs skew: < 50ps
- Extended frequency range in bypass mode:
Revision B: up to 333.33MHz
Revision C: up to 400MHz

Features/Benefits:

- Spread spectrum modulation tolerant, 0 to -0.5% down spread and +/- 0.25% center spread
- Supports undriven differential outputs in PD# and SRC_STOP# modes for power management.

Pin Configurations

VDD	1	ICS9DB401 (same as ICS9DB104)	28	VDDA
SRC_IN	2		27	GNDA
SRC_IN#	3		26	IREF
GND	4		25	OE_INV
VDD	5		24	VDD
DIF_1	6		23	DIF_6
DIF_1#	7		22	DIF_6#
OE_1	8		21	OE_6
DIF_2	9		20	DIF_5
DIF_2#	10		19	DIF_5#
VDD	11		18	VDD
BYPASS#/PLL	12		17	HIGH_BW#
SCLK	13		16	SRC_STOP#
SDATA	14		15	PD#
OE_INV = 0				

VDD	1	ICS9DB401	28	VDDA
SRC_IN	2		27	GNDA
SRC_IN#	3		26	IREF
GND	4		25	OE_INV
VDD	5		24	VDD
DIF_1	6		23	DIF_6
DIF_1#	7		22	DIF_6#
OE1#	8		21	OE6#
DIF_2	9		20	DIF_5
DIF_2#	10		19	DIF_5#
VDD	11		18	VDD
BYPASS#/PLL	12		17	HIGH_BW#
SCLK	13		16	SRC_STOP
SDATA	14		15	PD
OE_INV = 1				

28-pin SSOP & TSSOP



Pin Description When OE_INV = 0

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDD	PWR	Power supply, nominal 3.3V
2	SRC_IN	IN	0.7 V Differential SRC TRUE input
3	SRC_IN#	IN	0.7 V Differential SRC COMPLEMENTARY input
4	GND	PWR	Ground pin.
5	VDD	PWR	Power supply, nominal 3.3V
6	DIF_1	OUT	0.7V differential true clock output
7	DIF_1#	OUT	0.7V differential complement clock output
8	OE_1	IN	Active high input for enabling output 1. 0 = tri-state outputs, 1= enable outputs
9	DIF_2	OUT	0.7V differential true clock output
10	DIF_2#	OUT	0.7V differential complement clock output
11	VDD	PWR	Power supply, nominal 3.3V
12	BYPASS#/PLL	IN	Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode
13	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
14	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
15	PD#	IN	Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped.
16	SRC_STOP#	IN	Active low input to stop SRC outputs.
17	HIGH_BW#	IN	3.3V input for selecting PLL Band Width 0 = High, 1= Low
18	VDD	PWR	Power supply, nominal 3.3V
19	DIF_5#	OUT	0.7V differential complement clock output
20	DIF_5	OUT	0.7V differential true clock output
21	OE_6	IN	Active high input for enabling output 6. 0 = tri-state outputs, 1= enable outputs
22	DIF_6#	OUT	0.7V differential complement clock output
23	DIF_6	OUT	0.7V differential true clock output
24	VDD	PWR	Power supply, nominal 3.3V
25	OE_INV	IN	This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#)
26	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
27	GNDA	PWR	Ground pin for the PLL core.
28	VDDA	PWR	3.3V power for the PLL core.

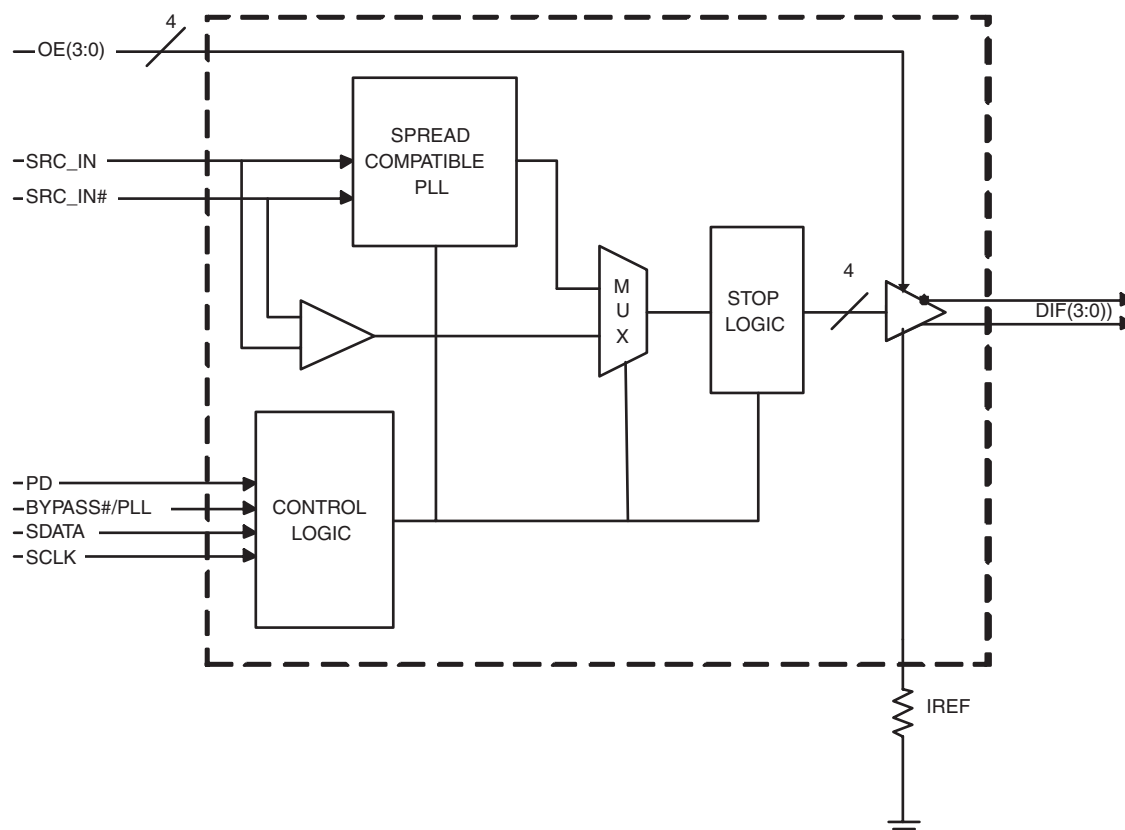
Pin Description When OE_INV = 1

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	VDD	PWR	Power supply, nominal 3.3V
2	SRC_IN	IN	0.7 V Differential SRC TRUE input
3	SRC_IN#	IN	0.7 V Differential SRC COMPLEMENTARY input
4	GND	PWR	Ground pin.
5	VDD	PWR	Power supply, nominal 3.3V
6	DIF_1	OUT	0.7V differential true clock output
7	DIF_1#	OUT	0.7V differential complement clock output
8	OE1#	IN	Active low input for enabling DIF pair 1. 1 = tri-state outputs, 0 = enable outputs
9	DIF_2	OUT	0.7V differential true clock output
10	DIF_2#	OUT	0.7V differential complement clock output
11	VDD	PWR	Power supply, nominal 3.3V
12	BYPASS#/PLL	IN	Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode
13	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
14	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
15	PD	IN	Asynchronous active high input pin used to power down the device. The internal clocks are disabled and the VCO is stopped.
16	SRC_STOP	IN	Active high input to stop SRC outputs.
17	HIGH_BW#	IN	3.3V input for selecting PLL Band Width 0 = High, 1= Low
18	VDD	PWR	Power supply, nominal 3.3V
19	DIF_5#	OUT	0.7V differential complement clock output
20	DIF_5	OUT	0.7V differential true clock output
21	OE6#	IN	Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs
22	DIF_6#	OUT	0.7V differential complement clock output
23	DIF_6	OUT	0.7V differential true clock output
24	VDD	PWR	Power supply, nominal 3.3V
25	OE_INV	IN	This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#)
26	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
27	GNDA	PWR	Ground pin for the PLL core.
28	VDDA	PWR	3.3V power for the PLL core.

General Description

The **ICS9DB401** follows the Intel DB400 Differential Buffer Specification v2.0. This buffer provides four PCI-Express SRC clocks. The **ICS9DB401** is driven by a differential input pair from a CK409/CK410/CK410M main clock generator, such as the ICS952601, ICS954101 or ICS954201. It provides outputs meeting tight cycle-to-cycle jitter (50ps) and output-to-output skew (50ps) requirements.

Block Diagram



Note: Polarities shown for OE_INV = 0.

Power Groups

Pin Number		Description
VDD	GND	
1	4	SRC_IN/SRC_IN#
5,11,18, 24	4	DIF(1,2,5,6)
N/A	27	IREF
28	27	Analog VDD & GND for PLL core

Absolute Max

Symbol	Parameter	Min	Max	Units
VDD_A	3.3V Core Supply Voltage		4.6	V
VDD_In	3.3V Logic Supply Voltage		4.6	V
V _{IL}	Input Low Voltage	GND-0.5		V
V _{IH}	Input High Voltage		V _{DD} +0.5V	V
T _s	Storage Temperature	-65	150	°C
T _{ambient}	Ambient Operating Temp	0	70	°C
T _{case}	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V _{IH}	3.3 V +/-5%	2		V _{DD} + 0.3	V	
Input Low Voltage	V _{IL}	3.3 V +/-5%	GND - 0.3		0.8	V	
Input High Current	I _{IH}	V _{IN} = V _{DD}	-5		5	uA	
Input Low Current	I _{IL1}	V _{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	
	I _{IL2}	V _{IN} = 0 V; Inputs with pull-up resistors	-200			uA	
Operating Supply Current	I _{DD3.3PLL}	Full Active, C _L = Full load;		175	200	mA	
	I _{DD3.3ByPass}			160	175	mA	
Powerdown Current	I _{DD3.3PD}	all diff pairs driven			40	mA	
		all differential pairs tri-stated			4	mA	
Input Frequency	F _{iPLL}	PLL Mode	50		200	MHz	
Input Frequency	F _{iBypass}	Bypass Mode (Revision B/REV ID = 1H)	0		333.33	MHz	
Input Frequency	F _{iBypass}	Bypass Mode (Revision C/REV ID = 2H)	0		400	MHz	
Pin Inductance ¹	L _{pin}				7	nH	1
Input Capacitance ¹	C _{IN}	Logic Inputs	1.5		4	pF	1
	C _{OUT}	Output pin capacitance			4	pF	1
PLL Bandwidth	BW	PLL Bandwidth when PLL_BW=0	2.4	3	3.4	MHz	1
		PLL Bandwidth when PLL_BW=1	0.7	1	1.4	MHz	1
Clk Stabilization ^{1,2}	T _{STAB}	From V _{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.5	1	ms	1,2
Modulation Frequency	fMOD	Triangular Modulation	30		33	kHz	1
Tdrive_SRC_STOP#		DIF output enable after SRC_Stop# de-assertion		10	15	ns	1,3
Tdrive_PD#		DIF output enable after PD# de-assertion			300	us	1,3
Tfall		Fall time of PD# and SRC_STOP#			5	ns	1
Trise		Rise time of PD# and SRC_STOP#			5	ns	2

¹Guaranteed by design and characterization, not 100% tested in production.

²See timing diagrams for timing requirements.

³Time from deassertion until outputs are >200 mV

Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

$T_A = 0 - 70^\circ\text{C}$; $V_{DD} = 3.3\text{ V} \pm 5\%$; $C_L = 2\text{pF}$, $R_S = 33.2\Omega$, $R_P = 49.9\Omega$, $I_{REF} = 475\Omega$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Z_O^1	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values			0	ppm	1,2
Rise Time	t_r	$V_{OL} = 0.175\text{V}$, $V_{OH} = 0.525\text{V}$	175		700	ps	1
Fall Time	t_f	$V_{OH} = 0.525\text{V}$, $V_{OL} = 0.175\text{V}$	175		700	ps	1
Rise Time Variation	d- t_r				125	ps	1
Fall Time Variation	d- t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential waveform	45		55	%	1
Skew	t_{sk3}	$V_T = 50\%$			50	ps	1
Jitter, Cycle to cycle	$t_{j\text{cyc-cyc}}$	PLL mode, Measurement from differential waveform			50	ps	1
		BYPASS mode as additive jitter			50	ps	1

¹Guaranteed by design and characterization, not 100% tested in production.

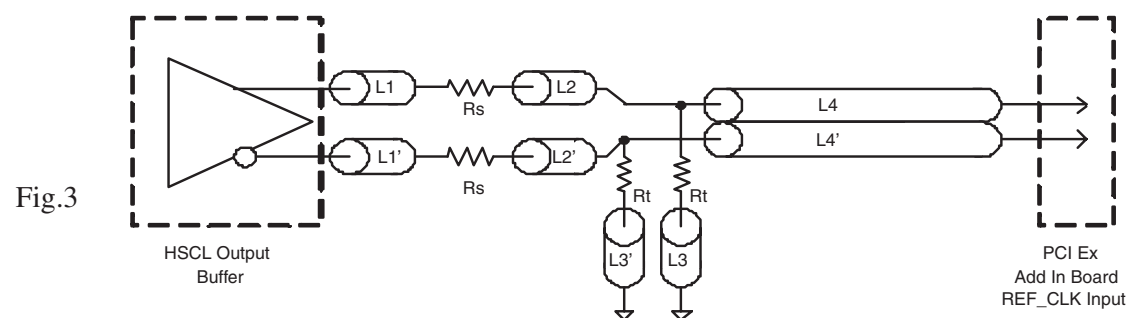
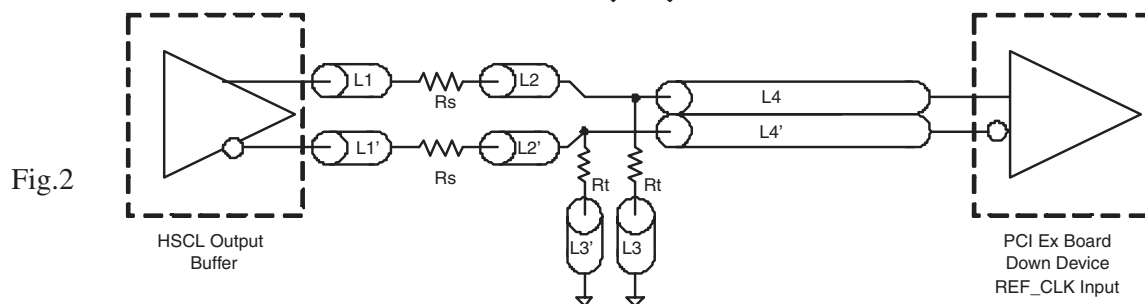
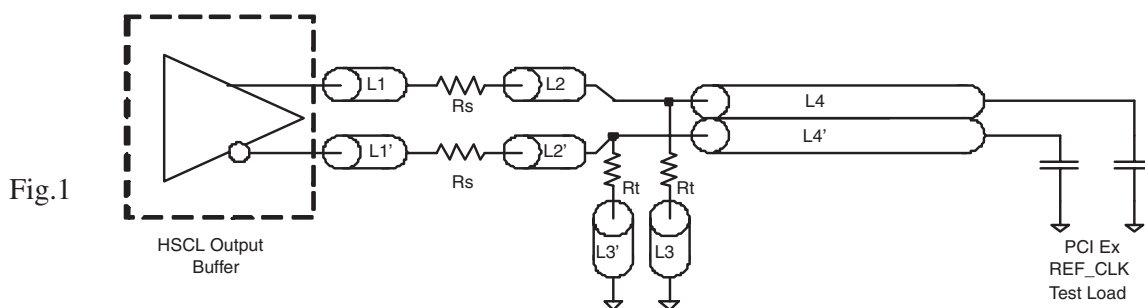
²All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that the input clock complies with CK409/CK410 accuracy requirements

³ $I_{REF} = V_{DD}/(3 \times R_R)$. For $R_R = 475\Omega$ (1%), $I_{REF} = 2.32\text{mA}$. $I_{OH} = 6 \times I_{REF}$ and $V_{OH} = 0.7\text{V}$ @ $Z_O = 50\Omega$.

SRC Reference Clock			
Common Recommendations for Differential Routing		Dimension or Value	Unit
L1 length, Route as non	-coupled 50 ohm trace.	0.5 max	inch
L2 length, Route as non	-coupled 50 ohm trace.	0.2 max	inch
L3 length, Route as non	-coupled 50 ohm trace.	0.2 max	inch
Rs		33	ohm
Rt		49.9	ohm

Down Device Differential Routing		Dimension or Value	Unit	Figure
L4 length, Route as coupled differential trace.	microstrip 100 ohm	2 min to 16 max	inch	2
L4 length, Route as coupled differential trace.	stripline 100 ohm	1.8 min to 14.4 max	inch	2

Differential Routing to PCI Express Connector		Dimension or Value	Unit	Figure
L4 length, Route as coupled differential trace.	microstrip 100 ohm	0.25 to 14 max	inch	3
L4 length, Route as coupled differential trace.	stripline 100 ohm	0.225 min to 12.6 max	inch	3



General SMBus serial interface information for the ICS9DB401

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $DC_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
(see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address DC _(H)			
R	Rite		
		ACK	
Beginning Byte N			
		ACK	
Data Byte Count			
		ACK	
Beginning Byte N		Byte	
			ACK
○			
○			○
○			○
			○
Byte N - 1			
		ACK	
P	stoP bit		

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $DC_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $DD_{(H)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address DC _(H)			
R	Rite		
		ACK	
Beginning Byte N			
		ACK	
RT	Repeat starT		
Slave Address DD _(H)			
RD	ReaD		
		ACK	
		Data Byte Count	
ACK			
		Byte	
ACK			Beginning Byte N
○			○
○			○
○			
		Byte N - 1	
N	Not acknowledge		
P	stoP bit		



SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (DC/DD)

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PD_Mode	PD# drive mode	RW	driven	Hi-Z	0
Bit 6	-	STOP_Mode	SRC_Stop# drive mode	RW	driven	Hi-Z	0
Bit 5	-	PD_SRC_INV	Power Down and SRC Invert	RW	Normal	Invert	0
Bit 4	-	Reserved	Reserved	RW	Reserved		X
Bit 3	-	Reserved	Reserved	RW	Reserved		X
Bit 2	-	PLL_BW#	Select PLL BW	RW	High BW	Low BW	1
Bit 1	-	BYPASS#	BYPASS#/PLL	RW	fan-out	ZDB	1
Bit 0	-	SRC_DIV#	SRC Divide by 2 Select	RW	x/2	1x	1

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		X
Bit 6	22,23	DIF_6	Output Control	RW	Disable	Enable	1
Bit 5	19,20	DIF_5	Output Control	RW	Disable	Enable	1
Bit 4	-	Reserved	Reserved	RW	Reserved		X
Bit 3	-	Reserved	Reserved	RW	Reserved		X
Bit 2	9,10	DIF_2	Output Control	RW	Disable	Enable	1
Bit 1	6,7	DIF_1	Output Control	RW	Disable	Enable	1
Bit 0	-	Reserved	Reserved	RW	Reserved		X

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		X
Bit 6	22,23	DIF_6	Output Control	RW	Free-run	Stoppable	0
Bit 5	19,20	DIF_5	Output Control	RW	Free-run	Stoppable	0
Bit 4	-	Reserved	Reserved	RW	Reserved		X
Bit 3	-	Reserved	Reserved	RW	Reserved		X
Bit 2	9,10	DIF_2	Output Control	RW	Free-run	Stoppable	0
Bit 1	6,7	DIF_1	Output Control	RW	Free-run	Stoppable	0
Bit 0	-	Reserved	Reserved	RW	Reserved		X



SMBus Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7			Reserved	RW	Reserved		X
Bit 6			Reserved	RW	Reserved		X
Bit 5			Reserved	RW	Reserved		X
Bit 4			Reserved	RW	Reserved		X
Bit 3			Reserved	RW	Reserved		X
Bit 2			Reserved	RW	Reserved		X
Bit 1			Reserved	RW	Reserved		X
Bit 0			Reserved	RW	Reserved		X

SMBus Table: Vendor & Revision ID Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: DEVICE ID

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID 7 (MSB)		RW	Reserved		0
Bit 6	-	Device ID 6		RW	Reserved		1
Bit 5	-	Device ID 5		RW	Reserved		0
Bit 4	-	Device ID 4		RW	Reserved		0
Bit 3	-	Device ID 3		RW	Reserved		0
Bit 2	-	Device ID 2		RW	Reserved		0
Bit 1	-	Device ID 1		RW	Reserved		0
Bit 0	-	Device ID 0		RW	Reserved		1

SMBus Table: Byte Count Register

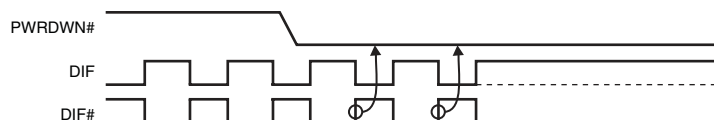
Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

PD#

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

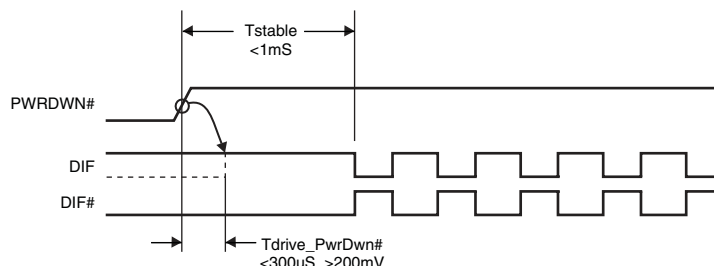
PD# Assertion

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to '0', all clock outputs will be held with DIF driven High with $2 \times I_{REF}$ and DIF# tri-stated. If the PD# drive mode bit is set to '1', both DIF and DIF# are tri-stated.



PD# De-assertion

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to '1', all the DIF outputs must driven to a voltage of >200 mV within 300 ms of PD# de-assertion.



Note: Polarities in timing diagrams are shown OE INV 0. They are similar to OE INV 1.

SRC_STOP#

The SRC_STOP# signal is an active-low asynchronous input that cleanly stops and starts the DIF outputs. A valid clock must be present on SRC_IN for this input to work properly. The SRC_STOP# signal is de-bounced and must remain stable for two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

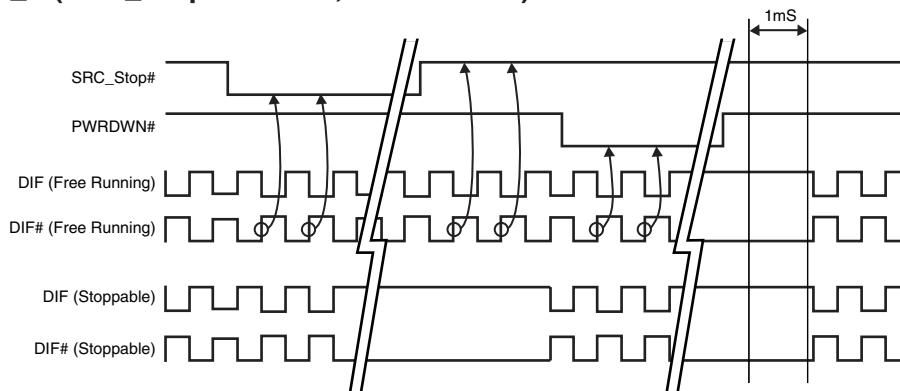
SRC_STOP# - Assertion (transition from '1' to '0')

Asserting SRC_STOP# causes all DIF outputs to stop after their next transition (if the control register settings allow the output to stop). When the SRC_STOP# drive bit is '0', the final state of all stopped DIF outputs is DIF = High and DIF# = Low. There is no change in output drive current. DIF is driven with $6 \times I_{REF}$. DIF# is not driven, but pulled low by the termination. When the SRC_STOP# drive bit is '1', the final state of all DIF output pins is Low. Both DIF and DIF# are not driven.

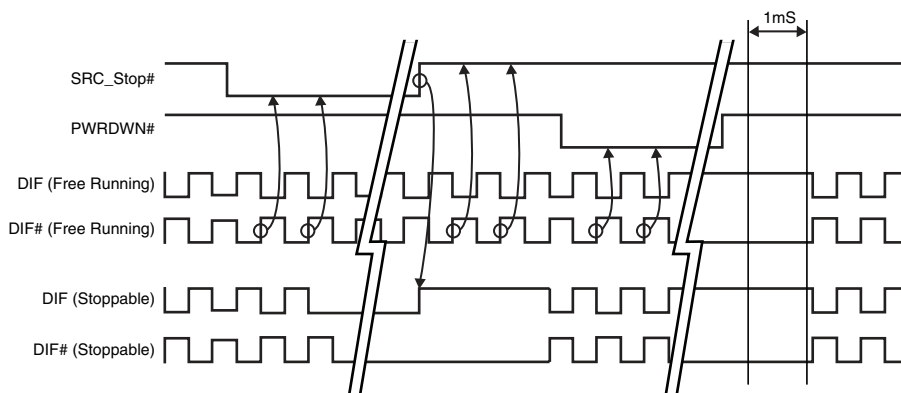
SRC_STOP# - De-assertion (transition from '0' to '1')

All stopped differential outputs resume normal operation in a glitch-free manner. The de-assertion latency to active outputs is 2-6 DIF clock periods, with all DIF outputs resuming simultaneously. If the SRC_STOP# drive control bit is '1' (tri-state), all stopped DIF outputs must be driven High (>200 mV) within 10 ns of de-assertion.

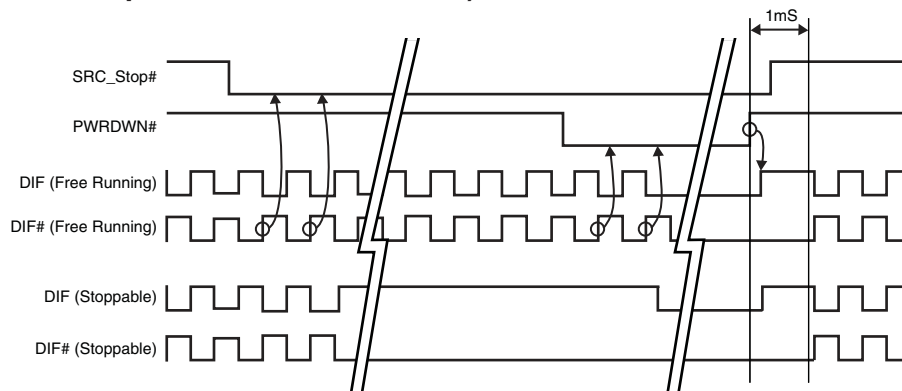
SRC_STOP_1 (SRC_Stop = Driven, PD = Driven)



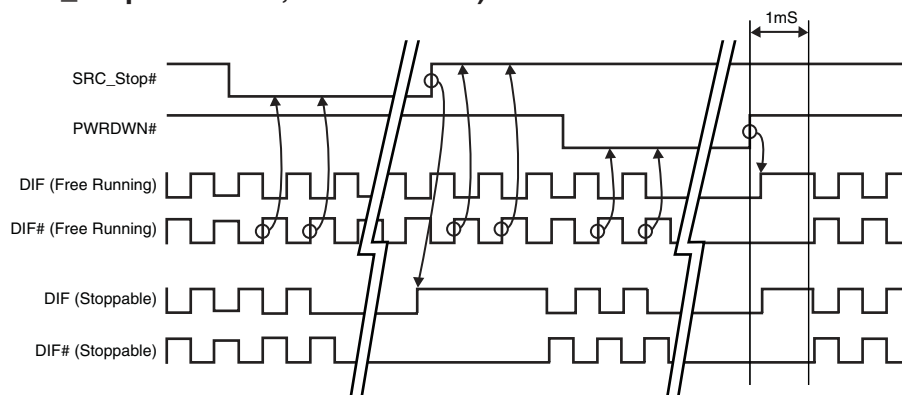
SRC_STOP_2 (SRC_Stop = Tri-state, PD = Driven)

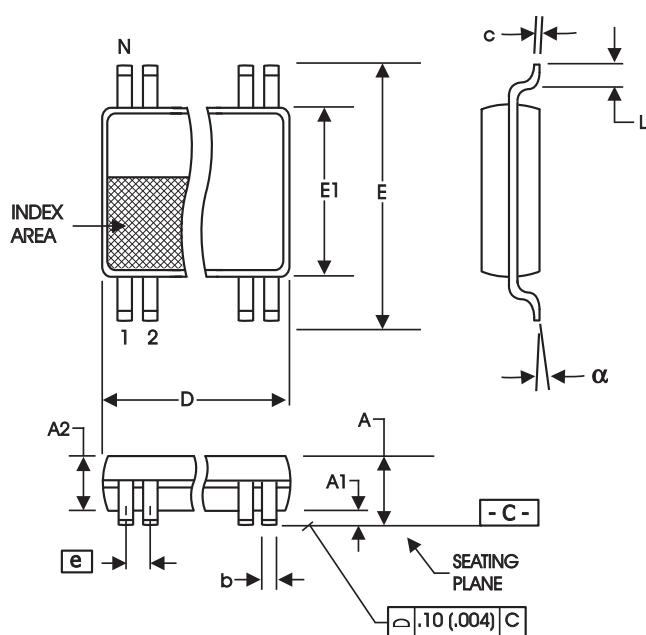


SRC_STOP_3 (SRC_Stop = Driven, PD = Tristate)



SRC_STOP_4 (SRC_Stop = Tristate, PD = Tristate)





209 mil SSOP

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS		COMMON DIMENSIONS	
	MIN	MA	MIN	MA
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0	8	0	8

VARIATIONS

N	D mm.		D (inch)	
	MIN	MA	MIN	MA
28	9.90	10.50	.390	.413

Reference Doc.: EDEC Publication 95, MO-150
10-0033

Ordering Information

ICS9DB401yFLFT

Example:

ICS XXXX y F L F T

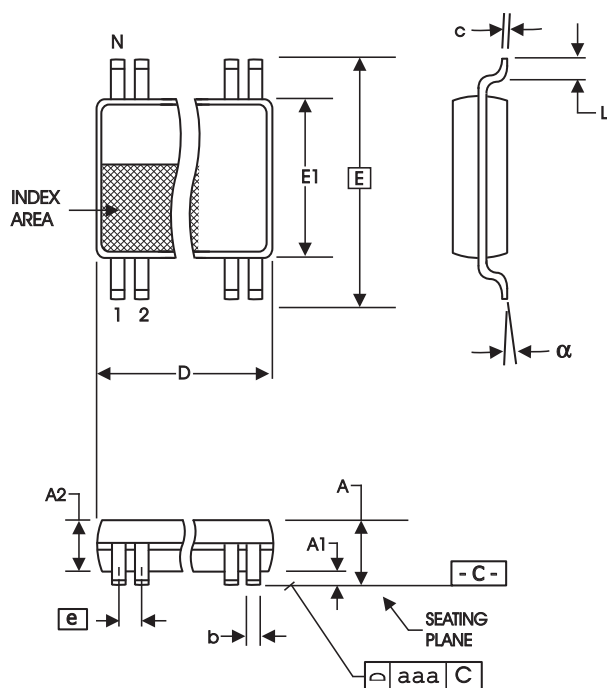
Designation for tape and reel packaging
RoHS Compliant (Optional)

Package Type
F = SSOP

Revision Designator (will not correlate with datasheet revision)

Device Type (consists of 3 to 7 digit numbers)

Prefix
ICS, AV = Standard Device



4.40 mm. Body, 0.65 mm. Pitch TSSOP

(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

ICS9DB401yGLFT

Example:

ICS XXXX y G LFT

- Designation for tape and reel packaging
- RoHS Compliant (Optional)
- Package Type
G = TSSOP
- Revision Designator (will not correlate with datasheet revision)
- Device Type (consists of 3 to 7 digit numbers)
- Prefix
ICS, AV = Standard Device



Revision History

Rev.	Issue Date	Description	Page #
0.1	4/21/2005	Changed Ordering Information from "LN" to "LF".	14,15
A	8/15/2005	1. Updated LF Ordering Information to RoHS Compliant. 2. Release to web.	14-15
B	9/7/2006	Updated Electrical Characteristics.	5

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9DB401 (Clock Buffers)

Description

Four Output Differential Buffer for PCI Express. DB800 Version 2.0 Yellow Cover part with PCI Express Support with extended bypass mode frequency range.

Market Group

PC CLOCK

Additional Info

The ICS9DB401 follows the Intel DB400 Differential Buffer Specification v2.0. This buffer provides four PCI-Express SRC clocks. The ICS9DB401 is driven by a differential input pair from a CK409/CK410/CK410M main clock generator, such as the ICS952601, ICS954101 or ICS954201. It provides outputs meeting tight cycle-to-cycle jitter (50ps) and output-to-output skew (50ps) requirements. 28-pin SSOP/TSSOP

**Time is
money**

Related Orderable Parts

Attributes	9DB401BFLF	9DB401BFLFT	9DB401BGLF	9DB401BGLFT	9DB401CFLF	9DB401CFLFT
Package	SSOP 28 (PYG28)	SSOP 28 (PYG28)	TSSOP 28 (PGG28)	TSSOP 28 (PGG28)	SSOP 28 (PYG28)	SSOP 28 (PYG28)
Speed	NA	NA	NA	NA	NA	NA
Temperature	C	C	C	C	C	C
Voltage	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Status	Active	Active	Active	Active	Active	Active
Sample	Yes	No	Yes	No	Yes	No
Minimum Order Quantity	188	1000	192	1000	188	1000
Factory Order Increment	47	1000	48	1000	47	1000

[1](#) [2](#)[1](#) [2](#)

Related Documents

Type	Title	Size	Revision Date
Datasheet	9DB401 Datasheet	244 KB	05/22/2007

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Related Orderable Parts

2
1

Attributes	9DB401BFLF	9DB401BFLFT	9DB401BGLF	9DB401BGLFT	9DB401CFLF	9DB401CFLFT
Package	SSOP 28 (PYG28)	SSOP 28 (PYG28)	TSSOP 28 (PGG28)	TSSOP 28 (PGG28)	SSOP 28 (PYG28)	SSOP 28 (PYG28)
Speed	NA	NA	NA	NA	NA	NA
Temperature	C	C	C	C	C	C
Voltage	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Status	Active	Active	Active	Active	Active	Active
Sample	Yes	No	Yes	No	Yes	No
Minimum Order Quantity	188	1000	192	1000	188	1000
Factory Order Increment	47	1000	48	1000	47	1000

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Related Documents

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Datasheet	9DB401 Datasheet	244 KB	05/22/2007