## General Description

The IDT8V41S104I is a PLL-based clock generator specifically designed for PCI EXPRESS™ Generation 3 applications. This device generates a 100MHz differential HCSL clock from an input reference of 25MHz. The input reference may be derived from an external source or by the addition of a 25MHz crystal to the on-chip crystal oscillator. The device offers spread spectrum clock output for reduced EMI applications. The spread spectrum control pins are used to enable or disable spread spectrum operation, as well as selecting either a down spread value of -0.35% or -0.5%. The enable and disable for each of the outputs is controlled via individual output enable pins. The IDT8V41S104I is packaged in a compact, lead-free (RoHS 6) 32-lead VFQFN package. The industrial temperature range supports high end computing, telecommunication and networking end equipment requirements.

## Features

- Four 0.7V current mode differential HCSL output pairs
- One 0.7V current mode differential HCSL reference output
- CLK, nCLK input can accept the following input levels: HCSL, LVDS, LVPECL, LVHSTL
- Crystal oscillator interface: 25MHz
- Output frequency: 100MHz
- RMS phase jitter @ 100MHz (12kHz – 20MHz): 1.2ps (typical)
- Spread Spectrum for electromagnetic interference (EMI) reduction
- Individual output control via output enable pins
- In bypass mode functions as a 1 to 5 fanout buffer
- PCI Express (2.5 Gb/S), Gen 2 (5 Gb/s) and Gen 3 (8 Gb/s) jitter compliant
- 3.3V operating supply mode
- -40°C to 85°C ambient operating temperature
- Available lead-free (RoHS 6) package

## Pin Assignment
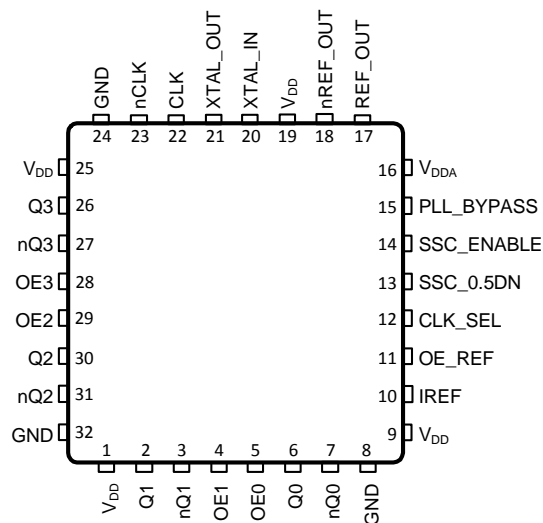


**IDT8V41S104I**
**32-Lead VFQFN**
**5mm x 5mm x 0.925mm package body**
**3.15mm x 3.15mm ePad size**
**NL Package**
**Top View**

## Block Diagram
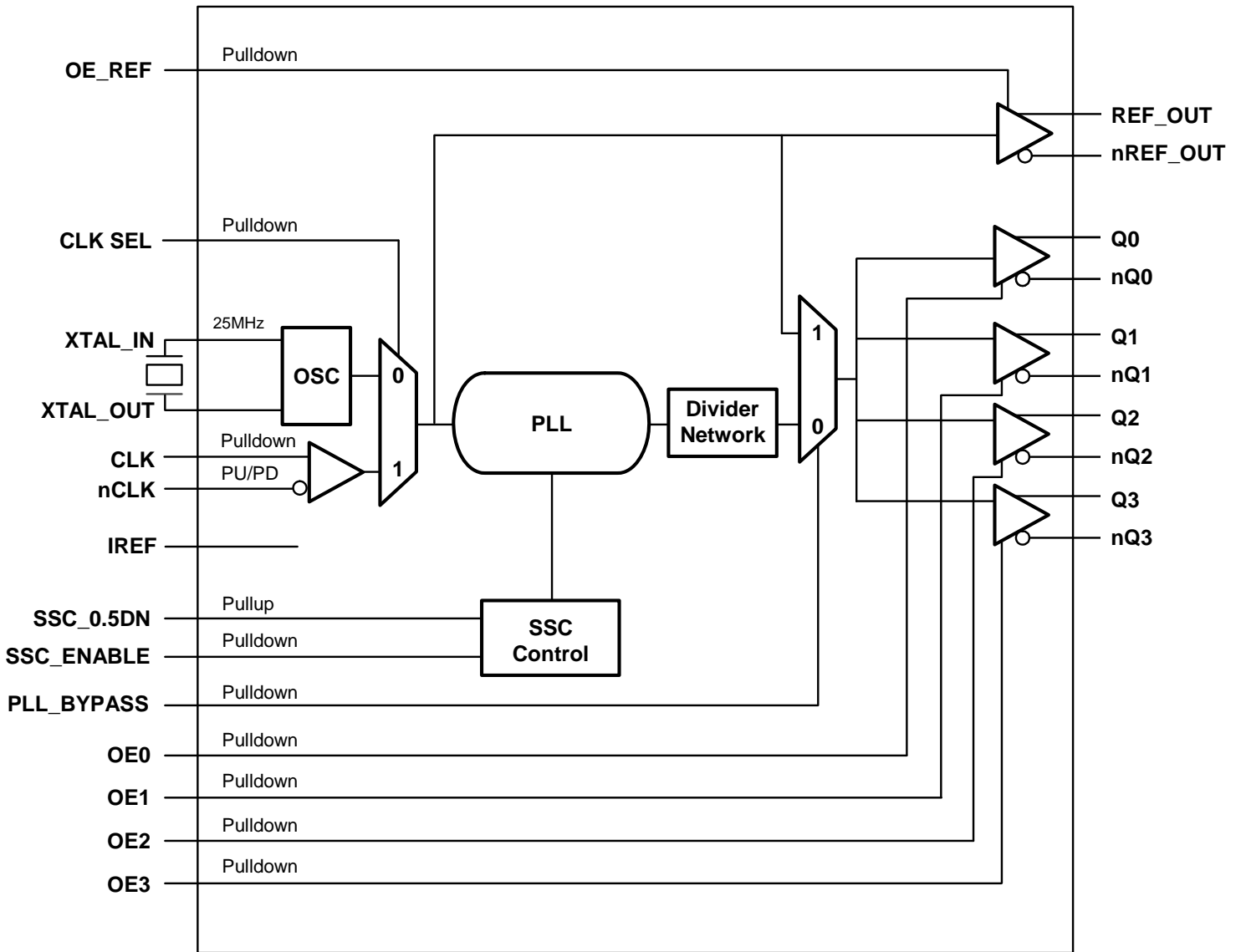
# Pin Description and Pin Characteristic Tables

**Table 1. Pin Descriptions**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 9, 19, 25 | $V_{DD}$ | Power | | Core supply voltage pins. |
| 2, 3 | Q1, nQ1 | Output | | Differential output pair. HSCL interface levels. |
| 4 | OE1 | Input | Pulldown | Active HIGH output enable for Q1, nQ1 differential output. LVCMOS/LVTTL interface levels.<br>OE1 = 0: Output disabled/high impedance (default)<br>OE1 = 1: Output enabled |
| 5 | OE0 | Input | Pulldown | Active HIGH output enable for Q0, nQ0 differential output. LVCMOS/LVTTL interface levels.<br>OE0 = 0: Output disabled/high impedance (default)<br>OE0 = 1: Output enabled |
| 6, 7 | Q0, nQ0 | Output | | Differential output pair. HCSL interface levels. |
| 8, 24, 32 | GND | Power | | Power supply ground. |
| 10 | IREF | Input | | An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for HCSL outputs. |
| 11 | OE_REF | Input | Pulldown | Active HIGH output enable for REF_OUT, nREF_OUT differential output. LVCMOS/LVTTL interface levels.<br>OE_REF = 0: Output disabled/high Impedance (default)<br>OE_REF = 1: Output enabled |
| 12 | CLK_SEL | Input | Pulldown | Active HIGH clock select input. Selects PLL input source. LVCMOS /LVTTL interface levels.<br>CLK_SEL = 0: XTAL_IN, XTAL_OUT (default)<br>CLK_SEL = 1: CLK, nCLK |
| 13 | SSC_0.5DN | Input | Pullup | Spread spectrum modulation level control. LVCMOS/LVTTL interface levels.<br>SSC_0.5DN = 0: -0.35%<br>SSC_0.5DN = 1: -0.5% (default) |
| 14 | SSC_ENABLE | Input | Pulldown | Spread spectrum enable. LVCMOS/LVTTL interface levels.<br>SSC_ENABLE = 0: Spread spectrum clocking off (default).<br>SSC_ENABLE = 1: Spread spectrum clocking on. |
| 15 | PLL_BYPASS | Input | Pulldown | Active HIGH PLL bypass. LVCMOS/LVTTL interface levels.<br>PLL_BYPASS = 0: PLL mode (default)<br>PLL_BYPASS = 1: Bypass mode |
| 16 | $V_{DDA}$ | Power | | Analog supply voltage. |
| 17, 18 | REF_OUT, nREF_OUT | Output | | Differential reference clock output pair. HCSL interface levels. |
| 20, 21 | XTAL_IN, XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 22 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 23 | nCLK | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{DD}$/2 default when left floating. |
| 26, 27 | Q3, nQ3 | Output | | Differential output pair. HCSL interface levels. |
| 28 | OE3 | Input | Pulldown | Active HIGH output enable for Q3, nQ3 differential output. LVCMOS/LVTTL interface levels.<br>OE3 = 0: Output disabled/high impedance (default)<br>OE3 = 1: Output enabled |
| 29 | OE2 | Input | Pulldown | Active HIGH output enable for Q2, nQ2 differential output. LVCMOS/LVTTL interface levels.<br>OE2 = 0: Output disabled/high impedance (default)<br>OE2 = 1: Output enabled |
| 30, 31 | Q2, nQ2 | Output | | Differential output pair. HCSL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

**Table 2. Pin Characteristics**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 2 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | $K\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | $K\Omega$ |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.
These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond
those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for
extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$<br> XTAL_IN<br> Other Inputs | 0V to $V_{DD}$<br>-0.5V to $V_{DD}$ + 0.5V |
| Outputs, $V_O$ | -0.5V to $V_{DD}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 39.5°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

# DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ =-40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA}$ | Analog Supply Voltage | | $V_{DD}$ – 0.30 | 3.3 | $V_{DD}$ | V |
| $I_{DD}$ | Power Supply Current | | | | 84 | mA |
| $I_{DDA}$ | Analog Supply Current | CLK, nCLK Input, SSC Enabled | | | 20 | mA |
| | | Crystal Input, SSC Enabled | | | 30 | mA |

NOTE: Characterized with all outputs disabled.

**Table 3B. LVCMOS/LVTTL DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ =-40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2.2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input<br>High Current | SSC_0.5DN, | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 10 | µA |
| | | CLK_SEL, OE_REF,<br>PLL_BYPASS,<br>SSC_ENABLE, OE0,<br>OE1, OE2, OE3 | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input<br>Low Current | SSC_0.5DN | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| | | CLK_SEL, OE_REF,<br>PLL_BYPASS,<br>SSC_ENABLE, OE0,<br>OE1, OE2, OE3 | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -10 | | | |

**Table 3C. Differential DC Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ =-40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|---|-----------------|---------|---------|---------|-------|
| $I_{IH}$ | Input High Current | CLK, nCLK | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | CLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | nCLK | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{PP}$ | Peak-to-Peak Input Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| $V_{CMR}$ | Common Mode Input Voltage; NOTE 1, 2 | | | GND + 0.5 | | $V_{DD}$ – 0.85 | V |

NOTE 1: $V_{IL}$ should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as $V_{IH}$.

**Table 4. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------|---------|---------|---------|-------|
| Mode of Oscillation | | | Fundamental | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Load Capacitance ($C_L$) | | 12 | | 18 | pF |

**Table 5. Input Frequency Characteristics,** $V_{DD}$ = 3.3V ± 5%, $T_A$ =-40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|---|-----------------|---------|---------|---------|-------|
| $f_{IN}$ | Input Frequency | XTAL_IN, XTAL_OUT | | | 25 | | MHz |
| | | CLK, nCLK | | | 25 | | MHz |

# AC Electrical Characteristics

**Table 6A. PCI Express Jitter Specifications,** $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | PCIe Industry Specification | Units |
|---|---|---|---|---|---|---|---|
| $t_j$ (PCIe Gen 1) | Phase Jitter Peak-to-Peak; NOTE 1, 4 | $f$ = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 18 | 27 | 86 | ps |
| $t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2) | Phase Jitter RMS; NOTE 2, 4 | $f$ = 100MHz, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2) | | 0.95 | 2.0 | 3.10 | ps |
| $t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2) | Phase Jitter RMS; NOTE 2, 4 | $f$ = 100MHz, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz | | 1.1 | 2.4 | 3.0 | ps |
| $t_{REFCLK\_RMS}$ (PCIe Gen 3) | Phase Jitter RMS; NOTE 3, 4 | $f$ = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2) | | 0.43 | 0.63 | 0.8 | ps |

**NOTE:** Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
**NOTE:** Characterized with Spread Spectrum Modulation disabled, unless otherwise noted.
**NOTE 1:** Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of $10^6$ clock periods.
**NOTE 2:** RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
**NOTE 3:** RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
**NOTE 4:** This parameter is guaranteed by characterization. Not tested in production.

## Table 6B. AC Characteristics, $V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | Q[0:3], nQ[0:3] | CLK, nCLK or Crystal Input = 25MHz (PLL Mode) | | 100 | | MHz |
| | | Q[0:3], nQ[0:3] | CLK, nCLK or Crystal Input = 25MHz (Bypass Mode) | | 25 | | MHz |
| | | REF_OUT, nREF_OUT | CLK, nCLK or Crystal Input = 25MHz | | 25 | | MHz |
| $t_{jit1}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 1 | | $f_{OUT}$ = 100MHz, 25MHz Crystal Input Integration Range: (12kHz to 20MHz) | | 1.21 | 1.67 | ps |
| $t_{jit2}(\emptyset)$ | Additive RMS Phase Jitter; refer to Additive Phase Jitter Section | | Bypass Mode; CLK, nCLK = 25MHz, Integration Range: (12kHz to 5MHz) | | 0.335 | 0.41 | ps |
| $t_{REF\_OUT\_RMS}$ | Phase Jitter RMS; NOTE 1 | | 25MHz Crystal Input, Integration Range: (12kHz to 5MHz) | | 0.548 | 0.70 | ps |
| $t_{sk}(o)$ | Output Skew; NOTE 2, 3 | Q[0:3], nQ[0:3] | 25MHz Crystal Input | | | 50 | ps |
| $t_{jit}(cc)$ | Cycle-to-Cycle Jitter; NOTE 2 | | PLL Mode | | | 36 | ps |
| $t_{jit}(per)$ | Period Jitter, RMS; NOTE 2 | | PLL Mode | | 2.1 | 2.6 | ps |
| $t_L$ | PLL Lock Time | | | | | 100 | ms |
| $V_{MAX}$ | Absolute Max. Output Voltage; NOTE 4, 5 | | | | | 1150 | mV |
| $V_{MIN}$ | Absolute Min. Output Voltage; NOTE 4, 6 | | | -300 | | | mV |
| $V_{RB}$ | Ringback Voltage; NOTE 7, 8 | | | -100 | | 100 | mV |
| $t_{STABLE}$ | Time before $V_{RB}$ is allowed; NOTE 7, 8 | | | 500 | | | ps |
| $V_{CROSS}$ | Absolute Crossing Voltage; NOTE 4, 9, 10 | | | 175 | | 550 | mV |
| $\Delta V_{CROSS}$ | Total Variation of $V_{CROSS}$ over all edges; NOTE 4, 9, 11 | | | | | 140 | mV |
| $t_{SLEW+}$ | Rising Edge Rate; NOTE 7, 12 | | Measured between 150mV to +150mV | 0.6 | | 4.0 | V/ns |
| $t_{SLEW-}$ | Falling Edge Rate; NOTE 7, 12 | | Measured between 150mV to +150mV | 0.6 | | 4.0 | V/ns |
| odc | Output Duty Cycle; NOTE 7 | | 25MHz Crystal Input, PLL Mode | 48 | | 52 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized with Spread Spectrum Modulation disabled, unless otherwise noted.
NOTE 1. Refer to Phase Noise Plot section.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4. Measurement taken from a single ended waveform.
NOTE 5. Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 6: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 7: Measurement taken from a differential waveform.
NOTE 8: $T_{STABLE}$ is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to drop back into the $V_{RB}$ ±100 mV differential range.
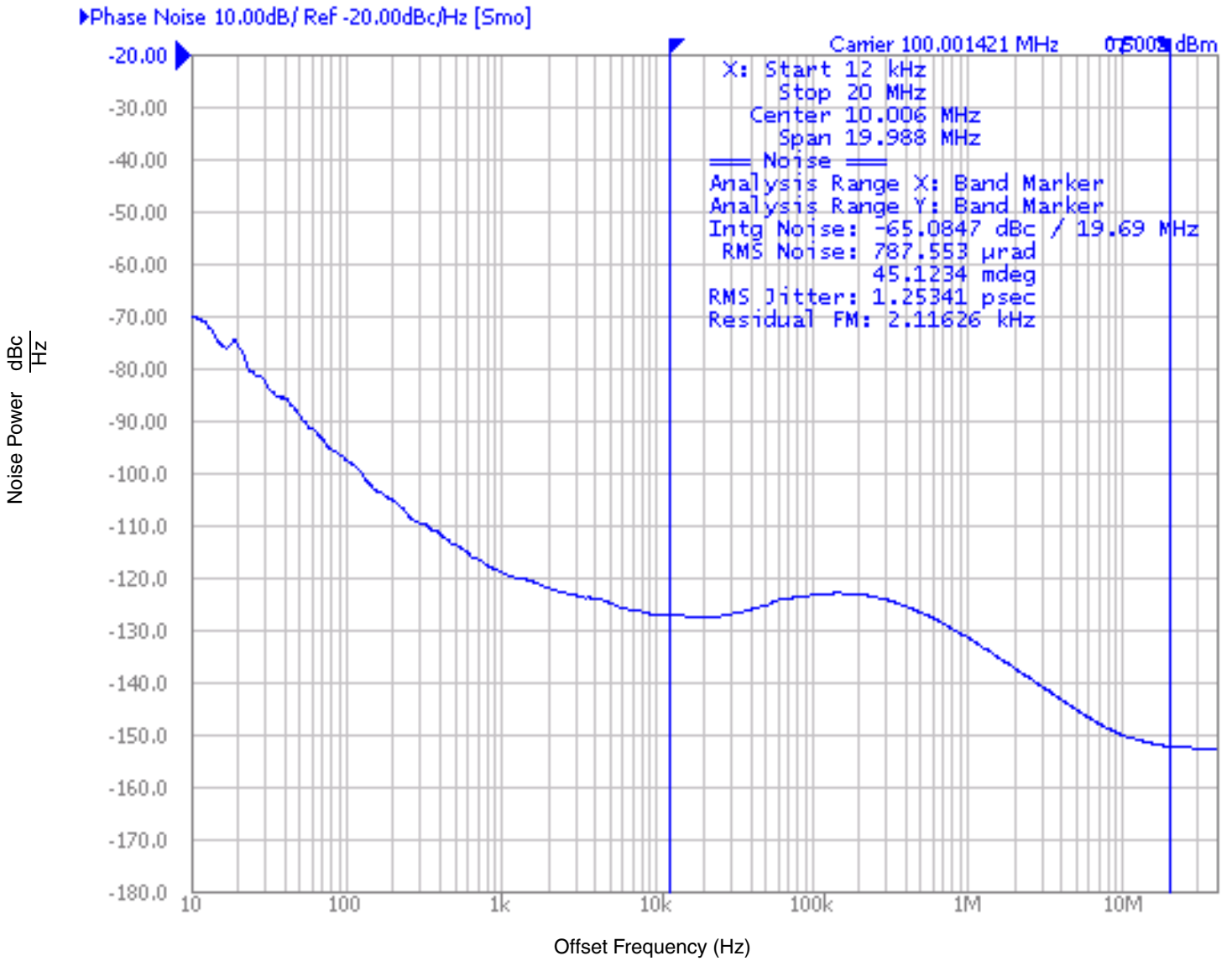NOTE 9: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.
NOTE 10: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
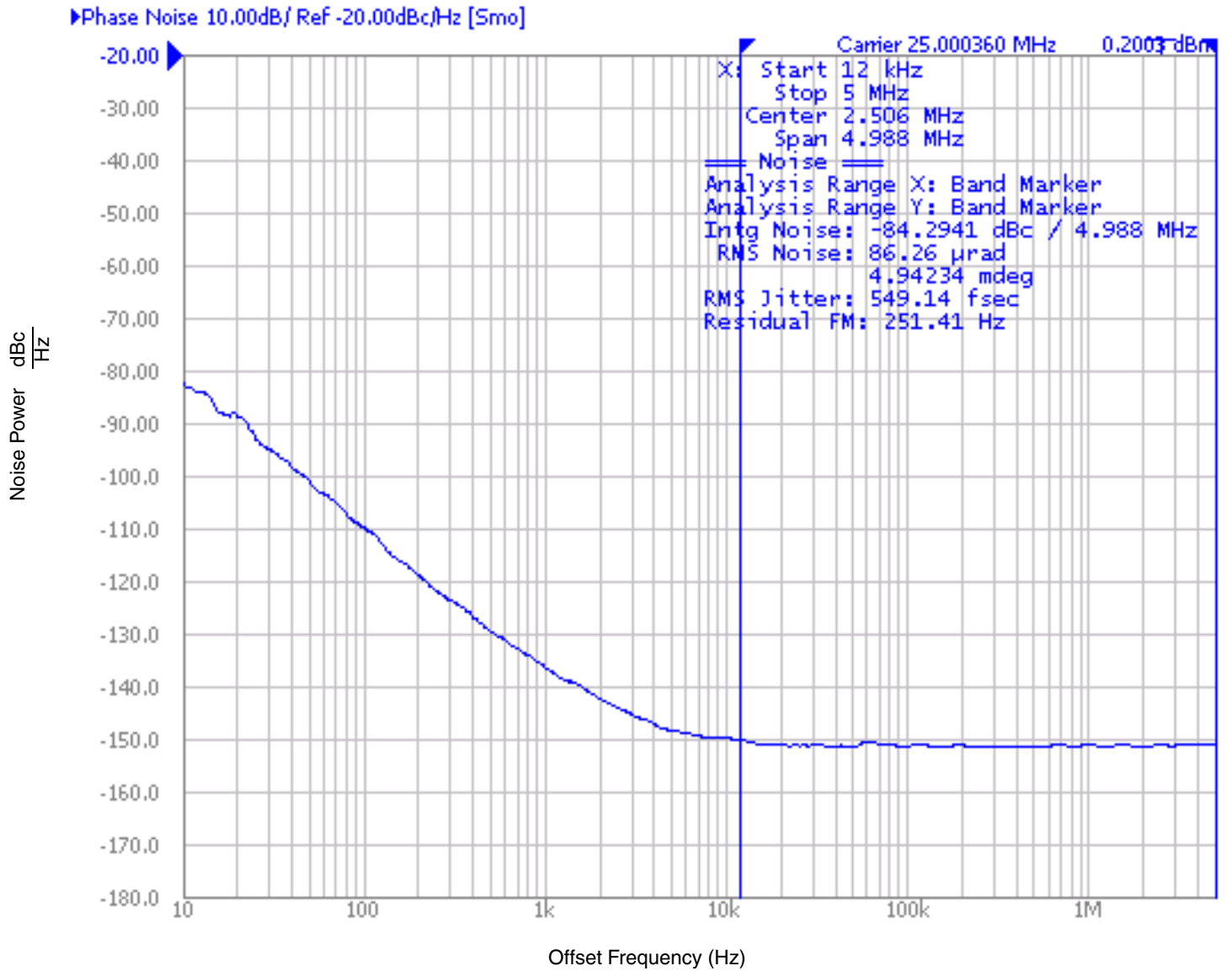NOTE 11:Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system. See Parameter Measurement Information Section.
NOTE 12: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

## Typical Phase Noise at 100MHz

## Typical Phase Noise at 25MHz



▶Phase Noise 10.00dB/ Ref -20.00dBc/Hz [Smo]

```
X:  Start 12 kHz
     Stop 5 MHz
   Center 2.506 MHz
     Span 4.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -84.2941 dBc / 4.988 MHz
  RMS Noise: 86.26 μrad
             4.94234 mdeg
RMS Jitter: 549.14 fsec
Residual FM: 251.41 Hz
```

Carrier 25.000360 MHz    0.2003 dBm

Noise Power $\frac{dBc}{Hz}$

Offset Frequency (Hz)

# Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



Additive Phase Jitter @ 25MHz
12kHz to 5MHz = 0.335ps (typical)
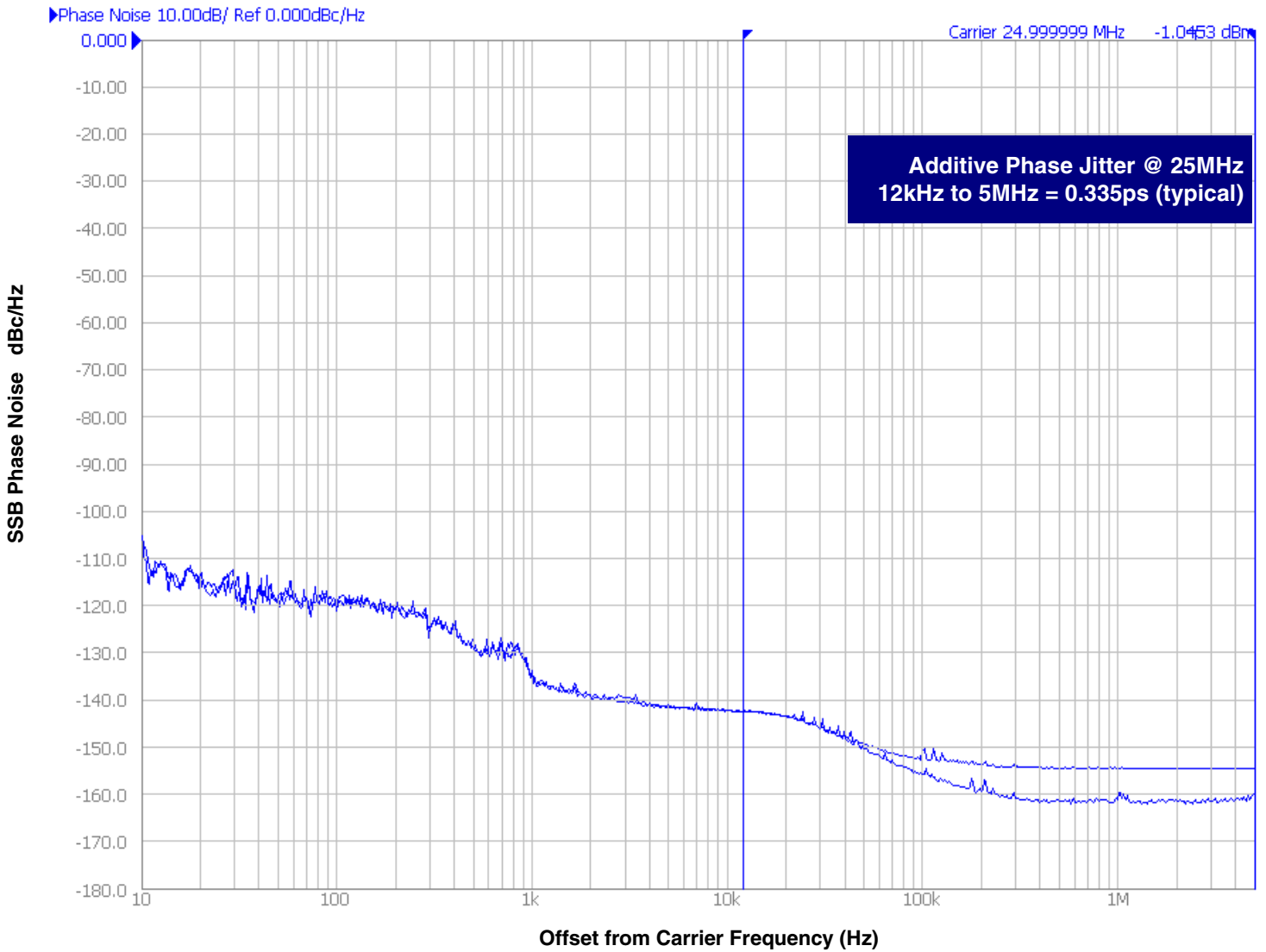
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Rohde & Schwarz SMA100 as the input source.

# Parameter Measurement Information

3.3V±5%

3.3V±5%

$V_{DD}$

$V_{DDA}$

10Ω

33Ω

50Ω

Measurement Point

49.9Ω

2pF

IREF

33Ω

50Ω

Measurement Point

GND

475Ω

49.9Ω

2pF

0V

0V

This load condition is used for $V_{MAX}$, $V_{MIN}$, $V_{RB}$, $t_{STABLE}$, $V_{CROSS}$, $\Delta V_{CROSS}$ and $t_{SLEW\pm}$ measurements.

**3.3V HCSL Output Load AC Test Circuit 1**

3.3V±5%

3.3V±5%

SCOPE

$V_{DD}$

$V_{DDA}$

10Ω

50Ω

50Ω

IREF

50Ω

GND

475Ω

50Ω

0V

0V

This load condition is used for tjit(cc), tjit(per), tjit(Ø), tjit and tsk(o) measurements.

**3.3V HCSL Output Load AC Test Circuit 2**

$V_{DD}$

nCLK

$V_{PP}$

Cross Points

$V_{CMR}$

CLK

GND

**Differential Input Level**

nQ[0:3], nREF_OUT

Q[0:3], REF_OUT

$t$cycle n

$t$cycle n+1

$$tjit(cc) = \frac{|tcycle\ n - tcycle\ n+1|}{1000\ Cycles}$$

**Cycle-to-Cycle Jitter**

$V_{OH}$

$V_{REF}$

$V_{OL}$

1σ contains 68.26% of all measurements
2σ contains 95.4% of all measurements
3σ contains 99.73% of all measurements
4σ contains 99.99366% of all measurements
6σ contains (100-1.973x10$^{-7}$)% of all measurements

Reference Point
(Trigger Edge)

Histogram
Mean Period
(First edge after trigger)

**Period Jitter**

nQx

Qx

nQy

Qy

$t$sk(o)

**Output Skew**

# Parameter Measurement Information, continued
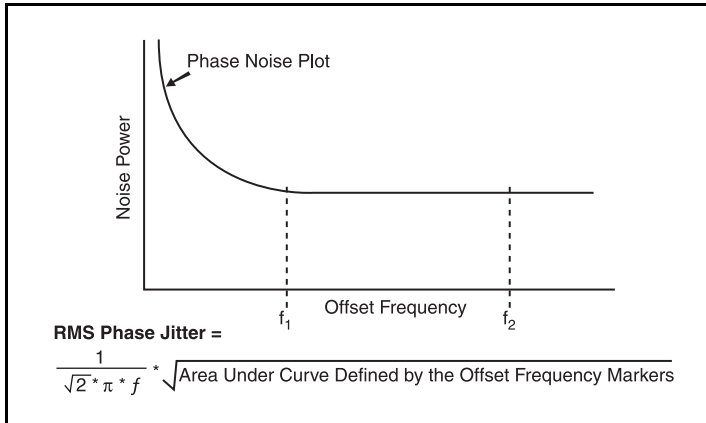


**RMS Phase Jitter**
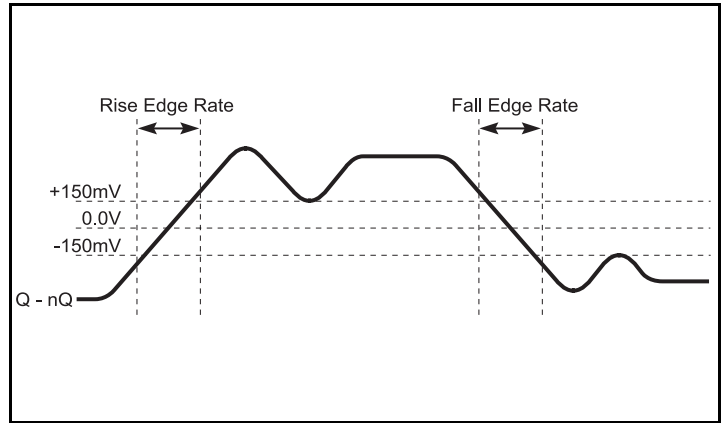


**Differential Measurement Points for Rise/Fall Edge Rate**
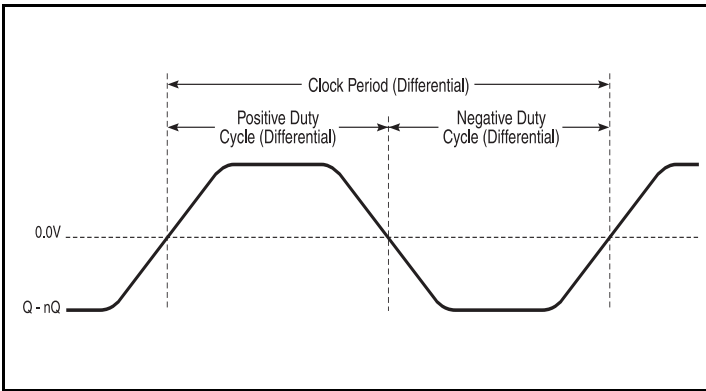


**Differential Measurement Points for Duty Cycle/Period**
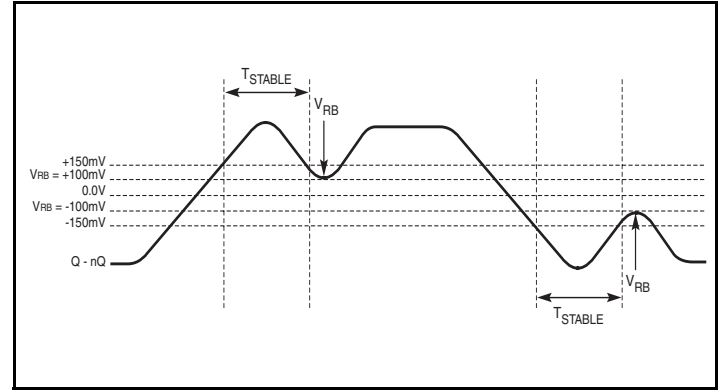


**Differential Measurement Points for Ringback**
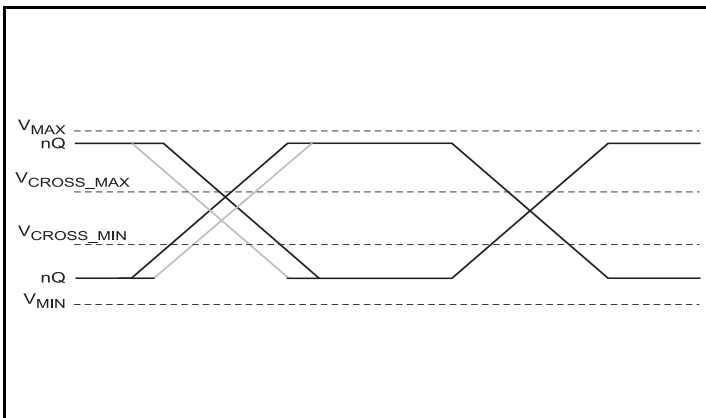


**Single-ended Measurement Points for Absolute Cross Point and Swing**
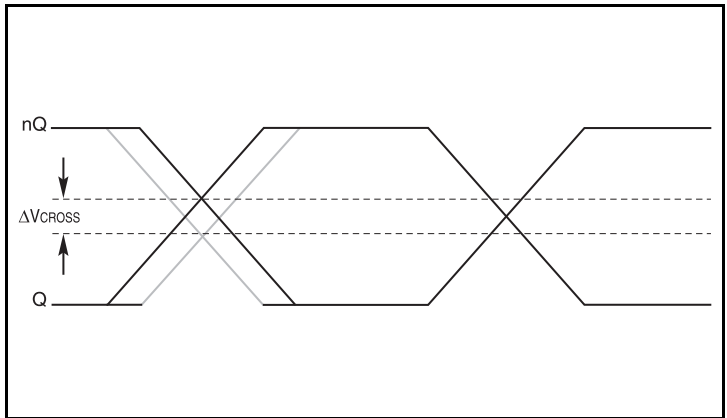


**Single-ended Measurement Points for Delta Cross Point**

# Parameter Measurement Information, continued
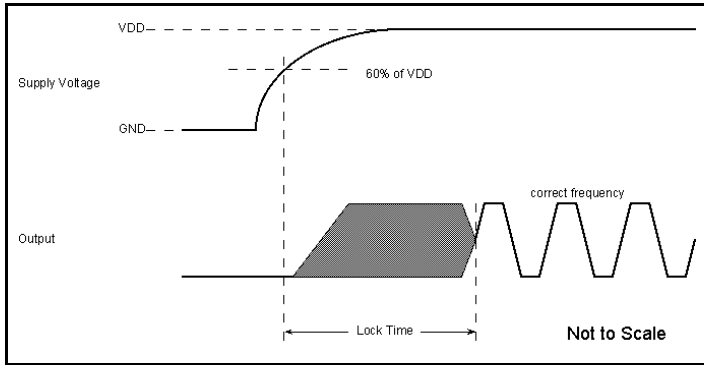


**PLL Lock Time**

# Applications Information

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

#### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

### Outputs:

#### Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

# Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the $V_1$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{DD}$ = 3.3V, R1 and R2 value should be adjusted to set $V_1$ at 1.25V. The values below are for when both the single ended swing and $V_{DD}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω.

The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{DD}$ + 0.3V. Suggested edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.
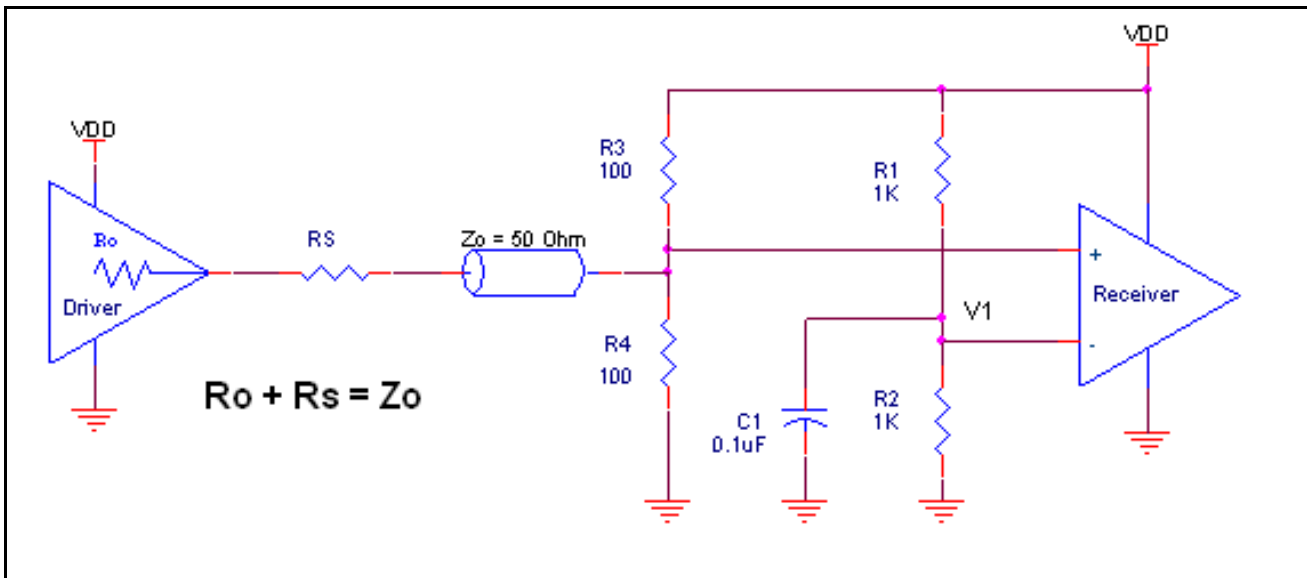


**Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels**

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both signals must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.
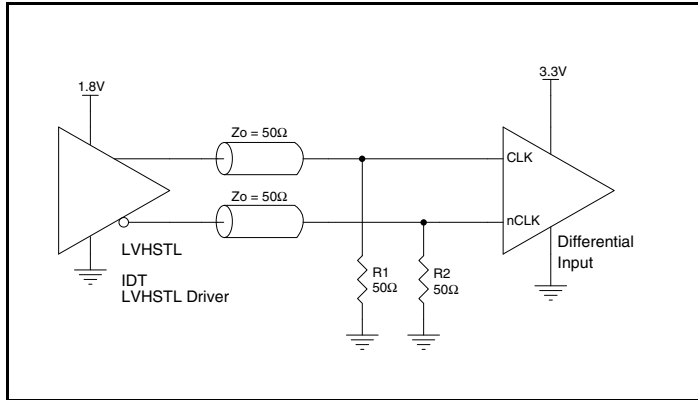
**Figure 2A.  CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**
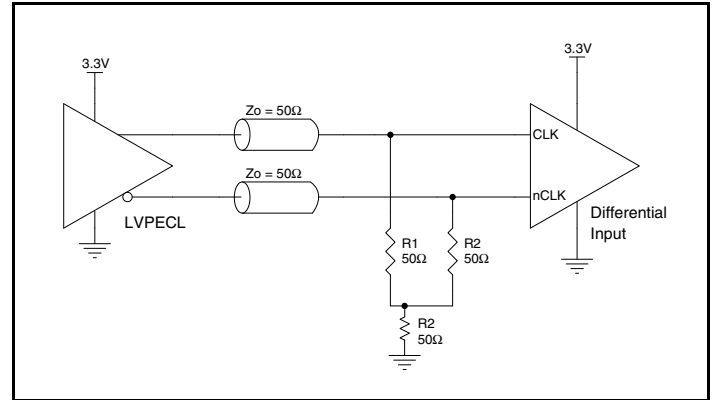
**Figure 2B.  CLK/nCLK Input Driven by a 3.3V LVPECL Driver**
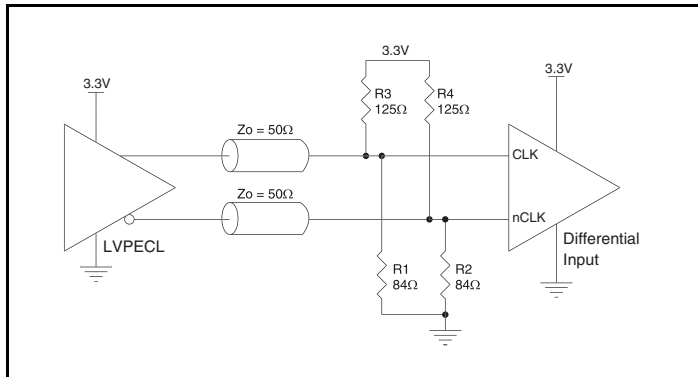
**Figure 2C.  CLK/nCLK Input Driven by a 3.3V LVPECL Driver**
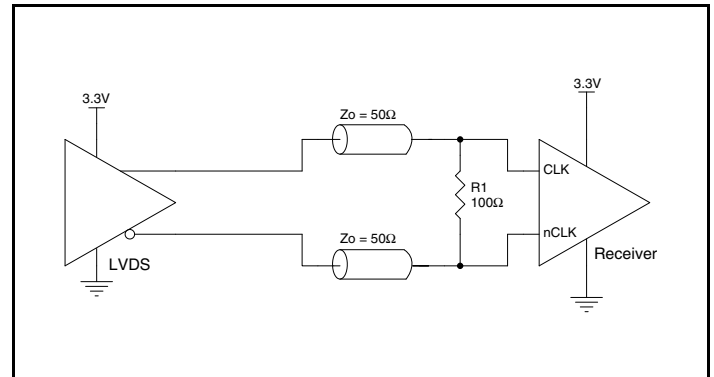
**Figure 2D.  CLK/nCLK Input Driven by a 3.3V LVDS Driver**
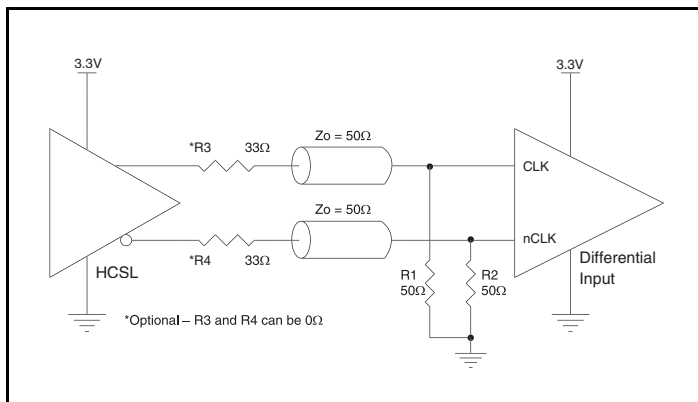
**Figure 2E.  CLK/nCLK Input Driven by a 3.3V HCSL Driver**

## Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.
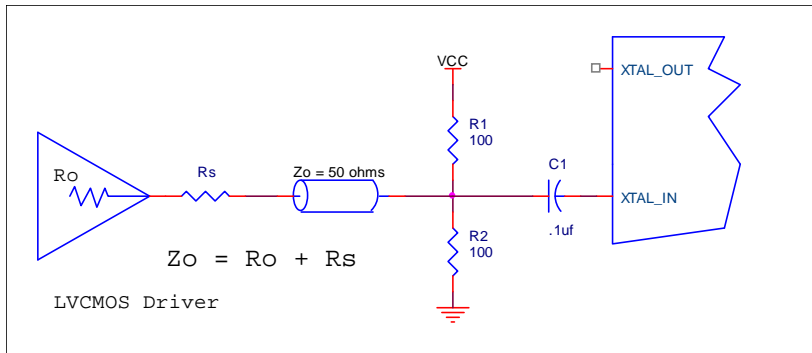


**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**
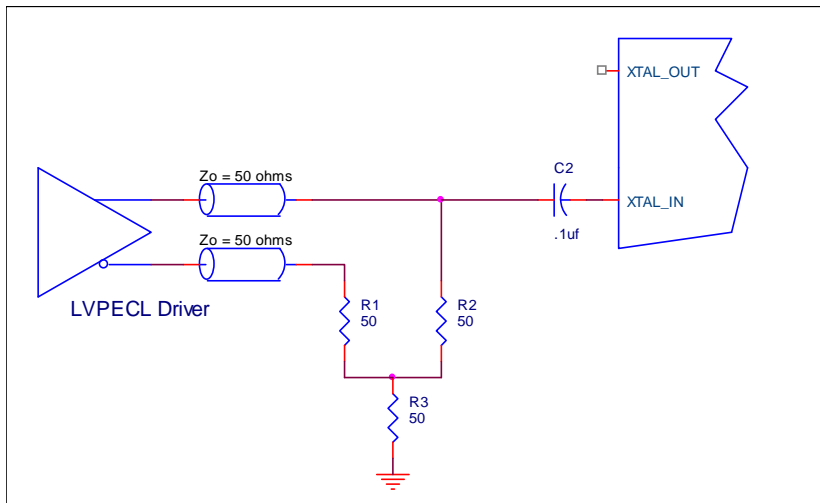


**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.
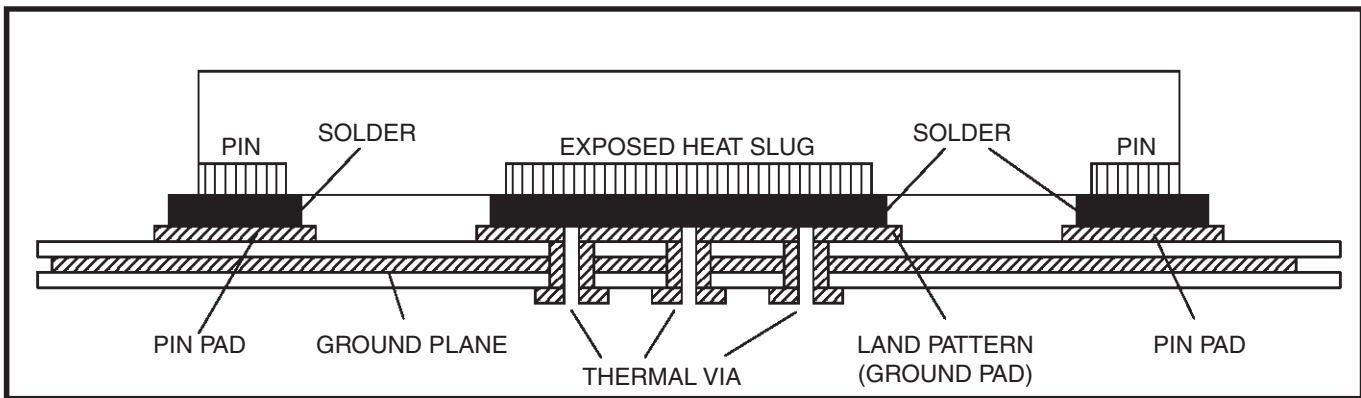


**Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

# Recommended Termination

*Figure 5A* is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output

types. All traces should be 50Ω impedance single-ended or 100Ω differential.
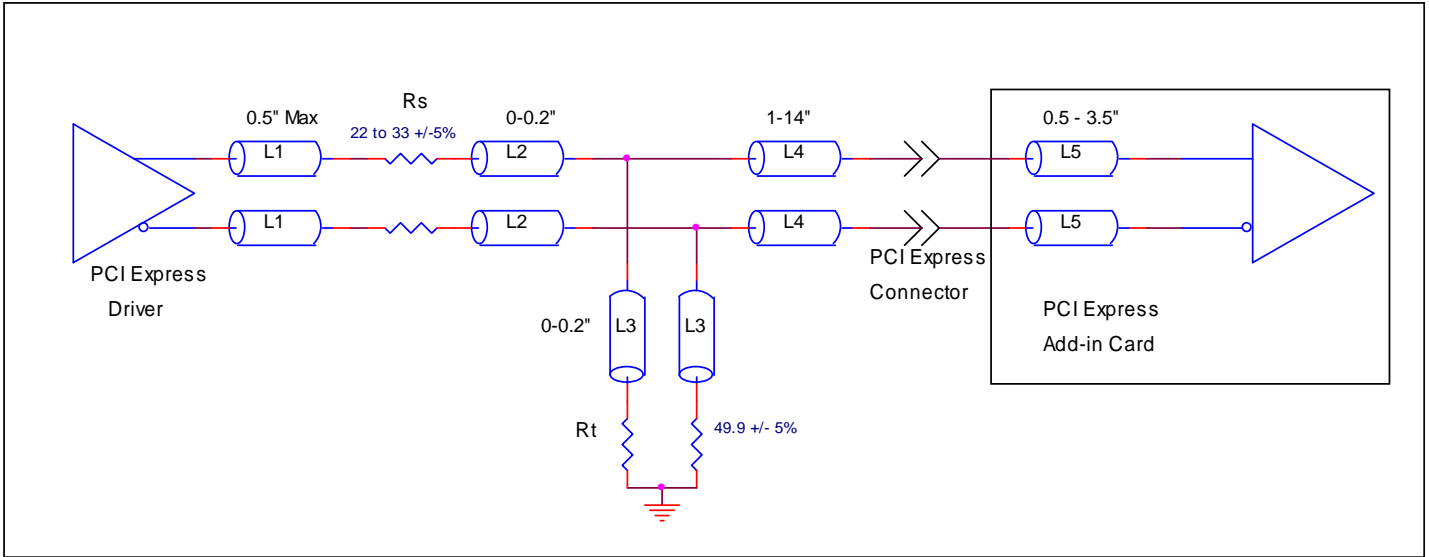


**Figure 5A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)**

*Figure 5B* is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.
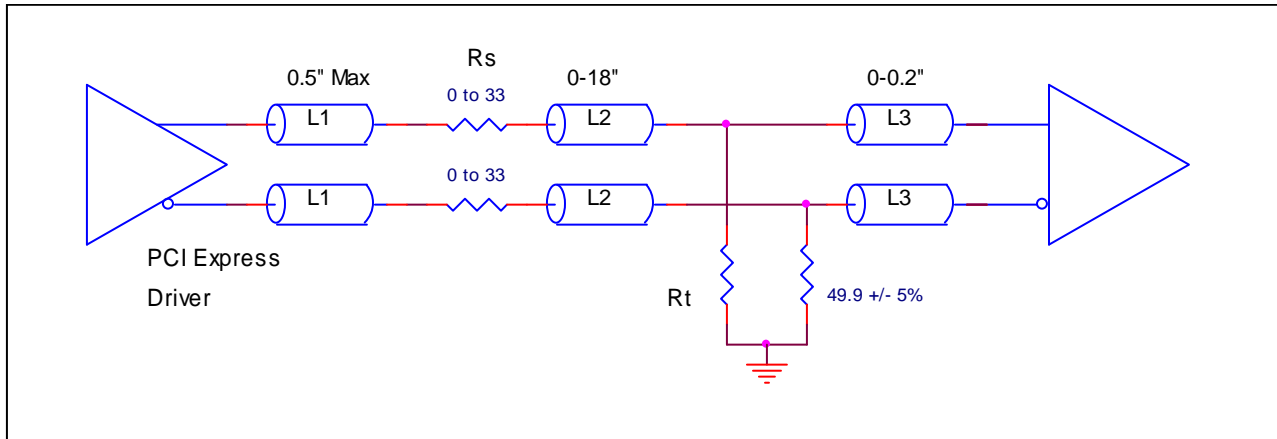


**Figure 5B. Recommended Termination (where a point-to-point connection can be used)**

# PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].
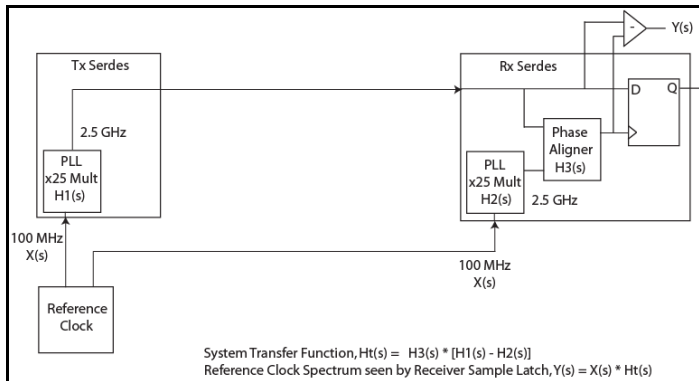


**PCI Express Common Clock Architecture**

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.
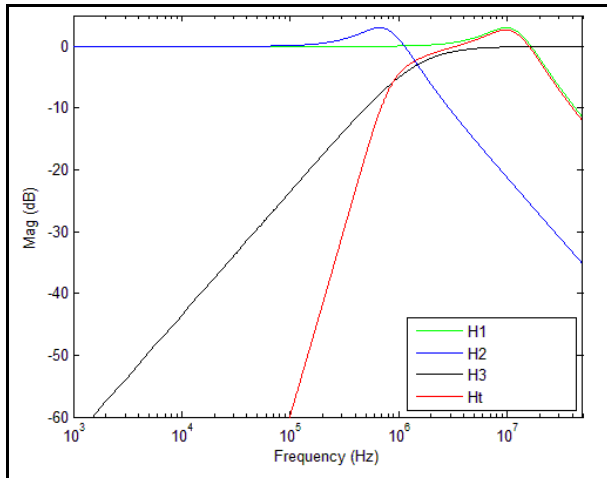


**PCIe Gen 1 Magnitude of Transfer Function**

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.
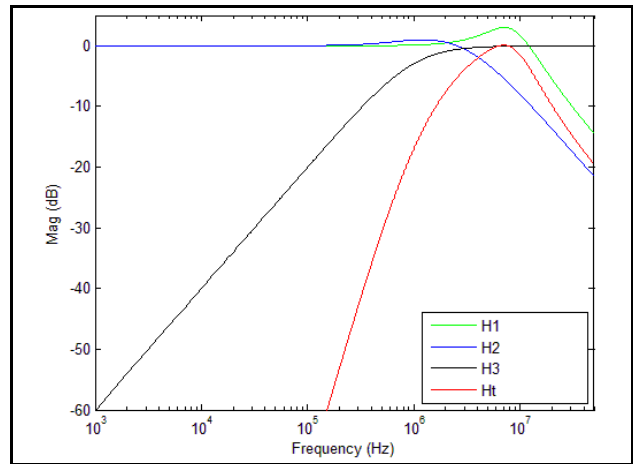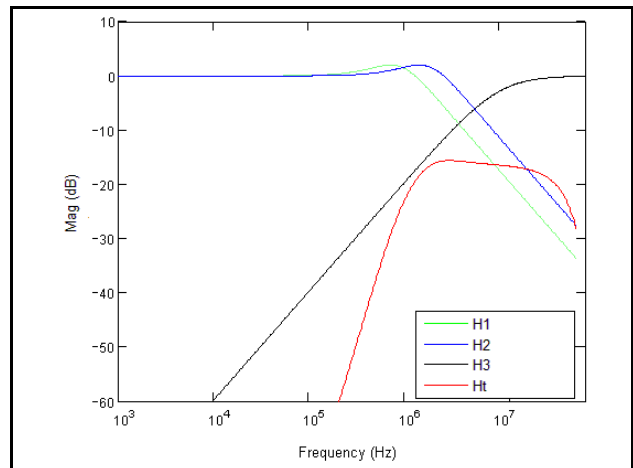


**PCIe Gen 2A Magnitude of Transfer Function**
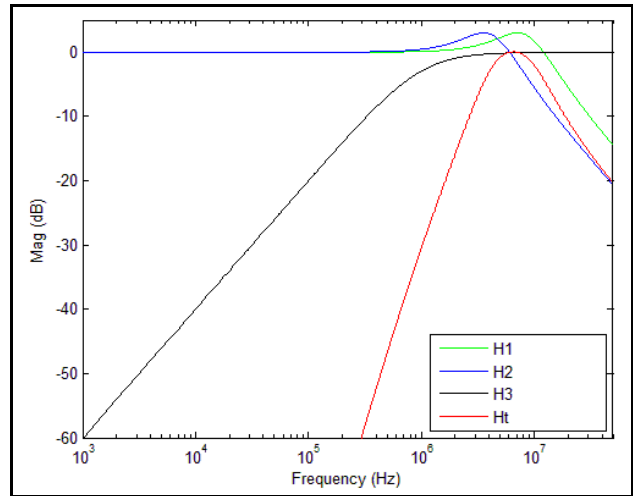


**PCIe Gen 2B Magnitude of Transfer Function**

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



**PCIe Gen 3 Magnitude of Transfer Function**

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

## Schematic Example

*Figure 6* (next page) shows an example of IDT8V41S104I application schematic. In this example, the device is operated at $V_{DD} = V_{DDA} = V_{DD\_REF} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The load capacitance C1 = 22pF and C2 = 22pF are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8V41S104I provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the

0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.
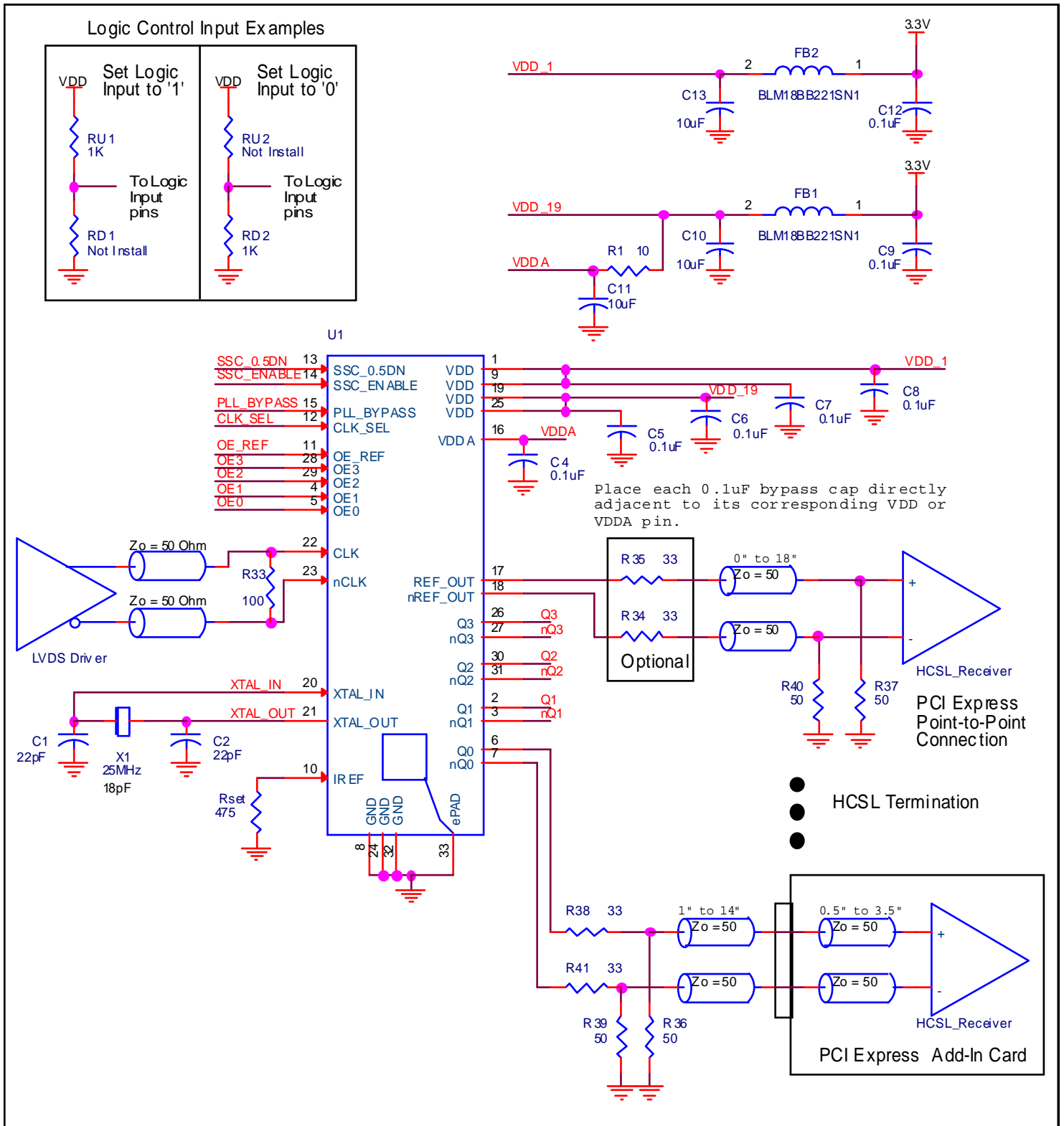
**Figure 6. IDT8V41S104I Schematic Example**

# Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8V41S104I.
Equations and example calculations are also provided.

### 1.   Power Dissipation.

The total power dissipation for the IDT8V41S104I is the sum of the core power plus analog plus the power dissipation into the load.
The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation into the load.

- Power (core)$_{MAX}$ = $V_{DD\_MAX}$ * ($I_{DD\_MAX}$ + $I_{DDA\_MAX}$) = 3.465V * (84mA + 30mA) = **395mW**

- Power (outputs)$_{MAX}$ = **44.5mW/Loaded Output pair**
  If all outputs are loaded, the total power is 5 * 44.5mW = **222.5mW**

**Total Power$_{\_MAX}$** = (3.465V, if all outputs are loaded) = 395mW + 222.5mW = **617.5mW**

### 2.   Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.618W * 39.5°C/W = 109.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance $\theta_{JA}$ for 32 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 39.5°C/W | 34.5°C/W | 31.0°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate power dissipation on the IC per HCSL output pairs.

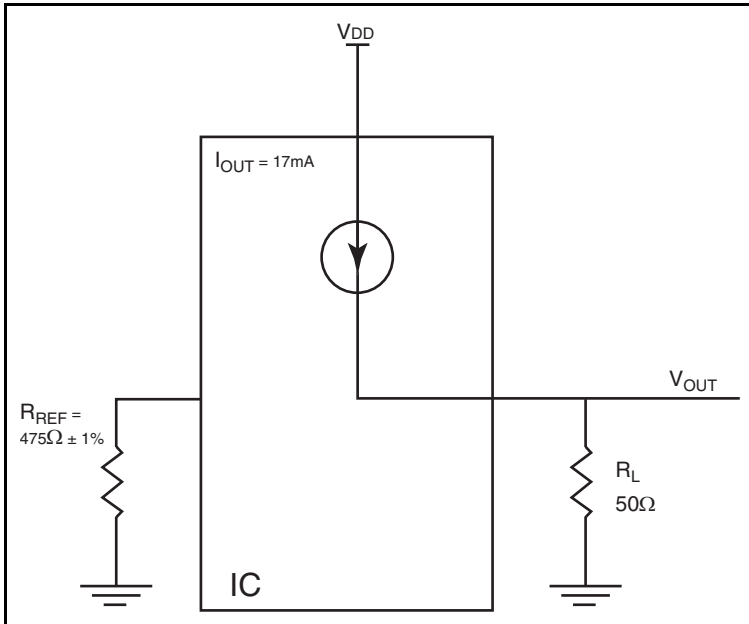HCSL output driver circuit and termination are shown in *Figure 7.*



**Figure 7. HCSL Driver Circuit and Termination**

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs at $V_{DD\_MAX}$.

Power $= (V_{DD\_MAX} - V_{OUT}) * I_{OUT}$
since $V_{OUT} = I_{OUT} * R_L$

Power $= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50Ω) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

# Reliability Information

**Table 8. $\theta_{JA}$ vs. Air Flow Table for a 32 Lead VFQFN**

| $\theta_{JA}$ vs. Air Flow | | | |
|---|---|---|---|
| Meters per Second | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 39.5°C/W | 34.5°C/W | 31.0°C/W |

# Transistor Count

The transistor count for IDT8V41S104I is: 11,988

## 32 Lead VFQFN Package Outline and Package Dimensions
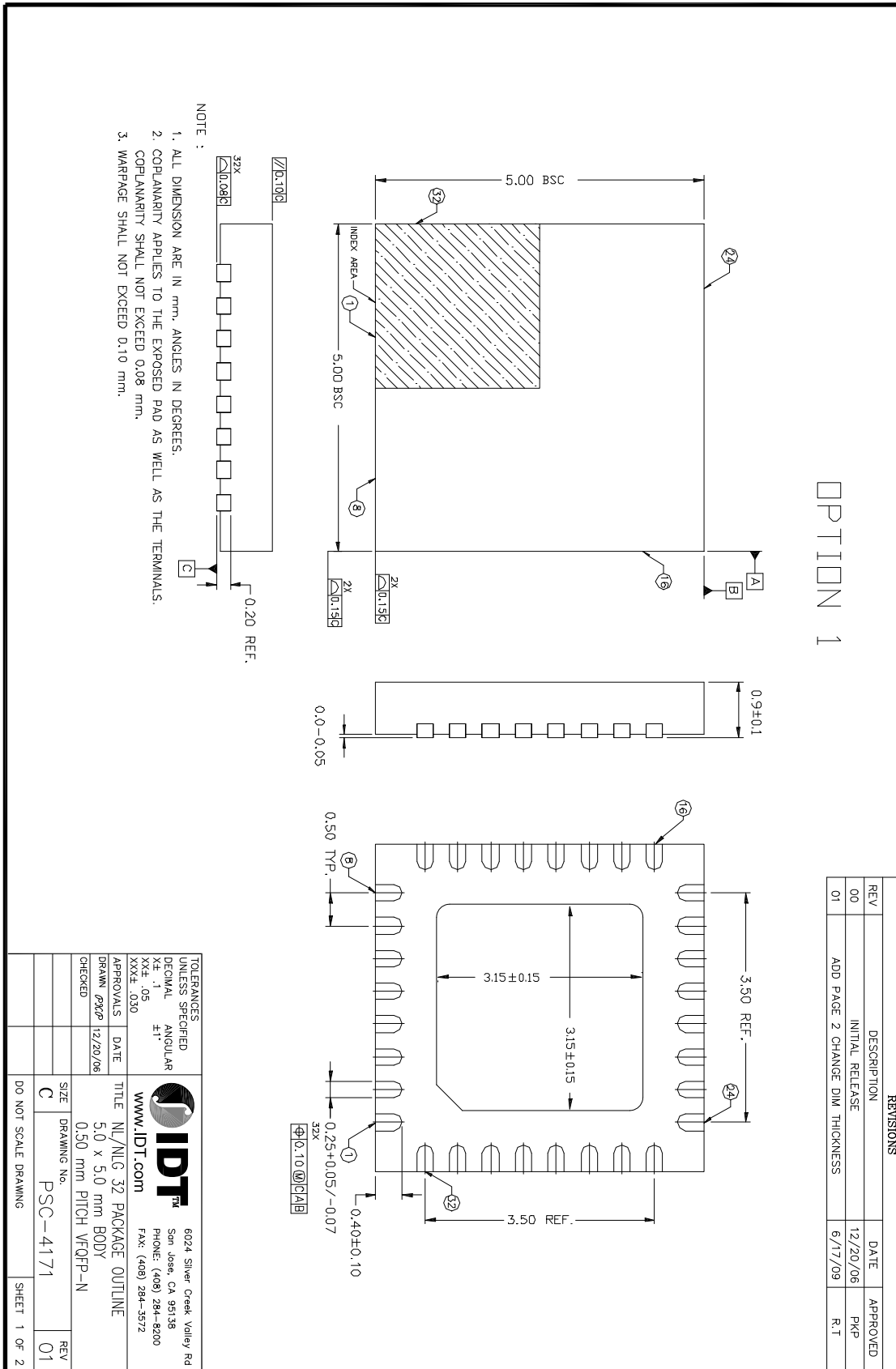
# Ordering Information

**Table 9. Ordering Information**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8V41S104NLGI | IDT8V41S104NLGI | 32 Lead VFQFN, Lead-Free | Tray | -40°C to 85°C |
| 8V41S104NLGI8 | IDT8V41S104NLGI | 32 Lead VFQFN, Lead-Free | Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

# Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| B | T3A | 5 | Power Supply DC Characteristics Table:<br>    Added $I_{DDA}$ specification row for Crystal Input. | 5/6/14 |
| | | 8 | AC Characteristics Table - added "PLL Mode" to test condition. | |
| | | 14 | Recommendations for Unused Input and Output Pins application note - Input Column, added Crystal Inputs. | |
| | T6B | 23 | Power Considerations - updated $I_{DDA}$ spec to correspond to Table 3A. | |

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