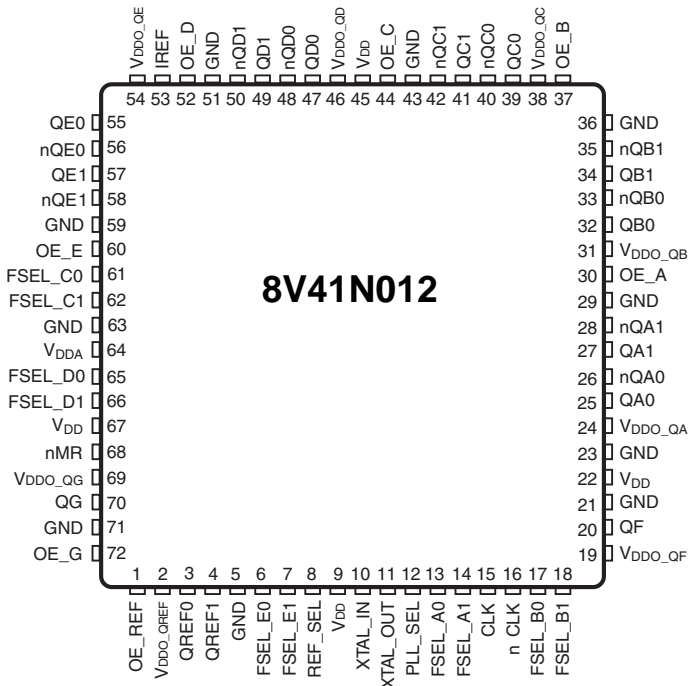


## General Description

The 8V41N012 is a PLL-based clock generator specifically designed for Cavium Networks Octeon II processors. This high performance device is optimized to generate the processor core reference clock, the PCI-Express, sRIO, XAUI, SerDes reference clocks and the clocks for both the Gigabit Ethernet MAC and PHY. The output frequencies are generated from a 25MHz external input source or an external 25MHz parallel resonant crystal. The industrial temperature range of the 8V41N012 supports telecommunication, networking, and storage requirements.

## Pin Assignment



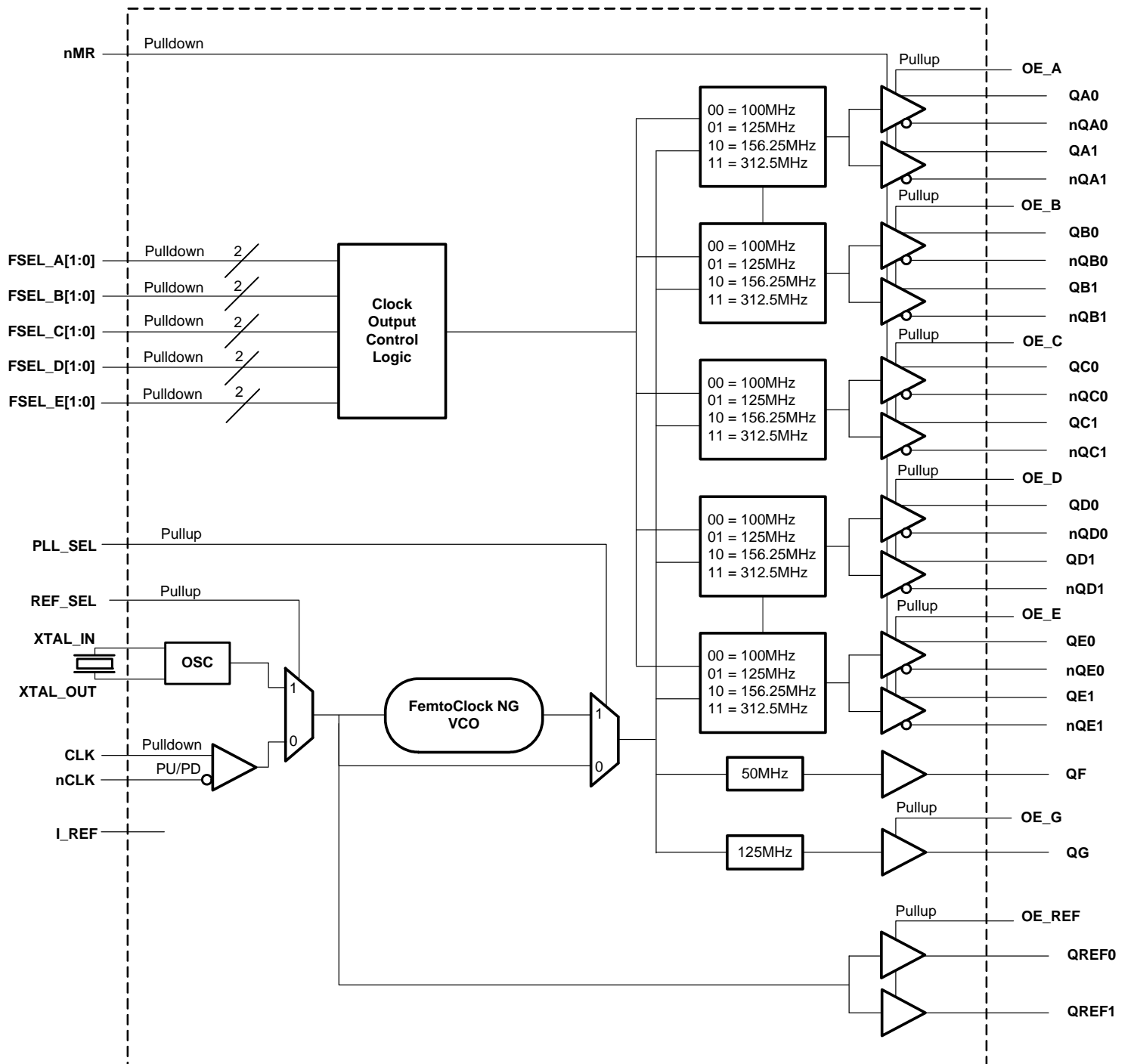
72-Lead, 10mm x 10mm VFQFN

NOTE: Exposed pad must always be connected to GND.  
NOTE: Pin 1 is located at bottom left corner as shown.

## Features

- Ten selectable 100MHz, 125MHz, 156.25MHz and 312.5MHz clocks for PCI Express, sRIO and GbE, HCSL interface levels
- One single-ended QG LVCMOS/LVTTL clock output at 125MHz
- One single-ended QF LVCMOS/LVTTL clock output at 50MHz
- Two single-ended QREFx LVCMOS/LVTTL outputs at 25MHz
- Selectable external crystal or differential (single-ended) input source
- Crystal oscillator interface designed for 25MHz, parallel resonant crystal
- Differential CLK, nCLK input pair that can accept: LVPECL, LVDS, LVHSTL, HCSL input levels
- Internal resistor bias on nCLK pin allows the user to drive CLK input with external single-ended (LVCMOS/ LVTTL) input levels
- Supply Modes, (125MHz QG output and 25MHz QREFx outputs):  
Core / Output  
3.3V / 3.3V  
3.3V / 2.5V
- Supply Modes, (HCSL outputs, and 50MHz QF output):  
Core / Output  
3.3V / 3.3V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

## Block Diagram



## Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE_REF	Input	Pullup	Active HIGH output enable for QREF0 and QREF1 outputs. LVCMOS/LVTTL interface levels. 0 = QREF0, QREF1 outputs disabled/high impedance 1 = QREF0, QREF1 outputs enabled (default)
2	V <sub>DDO_QREF</sub>	Power		QREF0, QREF1 output supply pin (LVCMOS/LVTTL). 3.3V or 2.5V supply.
3, 4	QREF0, QREF1	Output		Single-ended REF outputs. 3.3V or 2.5V LVCMOS/LVTTL interface levels.
5, 21, 23, 29, 36, 43, 51, 59, 63, 71	GND	Power		Power supply ground.
6, 7	FSEL_E0 FSEL_E1	Input	Pulldown	Selects the QEx, nQEx output frequency. LVCMOS/LVTTL interface levels. 00 = 100MHz (default) 01 = 125MHz 10 = 156.25MHz 11 = 312.5MHz
8	REF_SEL	Input	Pullup	Input source control pin. LVCMOS/LVTTL interface levels. 0 = CLK, nCLK 1 = XTAL (default)
9, 22, 45, 67	V <sub>DD</sub>	Power		Core supply pins.
10, 11	XTAL_IN XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
12	PLL_SEL	Input	Pullup	PLL bypass control pin. LVCMOS/LVTTL interface levels. 0 = Bypass mode 1 = PLL mode (default)
13, 14	FSEL_A0 FSEL_A1	Input	Pulldown	Selects the QAx, nQAx output frequency. LVCMOS/LVTTL interface levels. 00 = 100MHz (default) 01 = 125MHz 10 = 156.25MHz 11 = 312.5MHz
15	CLK	Input	Pulldown	Non-inverting differential clock input.
16	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to V <sub>DD</sub> /2.
17, 18	FSEL_B0 FSEL_B1	Input	Pulldown	Selects the QBx, nQBx output frequency. LVCMOS/LVTTL interface levels. 00 = 100MHz (default) 01 = 125MHz 10 = 156.25MHz 11 = 312.5MHz
19	V <sub>DDO_QF</sub>	Power		QF output supply pin (LVCMOS/LVTTL). 3.3V supply.
20	QF	Output		Single-ended output. 3.3V LVCMOS/LVTTL interface levels.
24	V <sub>DDO_QA</sub>	Power		Bank A (HCSL) output supply pin. 3.3 V supply.
25, 26	QA0, nQA0	Output		Bank A differential output pair. HCSL interface levels.
27, 28	QA1, nQA1	Output		Bank A differential output pair. HCSL interface levels.
30	OE_A	Input	Pullup	Active HIGH output enable for Bank A outputs. LVCMOS/LVTTL interface levels. 0 = Bank A outputs disabled/high impedance 1 = Bank A outputs enabled (default)
31	V <sub>DDO_QB</sub>	Power		Bank B (HCSL) output supply pin. 3.3V supply.

Continued on next page

**Table 1. Pin Descriptions, Continued**

Number	Name	Type		Description
32, 33	QB0, nQB0	Output		Bank B differential output pair. HCSL interface levels.
34, 35	QB1, nQB1	Output		Bank B differential output pair. HCSL interface levels.
37	OE_B	Input	Pullup	Active HIGH output enable for Bank B outputs. LVCMOS/LVTTL interface levels. 0 = Bank B outputs disabled/high impedance 1 = Bank B outputs enabled (default)
38	V <sub>DDO_QC</sub>	Power		Bank C (HCSL) output supply pin. 3.3V supply.
39, 40	QC0, nQC0	Output		Bank C differential output pair. HCSL interface levels.
41, 42	QC1, nQC1	Output		Bank C differential output pair. HCSL interface levels.
44	OE_C	Input	Pullup	Active HIGH output enable for Bank C outputs. LVCMOS/LVTTL interface levels. 0 = Bank C outputs disabled/high impedance 1 = Bank C outputs enabled (default)
46	V <sub>DDO_QD</sub>	Power		Bank D (HCSL) output supply pin. 3.3V supply.
47, 48	QD0, nQD0	Output		Bank D differential output pair. HCSL interface levels.
49, 50	QD1, nQD1	Output		Bank D differential output pair. HCSL interface levels.
52	OE_D	Input	Pullup	Active HIGH output enable for Bank D outputs. LVCMOS/LVTTL interface levels. 0 = Bank D outputs disabled/high impedance 1 = Bank D outputs active (default)
53	I <sub>REF</sub>	Input		External fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode.
54	V <sub>DDO_QE</sub>	Power		Bank E (HCSL) output supply pin. 3.3V supply.
55, 56	QE0, nQE0	Output		Bank E differential output pair. HCSL interface levels.
57, 58	QE1, nQE1	Output		Bank E differential output pair. HCSL interface levels.
60	OE_E	Input	Pullup	Active HIGH output enable for Bank E outputs. LVCMOS/LVTTL interface levels. 0 = Bank E outputs disabled/high impedance 1 = Bank E outputs enabled (default)
61, 62	FSEL_C0 FSEL_C1	Input	Pulldown	Selects the QCx, nQCx output frequency. LVCMOS/LVTTL interface levels. 00 = 100MHz (default) 01 = 125MHz 10 = 156.25MHz 11 = 312.5MHz
64	V <sub>DDA</sub>	Power		Analog supply pin.
65, 66	FSEL_D0 FSEL_D1	Input	Pulldown	Selects the QDx, nQDx output frequency. LVCMOS/LVTTL interface levels. 00 = 100MHz (default) 01 = 125MHz 10 = 156.25MHz 11 = 312.5MHz
68	nMR	Input	Pulldown	Active LOW Master Reset. LVCMOS/LVTTL interface levels. 0 = Reset. The internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. (default) 1 = Active. The internal dividers and the outputs are active.
69	V <sub>DDO_QG</sub>	Power		QG output supply pins (LVCMOS/LVTTL). 3.3V or 2.5V supply.
70	QG	Output		Bank G single-ended output. 3.3V or 2.5V LVCMOS/LVTTL interface levels.
72	OE_G	Input	Pullup	Active HIGH output enable for Bank G output. LVCMOS/LVTTL interface levels. 0 = Bank G outputs disabled/high impedance 1 = Bank G outputs enabled (default)
	EPAD			Connect to GND.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance	CLK, nCLK		2.5		pF
		Control Pins		6		pF
$R_{PULLUP}$	Input Pullup Resistor			50		k $\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor			50		k $\Omega$
$R_{OUT}$	Output Impedance	QF, QG, QREF[1:0] $V_{DDO\_QF} = V_{DDO\_QG} = V_{DDO\_QREF} = 3.465V$		15		$\Omega$
		QG, QREF[1:0] $V_{DDO\_QREF}, V_{DDO\_QG} = 2.625V$		19		$\Omega$

## Function Tables

**Table 3A. FSEL\_X Control Input Function Table**

Input	Output Frequency
FSEL_X[1:0]	Q[Ax:Ex], nQ[Ax:Ex]
00 (default)	100MHz
01	125MHz
10	156.25MHz
11	312.50MHz

NOTE: FSEL\_X denotes FSEL\_A, \_B, \_C, \_D, \_E.

NOTE: Any two outputs operated at the same frequency will be synchronous.

**Table 3B. PLL\_SEL Control Input Function Table**

Input	Operation
PLL_SEL	
0	PLL Bypass
1 (default)	PLL Mode

**Table 3C. REF\_SEL Control Input Function Table**

Input	Clock Source
REF_SEL	
0	CLK, nCLK
1 (default)	XTAL_IN, XTAL_OUT

**Table 3D. OE\_[A:E] Control Input Function Table**

Input	Outputs
OE_[A:E]	Q[Ax:Ex], nQ[Ax:Ex]
0	High-Impedance
1 (default)	Enabled

**Table 3E. OE\_G Control Input Function Table**

Input	Outputs
OE_G	QG
0	High-Impedance
1 (default)	Enabled

**Table 3F. OE\_REF Control Input Function Table**

Input	Output
OE_REF	QREF[1:0]
0	High-Impedance
1 (default)	Enabled

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	3.6V
Inputs, $V_I$ XTAL_IN Other Inputs	0V to 2V -0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO\_QX} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	26.6°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,**

$V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO\_Q[A:E]} = V_{DDO\_Q[F:G]} = V_{DDO\_QREF} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.225$	3.3	$V_{DD}$	V
$V_{DDO\_QX}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current			193	235	mA
$I_{DDA}$	Analog Supply Current			36	45	mA
$I_{DDO\_QX}$	Output Supply Current	No Load		24	30	mA

NOTE:  $V_{DDO\_QX}$  denotes  $V_{DDO\_Q[A:E]}$ ,  $V_{DDO\_Q[F:G]}$ ,  $V_{DDO\_QREF}$ .

NOTE:  $I_{DDO\_QX}$  denotes  $I_{DDO\_Q[A:E]} + I_{DDO\_Q[F:G]} + I_{DDO\_QREF}$ .

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO\_QG} = V_{DDO\_QREF} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.225$	3.3	$V_{DD}$	V
$V_{DDO\_QG}/$ $V_{DDO\_QREF}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current			193	235	mA
$I_{DDA}$	Analog Supply Current			36	45	mA
$I_{DDO\_QG} +$ $I_{DDO\_QREF}$	Output Supply Current	No Load		8	15	mA

**Table 4C. LVCMOS/LVTTL DC Characteristics,**
 $V_{DD} = V_{DDO\_Q[A:E]} = V_{DDO\_QF} = 3.3V \pm 5\%$ ;  $V_{DDO\_QG} = V_{DDO\_QREF} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage			2.2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage			-0.3		0.8	V
$I_{IH}$	Input High Current	nMR, FSEL_A[1:0], FSEL_B[1:0], FSEL_C[1:0], FSEL_D[1:0], FSEL_E[1:0]	$V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
		REF_SEL, PLL_SEL, OE_REF, OE_A, OE_B, OE_C, OE_D, OE_E, OE_G	$V_{DD} = V_{IN} = 3.465V$			10	$\mu A$
$I_{IL}$	Input Low Current	nMR, FSEL_A[1:0], FSEL_B[1:0], FSEL_C[1:0], FSEL_D[1:0], FSEL_E[1:0]	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-10			$\mu A$
		REF_SEL, PLL_SEL, OE_REF, OE_A, OE_B, OE_C, OE_D, OE_E, OE_G	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-150			$\mu A$
$V_{OH}$	Output High Voltage		$V_{DDO\_QF} = V_{DDO\_QG}$ , $V_{DDO\_QREF} = 3.465V$	2.6			V
			$V_{DDO\_QG}$ , $V_{DDO\_QREF} = 2.625V$	1.8			V
$V_{OL}$	Output Low Voltage		$V_{DDO\_QF} = V_{DDO\_QG}$ , $V_{DDO\_QREF} = 3.465V$ or $V_{DDO\_QG}$ , $V_{DDO\_QREF} = 2.625V$			0.6	V

**Table 4D. Differential DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK, nCLK	$V_{DD} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	CLK	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-5			$\mu A$
		nCLK	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-150			$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2			0.5		$V_{DD} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .

**Table 5. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Load Capacitance (CL)			12		pF
Shunt Capacitance				7	pF

**Table 6. Input Frequency Characteristics,**
 $V_{DD} = V_{DDO\_Q[A:E]} = V_{DDO\_QF} = 3.3V \pm 5\%$ ;  $V_{DDO\_QG} = V_{DDO\_QREF} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$F_{IN}$	Input Frequency	CLK, nCLK			25		MHz
		XTAL_IN, XTAL_OUT			25		MHz

## AC Electrical Characteristics

**Table 7A. PCI Express Jitter Specifications,**  $V_{DD} = V_{DDO\_Q[A:E]} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
$t_j$ (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	$f = 100MHz$ , 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		6.97	11.18	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	$f = 100MHz$ , 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2)		0.70	1.84	3.10	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	$f = 100MHz$ , 25MHz Crystal Input Low Band: 10kHz - 1.5MHz		0.03	0.07	3.0	ps
$t_{REFCLK\_RMS}$ (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	$f = 100MHz$ , 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.16	0.49	0.8	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note* section in the datasheet.

NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of  $10^6$  clock periods.

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for  $t_{REFCLK\_HF\_RMS}$  (High Band) and 3.0ps RMS for  $t_{REFCLK\_LF\_RMS}$  (Low Band).

NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.



**Table 7B. HCSL AC Characteristics,**
 $V_{DD} = V_{DDO\_Q[A:E]} = V_{DDO\_QF} = 3.3V \pm 5\%$ ;  $V_{DDO\_QG} = V_{DDO\_QREF} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	Q[A:E], nQ[A:E]	FSEL_x[1:0] = 00	100		MHz
			FSEL_x[1:0] = 01	125		MHz
			FSEL_x[1:0] = 10	156.25		MHz
			FSEL_x[1:0] = 11	312.5		MHz
$V_{RB}$	Ring-Back Voltage Margin; NOTE 1, 2	Q[A:E], nQ[A:E]	-100		100	mV
$t_{STABLE}$	Time before $V_{RB}$ is allowed; NOTE 1, 2	Q[A:E], nQ[A:E]	500			ps
$V_{MAX}$	Absolute Max Output Voltage; NOTE 3, 4	Q[A:E], nQ[A:E]			1150	mV
$V_{MIN}$	Absolute Min Output Voltage; NOTE 3, 5	Q[A:E], nQ[A:E]	-300			mV
$V_{CROSS}$	Absolute Crossing Voltage; NOTE 3, 6, 7	Q[A:E], nQ[A:E]	175		550	mV
$\Delta V_{CROSS}$	Total Variation of $V_{CROSS}$ over All Edges; NOTE 3, 6, 8	Q[A:E], nQ[A:E]			140	mV
$t_{SLEW+}$	Rising Edge Rate; NOTE 1, 9	Q[A:E], nQ[A:E]	0.6		4.0	V/ns
$t_{SLEW-}$	Falling Edge Rate; NOTE 1, 9	Q[A:E], nQ[A:E]	0.6		4.0	V/ns
odc	Output Duty Cycle	Q[A:E], nQ[A:E]	48	50	52	%
$t_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 10	Q[A:E], nQ[A:E]	100MHz, Integration Range: (12kHz to 20MHz)	0.32	0.45	ps
			125MHz, Integration Range: (12kHz to 20MHz)	0.31	0.45	ps
			156.25MHz, Integration Range: (12kHz to 20MHz)	0.30	0.45	ps
			312.5MHz, Integration Range: (12kHz to 20MHz)	0.29	0.45	ps
$t_{jit}(R_J)$	Random Jitter, RMS; NOTE 11	Q[A:E], nQ[A:E] = 125MHz, 25MHz XTAL, PLL Mode		2	5	ps
$t_{jit}(D_J)$	Deterministic Jitter, Pk-to-Pk; NOTE 11			1	3	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at  $f_{OUT}$  and in PLL mode unless noted otherwise.

NOTE: Refer to applications section for information on peak-to-peak jitter calculations.

NOTE 1: Measurement taken from differential waveform.

NOTE 2:  $t_{STABLE}$  is the time the differential clock must maintain a minimum  $\pm 150mV$  differential voltage after rising/falling edges before it is allowed to drop back into the  $V_{RB} \pm 100mV$  range. See Parameter Measurement Information Section.

NOTE 3: Measurement taken from single-ended waveform.

NOTE 4: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 5: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 6: Measured at the crossing point where the instantaneous voltage value of the rising edge of Q[Ax:Ex] equals the falling edge of nQ[Ax:Ex].

NOTE 7: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

Notes continued on next page.

NOTE 8: Defined as the total variation of all crossing voltages of rising Q[Ax:Ex] and falling nQ[Ax:Ex]. This is the maximum allowed variance in V<sub>CROSS</sub> for any particular system.

NOTE 9: Measured from -150mV to +150mV on the differential waveform (derived from Q[Ax:Ex] minus nQ[Ax:Ex]). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

NOTE 10: Measurements taken with 25MHz XTAL as input source and spur off.

NOTE 11: Measurements taken with Wavecrest SIA-3000 Analyzer.

**Table 7C. LVCMOS AC Characteristics,**

V<sub>DD</sub> = V<sub>DDO\_Q[A:E]</sub> = V<sub>DDO\_QF</sub> = 3.3V ± 5%; V<sub>DDO\_QG</sub> = V<sub>DDO\_QREF</sub> = 3.3V ± 5% or 2.5V ± 5%, T<sub>A</sub> = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f <sub>OUT</sub>	Output Frequency	QF		50		MHz
		QG		125		MHz
		QREF[1:0]		25		MHz
tr/tf	Output Rise/Fall Time	QF, QG, QREF[1:0]	20% to 80%	180	700	ps
odc	Output Duty Cycle	QF, QG, QREF[1:0]	47	50	53	%
t <sub>jitter</sub> (Ø)	RMS Phase Jitter, (Random); NOTE 1	QF	50MHz, Integration Range: (12kHz to 20MHz)	0.35	0.45	ps
		QG	125MHz, Integration Range: (12kHz to 20MHz)	0.30	0.40	ps
		QREF[1:0]	25MHz, Integration Range: (12kHz to 5MHz)	0.32	0.40	ps
t <sub>jitter</sub> (R <sub>J</sub> )	Random Jitter, RMS; NOTE 2	QF, QG, QREF[1:0]	Q[A:E], nQ[A:E] = 125MHz, 25MHz XTAL, PLL Mode	2	5	ps
t <sub>jitter</sub> (D <sub>J</sub> )	Deterministic Jitter, Pk-to-Pk; NOTE 2	QF	Q[A:E], nQ[A:E] = 125MHz, 25MHz XTAL, PLL Mode	3	25	ps
		QG		1	5	ps
		QREF[1:0]		1	3	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at f<sub>OUT</sub> and in PLL mode unless noted otherwise.

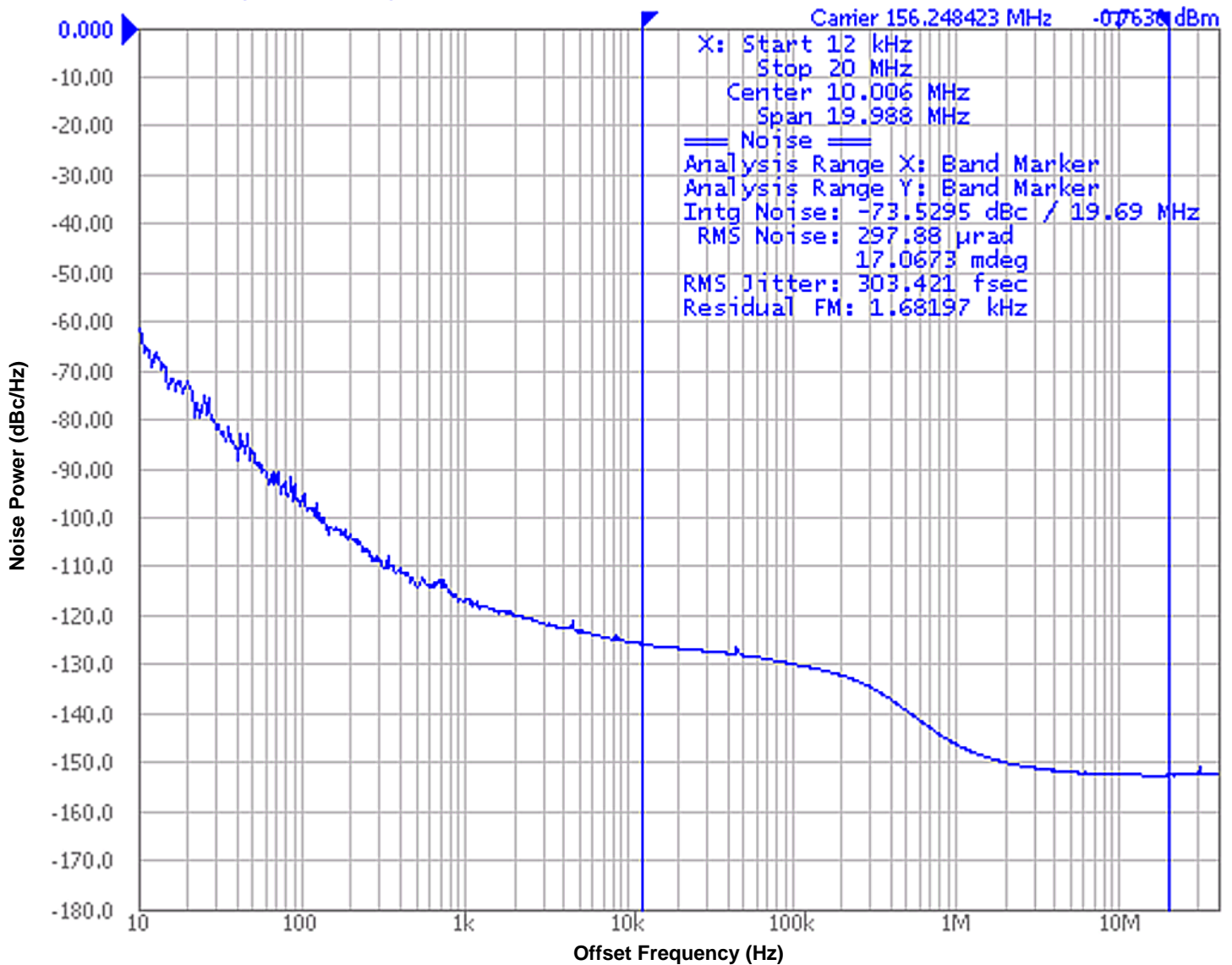
NOTE: Refer to applications section for information on peak-to-peak jitter calculations.

NOTE 1: Measurements taken with 25MHz XTAL as input source and spur off.

NOTE 2: Measurements taken with Wavecrest SIA-3000 Analyzer. QG characterized with QREF[1:0] disabled.

## Typical Phase Noise at 156.25MHz

►Phase Noise 10.00dB/ Ref 0.000dBc/Hz



Schematic diagram of a differential-mode input stage. The input stage is a differential pair with a tail resistor of  $10\Omega$  connected to  $V_{DDA}$ . The inputs are  $V_{DD}$ ,  $V_{DDO\_QG}$ , and  $V_{DDO\_QREF}$ . The output is  $Qx$ , which is connected to a  $50\Omega$  load resistor. The output is measured by a SCOPE. The input voltages are  $2.05V \pm 5\%$ ,  $1.25V \pm 5\%$ , and  $-1.25V \pm 5\%$ .

The diagram illustrates the internal structure of the HCSL output stage. It features a differential pair of NMOS and PMOS transistors. The PMOS gates are connected to a 3.3V±5% supply through a 5Ω resistor. The NMOS gates are connected to a 0V supply through a 475Ω resistor. The PMOS sources are connected to a 3.3V±5% supply through a 33Ω resistor. The NMOS sources are connected to a 0V supply through a 33Ω resistor. The PMOS drains are connected to a 50Ω load resistor, which is in series with a 49.9Ω resistor connected to ground. The NMOS drains are connected to a 50Ω load resistor, which is in series with a 49.9Ω resistor connected to ground. The output nodes are labeled Qx and nQx, each with a 2pF load capacitor connected to ground. The HCSL block is labeled with V<sub>DD</sub>, V<sub>DDO\_Q[A:E]</sub>, V<sub>DDA</sub>, and IREF pins.

This load condition is used for  $t_{\text{jit}}$  and  $\text{odc}$  measurements.

The diagram shows a timing sequence for a crossbar array. It features three horizontal dashed lines representing voltage levels:  $V_{DD}$  at the top,  $GND$  at the bottom, and an intermediate level. Two signals are plotted:  $nCLK$  and  $CLK$ . The  $nCLK$  signal is a square wave that transitions from low to high at the first 'Cross Point' and from high to low at the second 'Cross Point'. The  $CLK$  signal is a square wave that transitions from high to low at the first 'Cross Point' and from low to high at the second 'Cross Point'. The voltage swing of the  $CLK$  signal is labeled  $V_{PP}$ , and the voltage swing of the  $nCLK$  signal is labeled  $V_{CMR}$ . The two signal transitions are labeled 'Cross Points'.

Phase Noise Plot

Noise Power

Offset Frequency

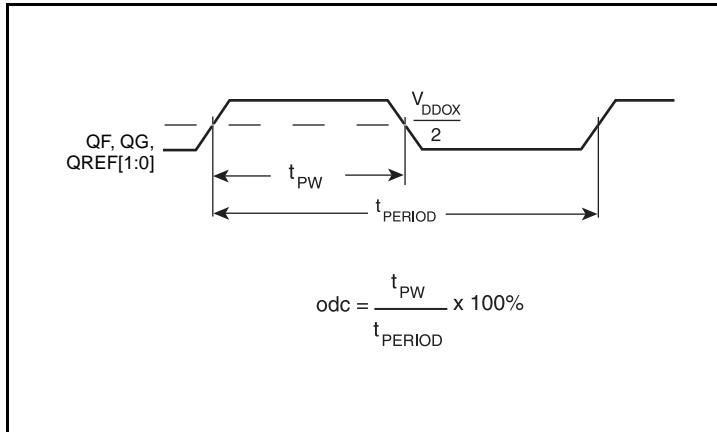
$f_1$   $f_2$

**RMS Phase Jitter =**

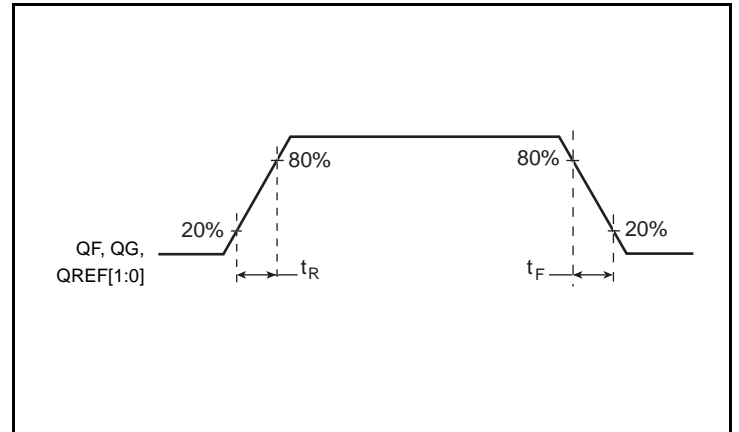
$$\frac{1}{\sqrt{2} * \pi * f} * \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}$$

Revision C, November 2, 2016

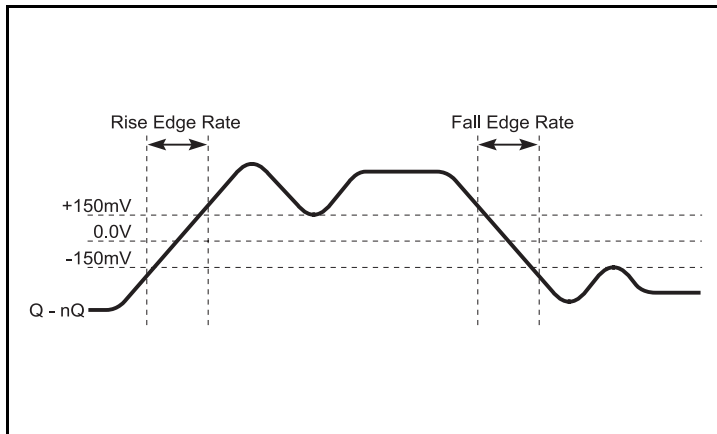
## Parameter Measurement Information, continued



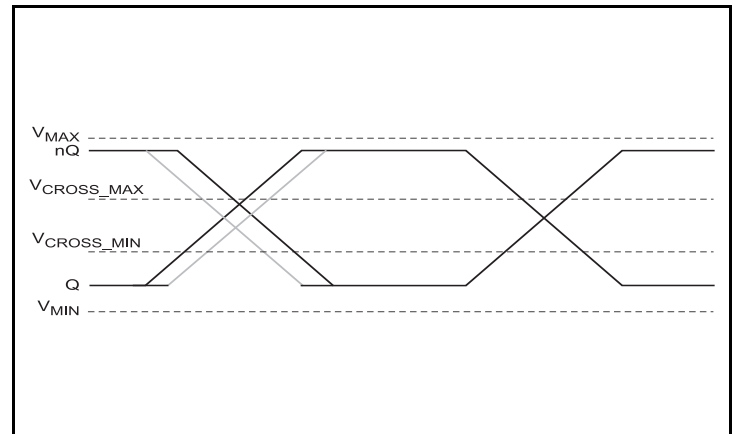
**LVCMOS Output Duty Cycle/Pulse Width**



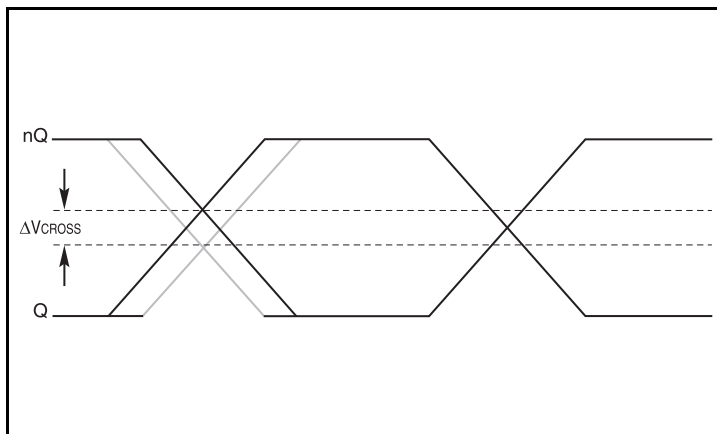
**LVCMOS Output Rise/Fall Time**



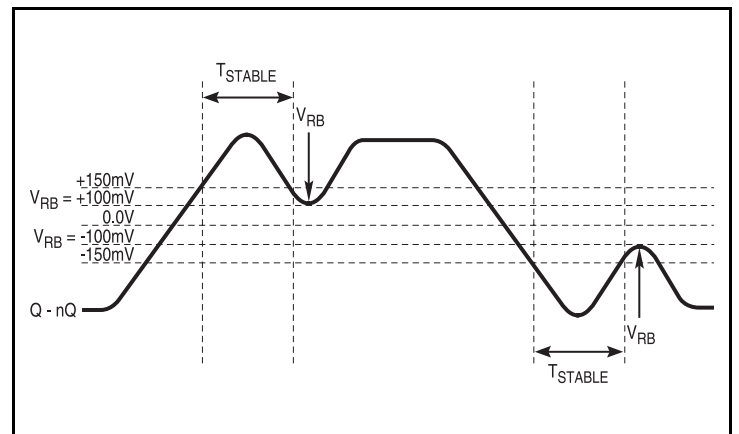
**Differential Measurement Points for Rise/Fall Time Edge Rate**



**Single-ended Measurement Points for Absolute Cross Point/Swing**

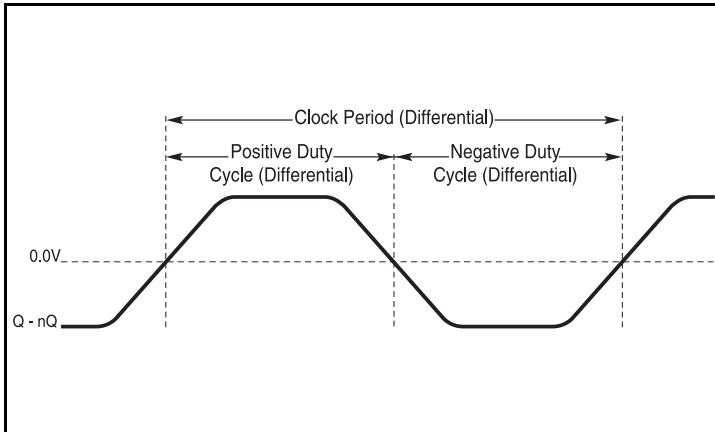


**Single-ended Measurement Points for Delta Cross Point**



**Differential Measurement Points for Ringback**

## Parameter Measurement Information, continued



**Differential Measurement Points for Duty Cycle/Period**

## Applications Information

### Peak-to-Peak Jitter Calculations

A standard deviation of a statistical population or data set is the square root of its variance. A standard deviation is used to calculate the probability of an anomaly or to predict a failure. Many times, the term "root mean square" (RMS) is used synonymously for standard deviation. This is accurate when referring to the square root of the mean squared deviation of a signal from a given baseline and when the data set contains a Gaussian distribution with no deterministic components. A low standard deviation indicates that the data set is close to the mean with little variation. A large standard deviation indicates that the data set is spread out and has a large variation from the mean.

A standard deviation is required when calculating peak-to-peak jitter. Since true peak-to-peak jitter is random and unbounded, it is important to always associate a bit error ratio (BER) when specifying a peak-to-peak jitter limit. Without it, the specification does not have a boundary and will continue get larger with sample size. Given that a BER is application specific, many frequency timing devices specify jitter as an RMS. This allows the peak-to-peak jitter to be calculated for the specific application and BER requirement. Because a standard deviation is the variation from the *mean* of the data set, it is important to always calculate the peak-to-peak jitter using the typical RMS value.

Table 8 shows the BER with its appropriate RMS Multiplier. There are two columns for the RMS multiplier, one should be used if your signal is data and the other should be used if the signal is a repetitive clock signal. The difference between the two is the data transition density (DTD). The DTD is the number of rising or falling transitions divided by the total number of bits. For a clock signal, they are equal, hence the DTD is 1. For Data, on average, most common encoding standards have a 0.5 DTD.

**Table 8. BER Table**

BER	RMS Multiplier Data, "DTD = 0.5"	RMS Multiplier Clock, "DTD = 1"
$10^{-3}$	6.180	6.582
$10^{-4}$	7.438	7.782
$10^{-5}$	8.530	8.834
$10^{-6}$	9.507	9.784
$10^{-7}$	10.399	10.654
$10^{-8}$	11.224	11.462
$10^{-9}$	11.996	12.218
$10^{-10}$	12.723	12.934
$10^{-11}$	13.412	13.614
$10^{-12}$	14.069	14.260
$10^{-13}$	14.698	14.882
$10^{-14}$	15.301	15.478
$10^{-15}$	15.883	16.028

Once the BER is chosen, there are two circumstances to consider. Is the data set purely Gaussian or does it contains any deterministic component? If it is Gaussian, then the peak to peak jitter can be calculated by simply multiplying the RMS multiplier with the typical RMS specification. For example, if a  $10^{-12}$  BER is required for a clock signal, multiply 14.260 times the typical jitter specification.

$$\text{Jitter (peak-to-peak)} = \text{RMS Multiplier} * \text{RMS (typical)}$$

If the datasheet contains deterministic components, then the random jitter ( $R_J$ ) and deterministic jitter ( $D_J$ ) must be separated and analyzed separately.  $R_J$ , also known as Gaussian jitter, is not bounded and the peak-to-peak will continue to get larger as the sample size increases. Alternatively, peak-to-peak value of  $D_J$  is bounded and can easily be observed and predicted. Therefore, the peak to peak jitter for the random component must be added to the deterministic component. This is called total jitter ( $T_J$ ).

$$\text{Total Jitter (peak-to-peak)} = [\text{RMS Multiplier} * \text{Random Jitter (} R_J \text{)}] + \text{Deterministic Jitter (} D_J \text{)}$$

The *total jitter equation* is not specific to one type of jitter classification. It can be used to calculate BER on various types of RMS jitter. It is important that the user understands their jitter requirement to ensure they are calculating the correct BER for their jitter requirement.

NOTE: Use  $R_J$  and  $D_J$  values from AC Characteristics Tables 7B and 7C to calculate  $T_J$ .

## Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{DD}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock is driven from a single-ended 2.5V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25V, the R1 and R2 values should be adjusted to set the  $V_1$  at 1.25V. The values below are for when both the single ended swing and  $V_{DD}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should

equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{DD} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

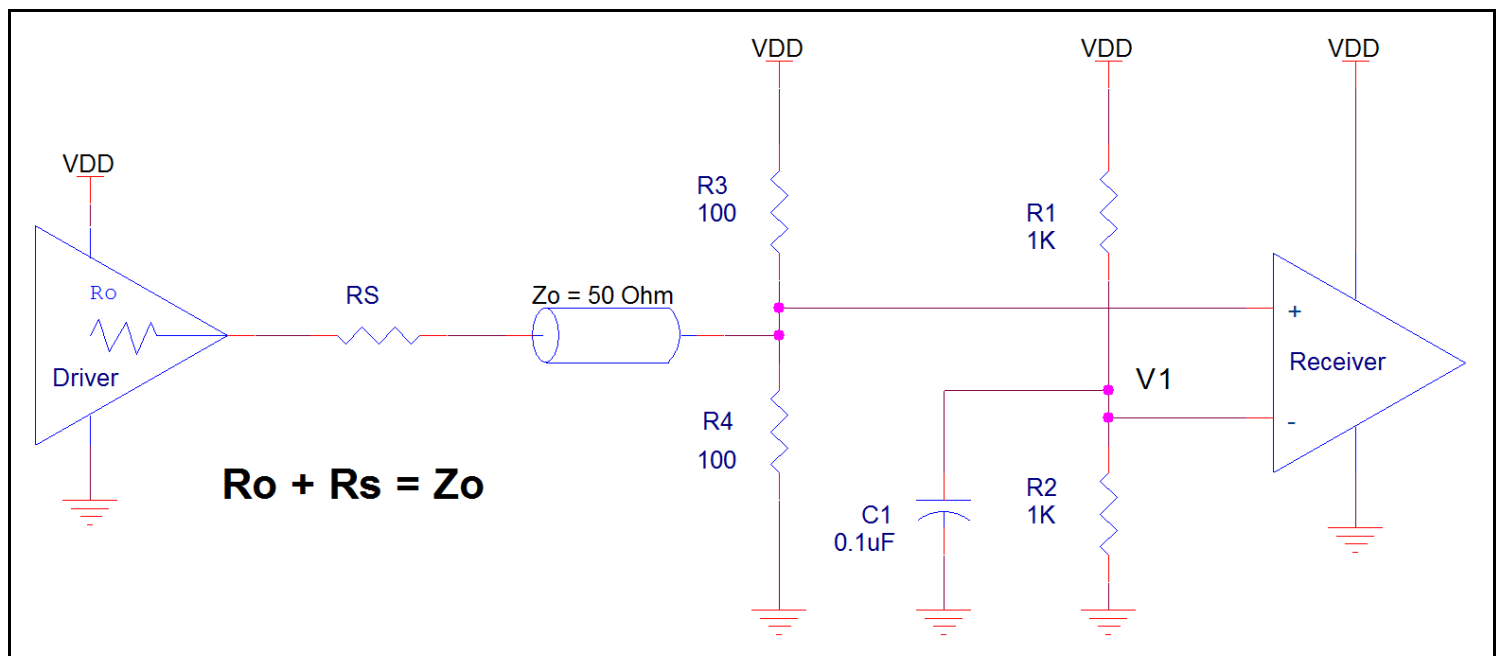


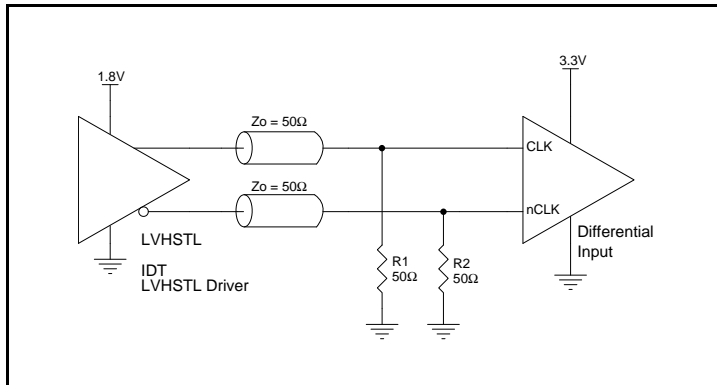
Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



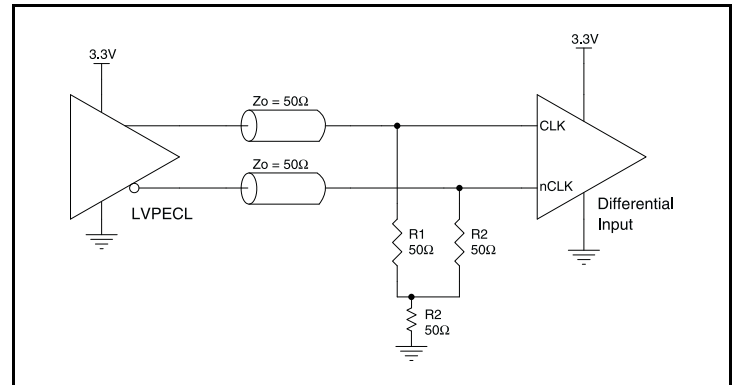
## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult

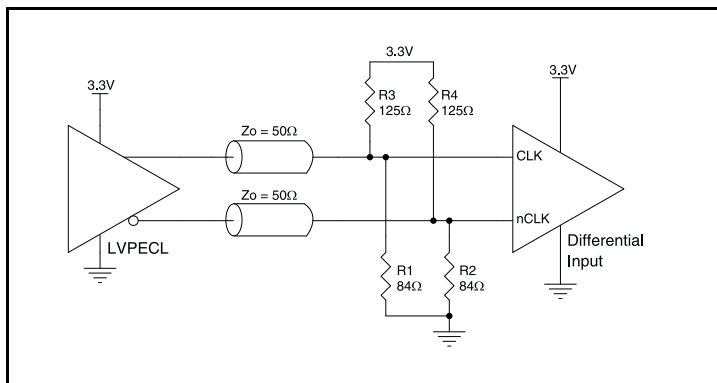
with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



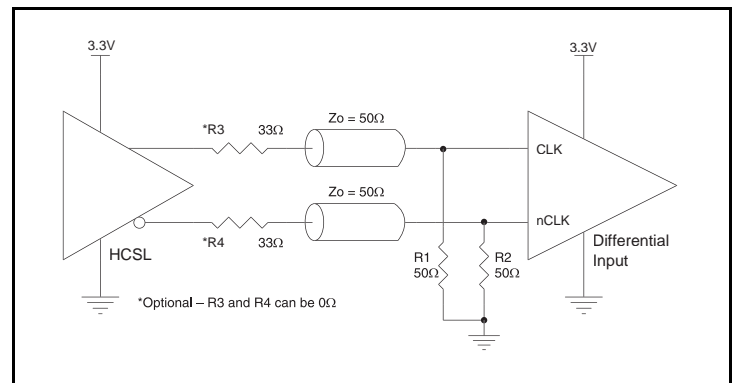
**Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**



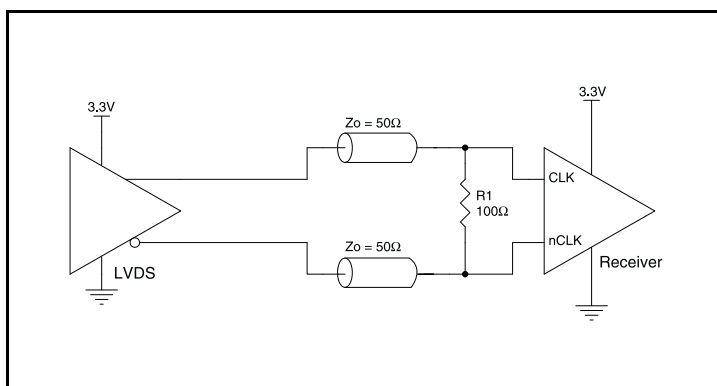
**Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 2D. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

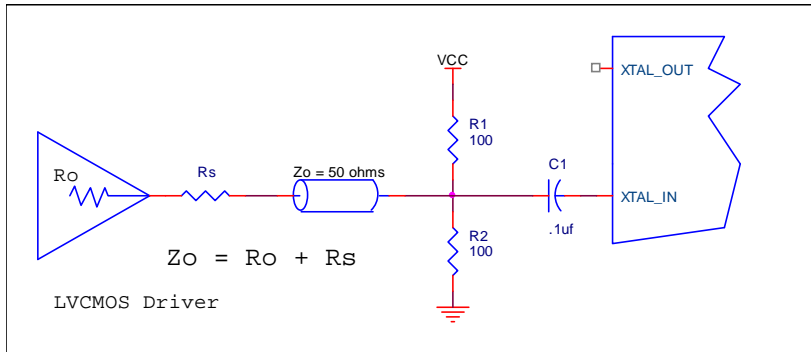


**Figure 2E. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

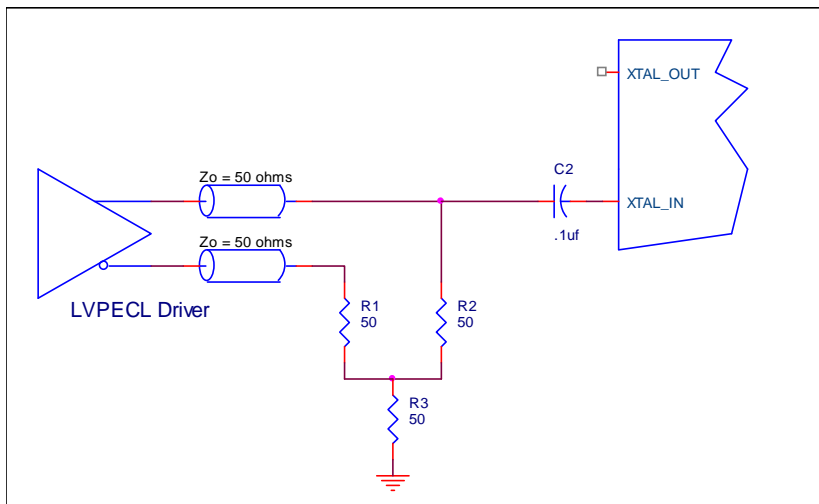
## Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.



**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**

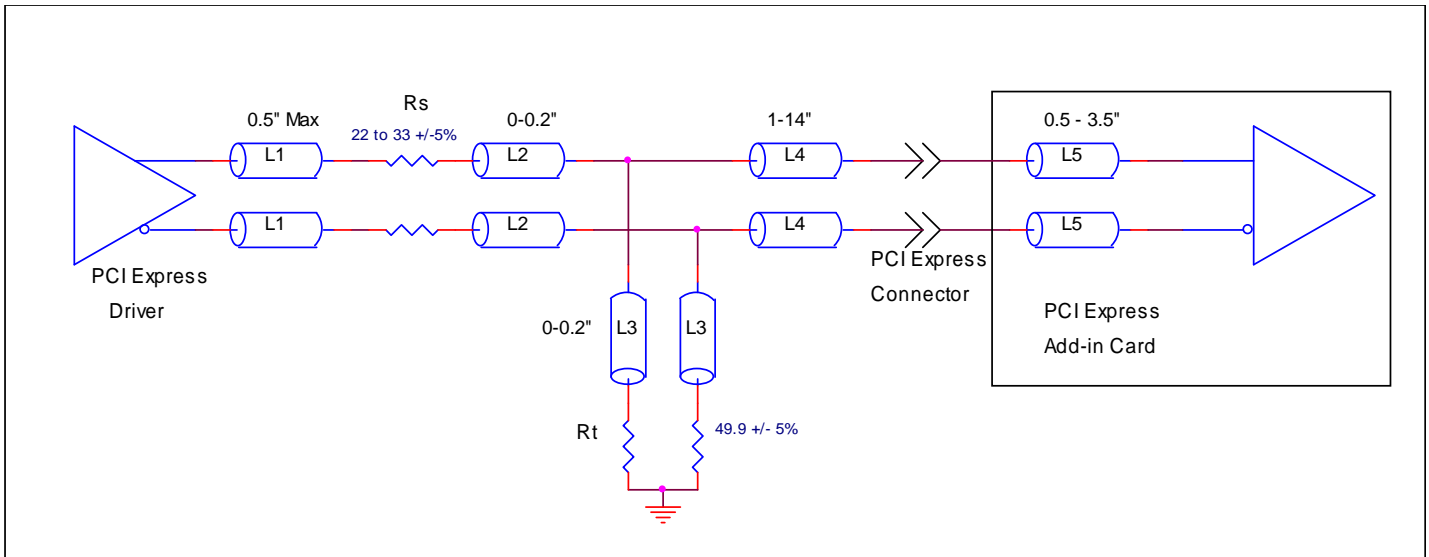


**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Recommended Termination

Figure 4A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output

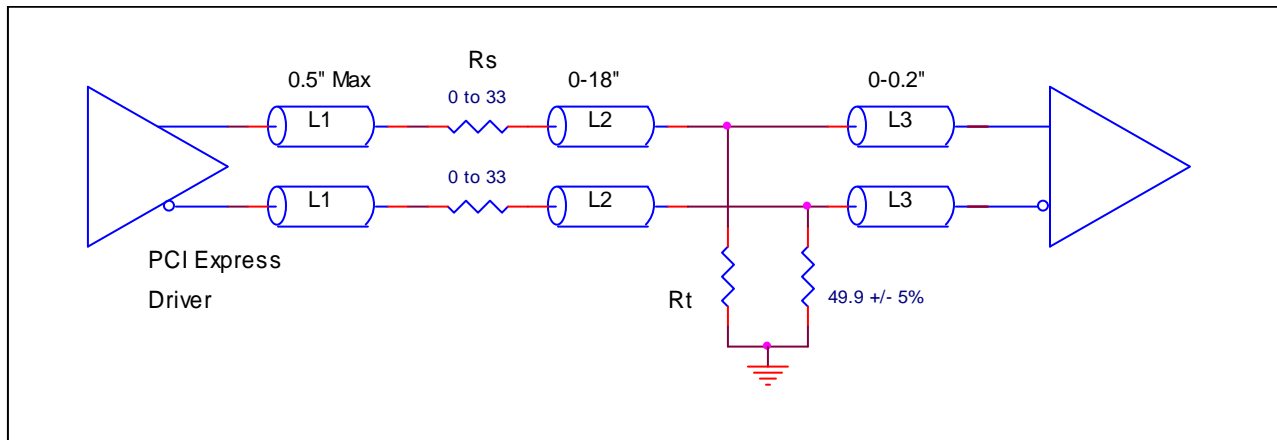
types. All traces should be 50Ω impedance single-ended or 100Ω differential.



**Figure 4A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)**

Figure 4B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.



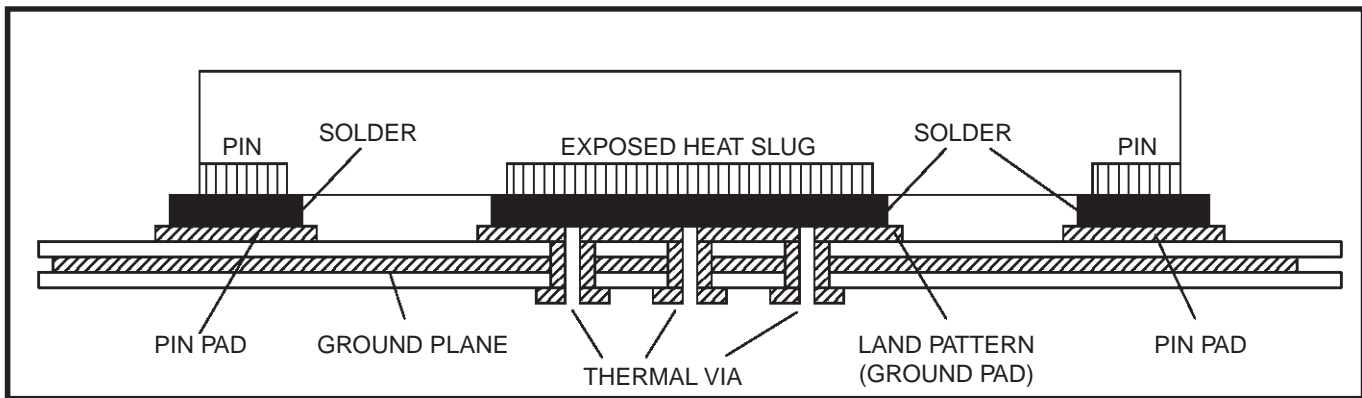
**Figure 4B. Recommended Termination (where a point-to-point connection can be used)**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

#### CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from CLK to ground.

### Outputs:

#### LVC MOS Outputs

All unused LVC MOS outputs can be left floating. There should be no trace attached.

#### Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

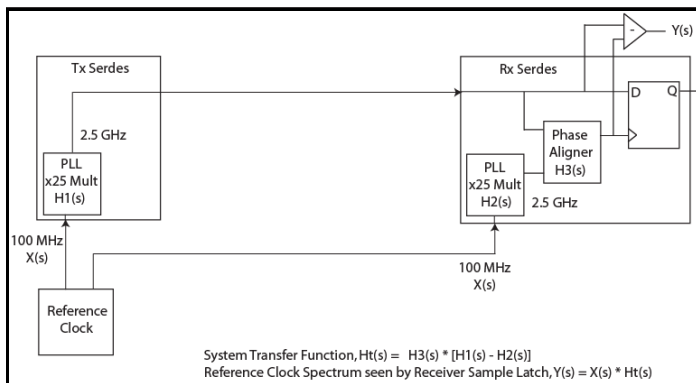
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$H_t(s) = H_3(s) \times [H_1(s) - H_2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum  $X(s)$  and is:

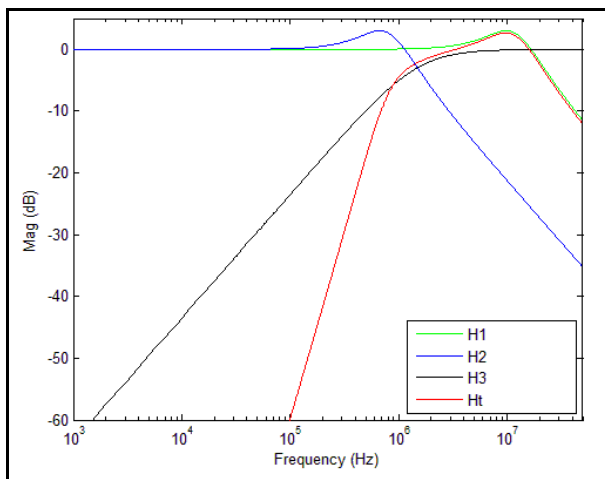
$$Y(s) = X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on  $X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$ .



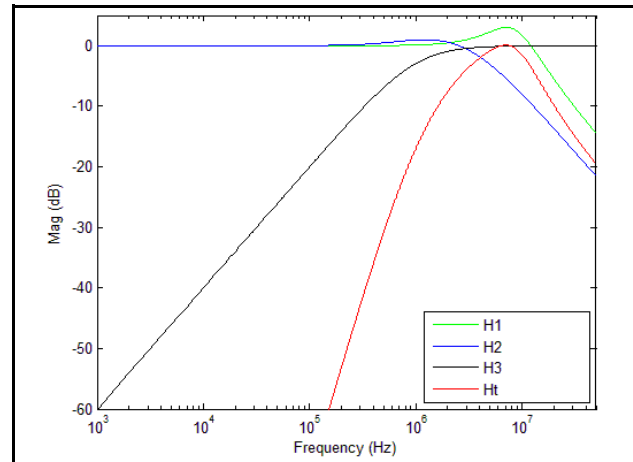
**PCI Express Common Clock Architecture**

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

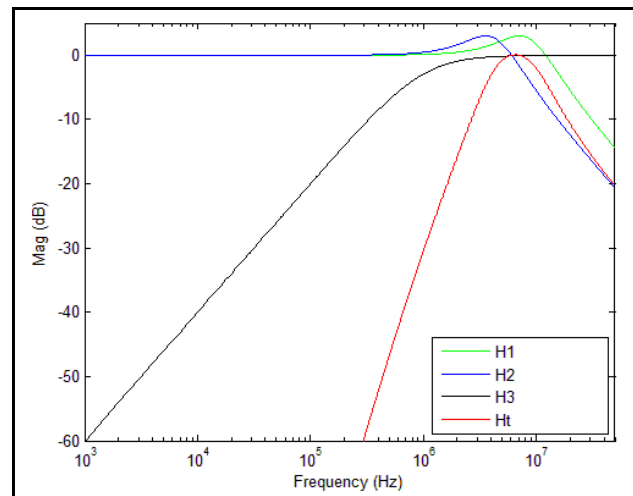


**PCI Gen 1 Magnitude of Transfer Function**

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function  $H_t$ .

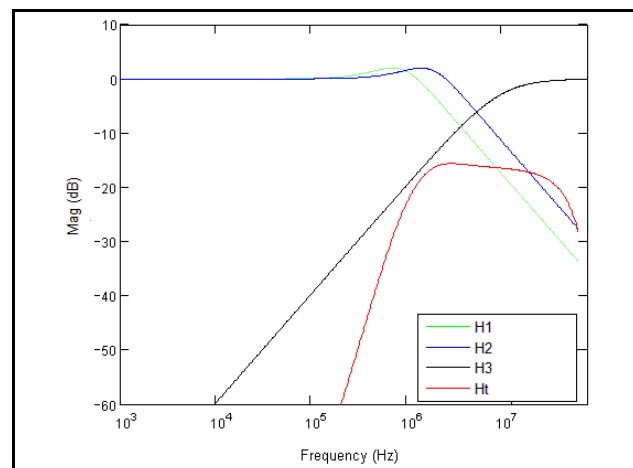


**PCIe Gen 2A Magnitude of Transfer Function**



**PCIe Gen 2B Magnitude of Transfer Function**

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



**PCIe Gen 3 Magnitude of Transfer Function**

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.

## Schematic Example

Figure 6 (next page) shows an example of 8V41N012 application schematic. In this example, the device is operated at  $V_{DD} = V_{DDA} = V_{DDO\_Qx} = 3.3V$ . The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

A 12pF parallel resonant 25MHz crystal is used. For this device, the crystal load capacitors are required for proper operation. The load capacitance,  $C1 = C2 = 2pF$ , are recommended for frequency accuracy. Depending on the variation of the parasitic stray capacity of the printed circuit board traces between the crystal and the Xtal\_In and Xtal\_Out pins, the values of C1 and C2 might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used, but this will require adjusting C1 and C2. When designing the circuit board, return the capacitors to ground through a single point contact close to the package. Two Fox crystal options are shown in the schematic for design flexibility.

The ePAD provides a low thermal impedance connection between the internal device and the PCB. It also provides an electrical connection to the die and must be connected to ground.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8V41N012 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1μF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

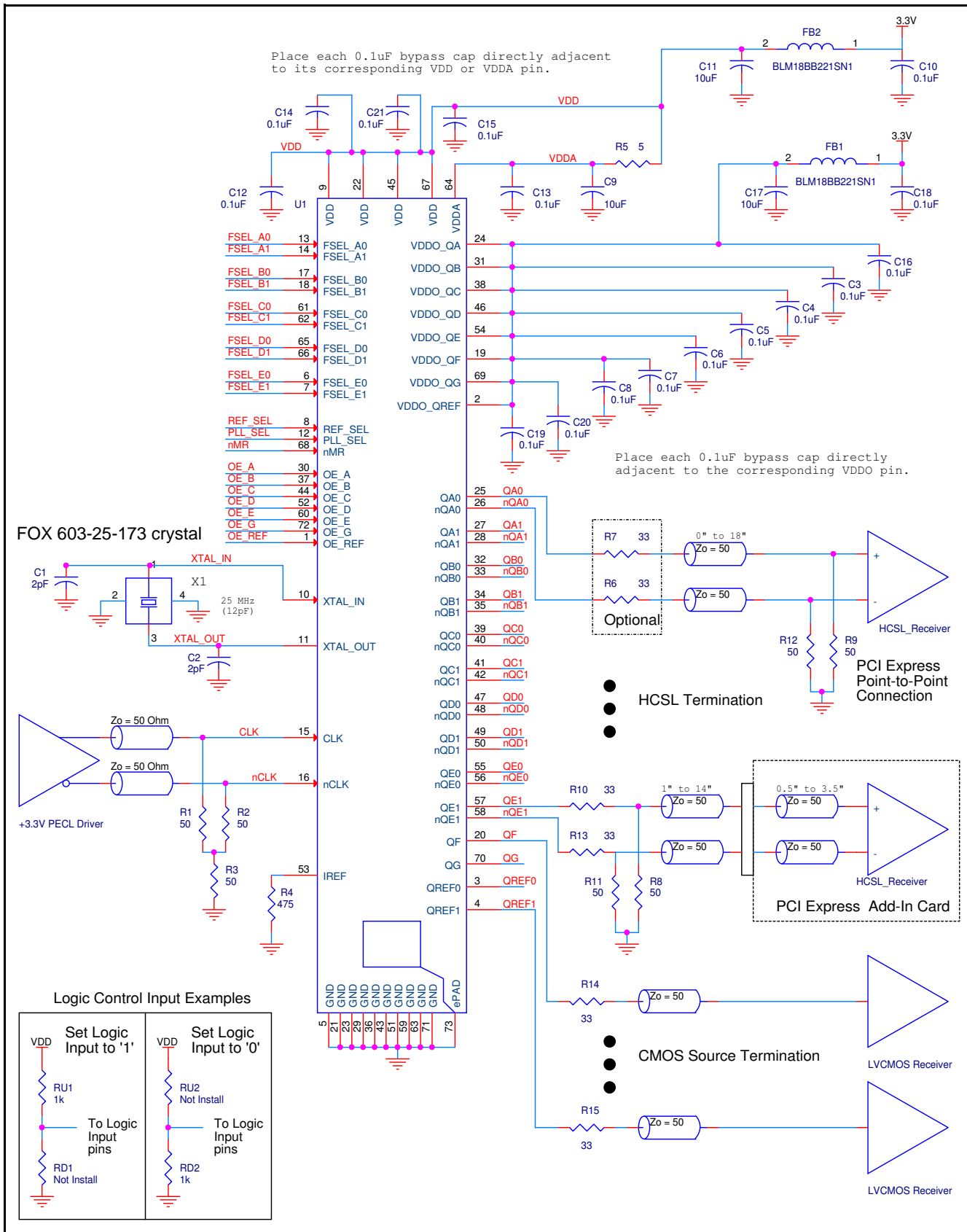


Figure 6. 8V41N012 Schematic Example

## Power Considerations

This section provides information on power dissipation and junction temperature for the 8V41N012. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8V41N012 is the sum of the core power plus the analog power plus the power dissipated due to loading. The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD} + I_{DDA}) = 3.465V * (235mA + 45mA) = \mathbf{970.2mW}$
- Power (HCSL)<sub>MAX</sub> =  $(3.465V - 17mA * 50) 17mA = \mathbf{44.5mW}$  per output
- Total Power (HCSL)<sub>MAX</sub> =  $44.5mW * 10 = \mathbf{445mW}$

### LVC MOS Driver Power Dissipation

- Output Impedance  $R_{OUT}$  Power Dissipation due to Loading  $50\Omega$  to  $V_{DDO\_Qx} / 2$   
Output Current  $I_{OUT} = V_{DD\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 15\Omega)] = \mathbf{26.65mA}$
- Power Dissipation on the  $R_{OUT}$  per LVC MOS output  
Power (LVC MOS) =  $R_{OUT} * (I_{OUT})^2 = 15\Omega * (26.65mA)^2 = \mathbf{10.65mW}$  per output
- Total Power Dissipation on the  $R_{OUT}$   
Total Power ( $R_{OUT}$ ) =  $10.65mW * 4 = \mathbf{42.6mW}$
- Total Power Dissipation
- Total Power**  
= Power (core) + Total Power (HCSL) + Total Power ( $R_{OUT}$ )  
=  $970.2mW + 445mW + 42.6mW$   
=  $\mathbf{1457.8mW}$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is  $125^\circ\text{C}$ . Limiting the internal transistor junction temperature,  $T_j$ , to  $125^\circ\text{C}$  ensures that the bond wire and bond pad temperature remains below  $125^\circ\text{C}$ .

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is  $26.6^\circ\text{C/W}$  per Table 9 below.

Therefore,  $T_j$  for an ambient temperature of  $85^\circ\text{C}$  with all outputs switching is:

$$85^\circ\text{C} + 1.458W * 26.6^\circ\text{C/W} = 123.8^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 9. Thermal Resistance  $\theta_{JA}$  for 72 Lead VFQFN, Forced Convection**

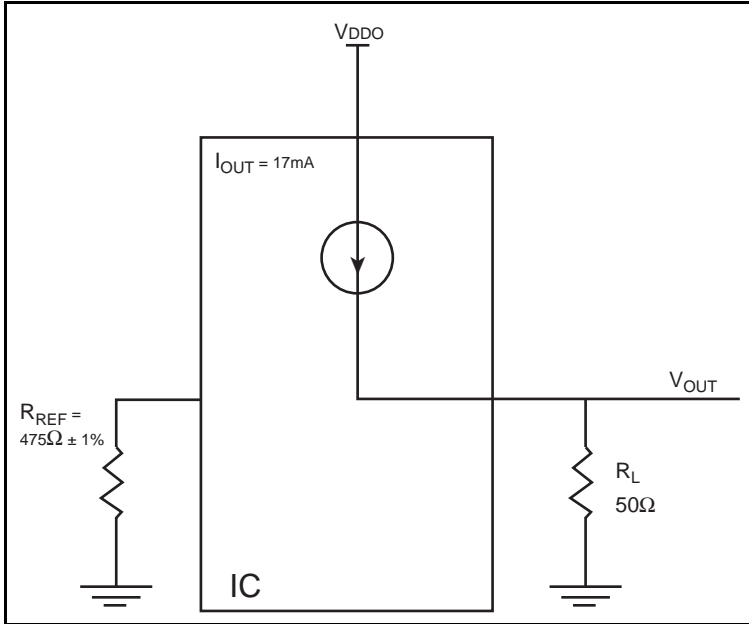
$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	$26.6^\circ\text{C/W}$	$20^\circ\text{C/W}$	$17.9^\circ\text{C/W}$



### 3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 7*.



**Figure 7. HCSL Driver Circuit and Termination**

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when  $V_{DD\_MAX}$ .

$$\text{Power} = (V_{DD\_MAX} - V_{OUT}) * I_{OUT}$$

$$\text{since } V_{OUT} = I_{OUT} * R_L$$

$$\text{Power} = (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$$

$$= (3.465V - 17mA * 50\Omega) * 17mA$$

Total Power Dissipation per output pair = **44.5mW**

## Reliability Information

**Table 10.  $\theta_{JA}$  vs. Air Flow Table for a 72 Lead VFQFN**

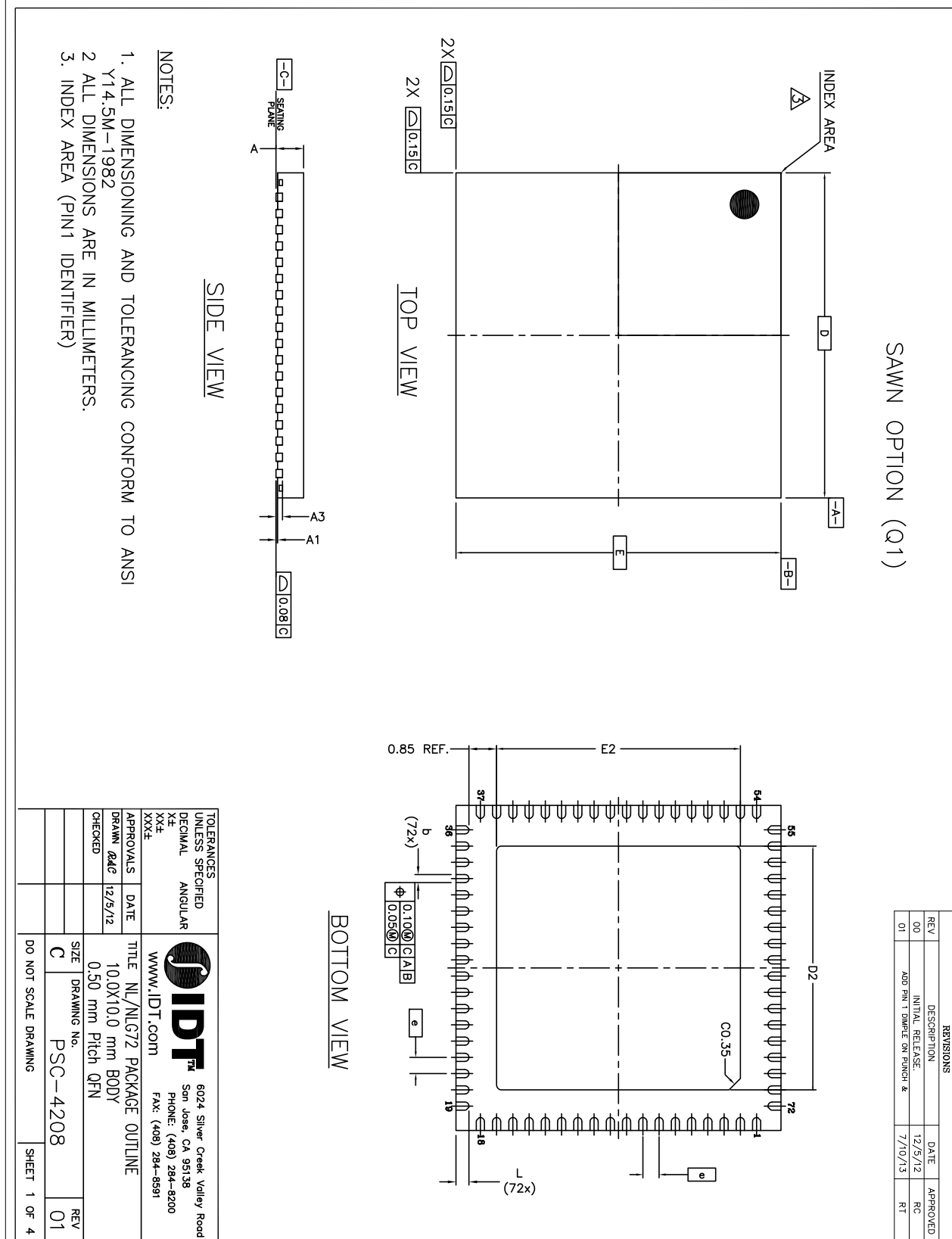
$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	26.6°C/W	20°C/W	17.9°C/W

## Transistor Count

The transistor count for 8V41N012 is: 175,936

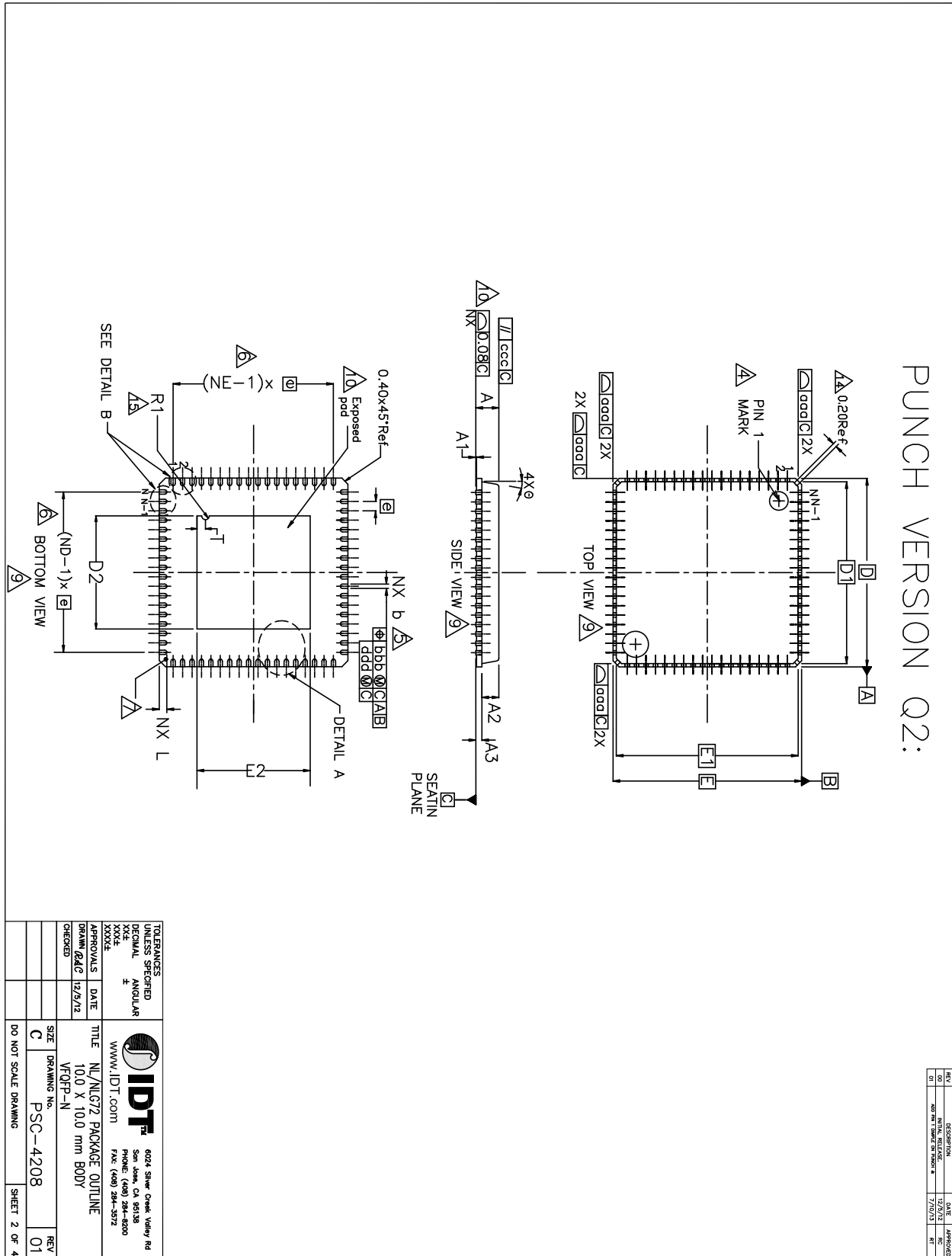
# Package Outline and Package Dimensions

## Package Outline - 72 Lead VFQFN



# Package Outline and Package Dimensions

## Package Outline - 72 Lead VFQFN



### Package Outline - 72 Lead VFQFN

Package Outline and Package Dimensions

Package Outline - 72 Lead VFQFN

SAW VERSION:

DIMENSION			N <sub>O</sub> 1 <sub>E</sub>
S <sub>Y</sub>	MIN.	NOM.	MAX.
L	SEE EPAD OPTION		
D2	SEE EPAD OPTION		
E2	SEE EPAD OPTION		
K	0.20	—	—
N	—	72	6
Nd	—	18	6
Ne	—	18	6

EPAD OPTION:

P1			P2			P3			
S <sub>Y</sub>	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
L	7.40	7.50	7.60	5.90	6.00	6.10	5.80	5.90	6.00
D2	7.40	7.50	7.60	5.90	6.00	6.10	5.80	5.90	6.00

LEAD OPTION

Z1			Z2			
S <sub>Y</sub>	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
L	0.45	0.50	0.55	0.30	0.40	050

TOLERANCE OF FORM & POSITION

pitch		
SYMBOL	0.40mm	0.50mm
aaa	0.10	0.15
bbb	0.07	0.10
ccc	0.10	0.10
ddd	0.05	0.05
NOTES	1,2	

COMMON DIMENSIONS

DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3 REF	—	0.20 ref	—
Ø	0	—	14
T ref.	—	0.45	—
R1	—	0.20	—
R ref. b min/2	—	—	—
NOTES	1,2		
b	0.18	0.25	0.30
Ø	0.50 BSC		
D	10.00 BSC		
E	10.00 BSC		

PUNCH VERSION

DIMENSION			N <sub>O</sub> 1 <sub>E</sub>
S <sub>Y</sub>	MIN.	NOM.	MAX.
L	SEE EPAD OPTION		
D2	SEE EPAD OPTION		
E2	SEE EPAD OPTION		
D1	9.75 BSC		
E1	9.75 BSC		
N	—	72	3
Nd	—	18	6
Ne	—	18	6
A2	0	0.65	1.00

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.

2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3. N IS THE TOTAL NUMBER OF TERMINALS.

Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &

Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUB. 95 SEC. 4.3 SP-002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.

5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.

6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	12/27/12	RC
01	ADD PWT 100µE FOR MOUNT *	7/30/15	RT

TOLERANCES UNLESS SPECIFIED

DECIMAL	ANGULAR
0.004	0.004
0.005	0.005
0.006	0.006
0.008	0.008
0.010	0.010
0.015	0.015
0.020	0.020
0.025	0.025
0.030	0.030
0.040	0.040
0.050	0.050
0.060	0.060
0.070	0.070
0.080	0.080
0.090	0.090
0.100	0.100
0.120	0.120
0.150	0.150
0.200	0.200
0.250	0.250
0.300	0.300
0.375	0.375
0.500	0.500
0.625	0.625
0.750	0.750
1.000	1.000
1.270	1.270
1.500	1.500
1.778	1.778
2.000	2.000
2.540	2.540
3.175	3.175
3.540	3.540
4.000	4.000
5.080	5.080
6.350	6.350
7.620	7.620
10.160	10.160
12.700	12.700
15.240	15.240
17.780	17.780
20.320	20.320
25.400	25.400
30.480	30.480
35.560	35.560
40.640	40.640
45.720	45.720
50.800	50.800
55.880	55.880
60.960	60.960
66.040	66.040
71.120	71.120
76.200	76.200
81.280	81.280
86.360	86.360
91.440	91.440
96.520	96.520
101.600	101.600
106.680	106.680
111.760	111.760
116.840	116.840
121.920	121.920
127.000	127.000
132.080	132.080
137.160	137.160
142.240	142.240
147.320	147.320
152.400	152.400
157.480	157.480
162.560	162.560
167.640	167.640
172.720	172.720
177.800	177.800
182.880	182.880
187.960	187.960
193.040	193.040
198.120	198.120
203.200	203.200
208.280	208.280
213.360	213.360
218.440	218.440
223.520	223.520
228.600	228.600
233.680	233.680
238.760	238.760
243.840	243.840
248.920	248.920
254.000	254.000
259.080	259.080
264.160	264.160
269.240	269.240
274.320	274.320
279.400	279.400
284.480	284.480
289.560	289.560
294.640	294.640
299.720	299.720
304.800	304.800
309.880	309.880
314.960	314.960
320.040	320.040
325.120	325.120
330.200	330.200
335.280	335.280
340.360	340.360
345.440	345.440
350.520	350.520
355.600	355.600
360.680	360.680
365.760	365.760
370.840	370.840
375.920	375.920
381.000	381.000
386.080	386.080
391.160	391.160
396.240	396.240
401.320	401.320
406.400	406.400
411.480	411.480
416.560	416.560
421.640	421.640
426.720	426.720
431.800	431.800
436.880	436.880
441.960	441.960
447.040	447.040
452.120	452.120
457.200	457.200
462.280	462.280
467.360	467.360
472.440	472.440
477.520	477.520
482.600	482.600
487.680	487.680
492.760	492.760
497.840	497.840
502.920	502.920
508.000	508.000
513.080	513.080
518.160	518.160
523.240	523.240
528.320	528.320
533.400	533.400
538.480	538.480
543.560	543.560
548.640	548.640
553.720	553.720
558.800	558.800
563.880	563.880
568.960	568.960
574.040	574.040
579.120	579.120
584.200	584.200
589.280	589.280
594.360	594.360
599.440	599.440
604.520	604.520
609.600	609.600
614.680	614.680
619.760	619.760
624.840	624.840
629.920	629.920
635.000	635.000
640.080	640.080
645.160	645.160
650.240	650.240
655.320	655.320
660.400	660.400
665.480	665.480
670.560	670.560
675.640	675.640
680.720	680.720
685.800	685.800
690.880	690.880
695.960	695.960
701.040	701.040
706.120	706.120
711.200	711.200
716.280	716.280
721.360	721.360
726.440	726.440
731.520	731.520
736.600	736.600
741.680	741.680
746.760	746.760
751.840	751.840
756.920	756.920
762.000	762.000
767.080	767.080
772.160	772.160
777.240	777.240
782.320	782.320
787.400	787.400
792.480	792.480
797.560	797.560
802.640	802.640
807.720	807.720
812.800	812.800
817.880	817.880
822.960	822.960
828.040	828.040
833.120	833.120
838.200	838.200
843.280	843.280
848.360	848.360
853.440	853.440
858.520	858.520
863.600	863.600
868.680	868.680
873.760	873.760
878.840	878.840
883.920	883.920
889.000	889.000
894.080	894.080
899.160	899.160
904.240	904.240
909.320	909.320
914.400	914.400
919.480	919.480
924.560	924.560
929.640	929.640
934.720	934.720
939.800	939.800
944.880	944.880
949.960	949.960
955.040	955.040
960.120	960.120
965.200	965.200
970.280	970.280
975.360	975.360
980.440	980.440
985.520	985.520
990.600	990.600
995.680	995.680
1000.760	1000.760
1005.840	1005.840
1010.920	1010.920
1016.000	1016.000
1021.080	1021.080
1026.160	1026.160
1031.240	1031.240
1036.320	1036.320
1041.400	1041.400
1046.480	1046.480
1051.560	1051.560
1056.640	1056.640
1061.720	1061.720
1066.800	1066.800
1071.880	1071.880
1076.960	1076.960
1082.040	1082.040
1087.120	1087.120
1092.200	1092.200
1097.280	1097.280
1102.360	1102.360
1107.440	1107.440
1112.520	1112.520
1117.600	1117.600
1122.680	1122.680
1127.760	1127.760
1132.840	1132.840
1137.920	1137.920
1143.000	1143.000
1148.080	1148.080
1153.160	1153.160
1158.240	1158.240
1163.320	1163.320
1168.400	1168.400
1173.480	1173.480
1178.560	1178.560
1183.640	1183.640
1188.720	1188.720
1193.800	1193.800
1198.880	1198.880
1203.960	1203.960
1209.040	1209.040
1214.120	1214.120
1219.200	1219.200
1224.280	1224.280
1229.360	1229.360
1234.440	1234.440
1239.520	1239.520
1244.600	1244.600
1249.680	1249.680
1254.760	1254.760
1259.840	1259.840
1264.920	1264.920
1270.000	1270.000
1275.080	1275.080
1280.160	1280.160
1285.240	1285.240
1290.320	1290.320
1295.400	1295.400
1300.480	1300.480
1305.560	1305.560
1310.640	1310.640
1315.720	1315.720
1320.800	1320.800
1325.880	1325.880
1330.960	1330.960
1336.040	1336.040
1341.120	1341.120
1346.200	1346.200
1351.280	1351.280
1356.360	1356.360
1361.440	1361.440
1366.520	1366.520
1371.600	1371.600
1376.680	1376.680
1381.760	1381.760
1386.840	1386.840
1391.920	1391.920
1397.000	1397.000
1402.080	1402.080
1407.160	1407.160
1412.240	1412.240
1417.320	1417.320
1422.400	1422.400
1427.480	1427.480
1432.560	1432.560
1437.640	1437.640
1442.720	1442.720
1447.800	1447.800
1452.880	1452.880
1457.960	1457.960
1463.040	1463.040
1468.120	1468.120
1473.200	1473.200
1478.280	1478.280
1483.360	1483.360
1488.440	1488.440
1493.520	1493.520
1498.600	1498.600
1503.680	1503.680
1508.760	1508.760
1513.840	1513.840
1518.920	1518.920
1524.000	1524.000
1529.080	1529.080
1534.160	1534.160
1539.240	1539.240
1544.320	1544.320
1549.400	1549.400
1554.480	1554.480
1559.560	1559.560
1564.640	1564.640
1569.720	1569.720
1574.800	1574.800
1579.880	1579.880
1584.960	1584.960
1590.040	1590.040
1595.120	1595.120
1600.200	1600.200
1605.280	1605.280
1610.360	1610.360
1615.440</	

## Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V41N012NLGI	8V41N012NLGI	72 Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
8V41N012NLGI8	8V41N012NLGI	72 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		23	Updated schematic with IDT crystal recommendation. Deleted prefix/suffix from part number throughout the datasheet. Updated header/footer.	7/22/15
C		23	Schematic - replaced IDT crystal recommendation with FOX crystal. Updated header/footer.	11/2/16



Corporate Headquarters  
6024 Silver Creek Valley Road  
San Jose, CA 95138 USA  
[www.IDT.com](http://www.IDT.com)

Sales  
1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
[www.IDT.com/go/sales](http://www.IDT.com/go/sales)

Tech Support  
[www.IDT.com/go/support](http://www.IDT.com/go/support)

DISCLAIMER Integrated Device Technology, Inc. (IDT) reserves the right to modify the products and/or specifications described herein at any time, without notice, at IDT's sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners. For datasheet type definitions and a glossary of common terms, visit [www.idt.com/go/glossary](http://www.idt.com/go/glossary). Integrated Device Technology, Inc. All rights reserved.

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[IDT \(Integrated Device Technology\):](#)

[8V41N012NLGI](#) [8V41N012NLGI8](#)