Crystal or Differential to Differential Clock Fanout Buffer

IDT8T39S10I

ADVANCE INFORMATION DATA SHEET

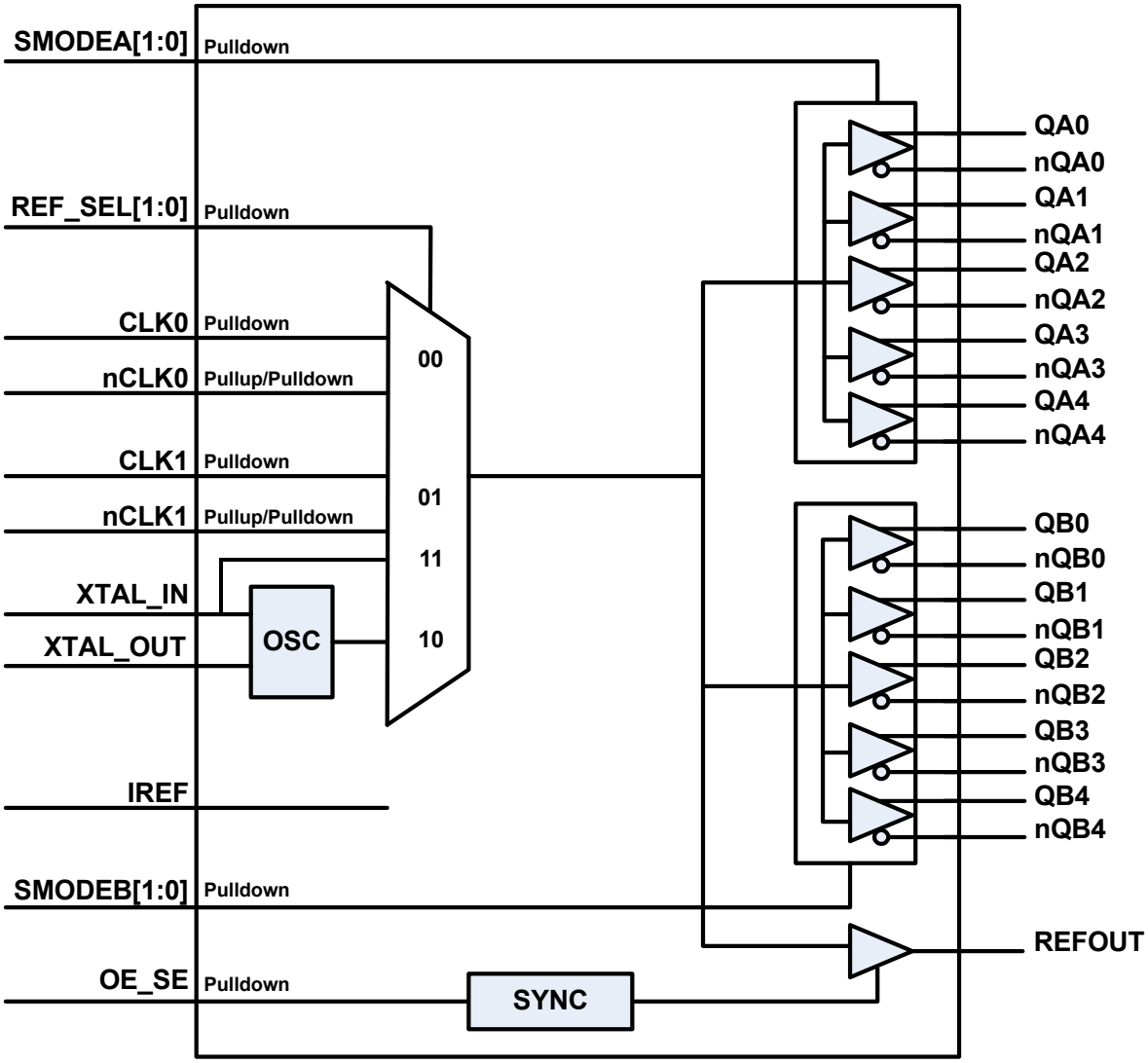
General Description

The IDT8T3910I is a high-performance clock fanout buffer. The input clock can be selected from two differential inputs or one crystal input. The internal oscillator circuit is automatically disabled if the crystal input is not selected. The crystal pin can be driven by single-ended clock when crystal is bypassed.The selected signal is distributed to ten differential outputs which can be configured as LVPECL, LVDS or HSCL outputs. In addition, an LVCMOS output is provided. The user should always turn off this LVCMOS output when (the) clock is over 200MHz. The differential outputs can be disabled into an high-impedance state. The device is designed for signal fanout of high-frequency, low phase-noise clock and data signal. The outputs are at a defined level when inputs are open or shorted. It's designed to operate from a 3.3V or 2.5V core power supply, and either a 3.3V or 2.5V output operating supply.

Features

- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL
- Crystal Oscillator Interface
- Crystal input frequency range: 10MHz to 50MHz
- Two banks, each has five differential output pairs that can be configured as LVPECL or LVDS or HCSL
- One single-ended reference output with synchronous enable to avoid clock glitch
- Output skew: (Bank A and Bank B at the same output level) 32ps (typical), design target
- Part-to-part skew: 200ps (typical), design target
- Additive RMS phase jitter: 0.08ps (typical), design target
- Power supply modes:
- Output supply voltage modes:
  V_{DD}/V_{DDO}
  3.3V/3.3V
  3.3V/2.5V
  2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment

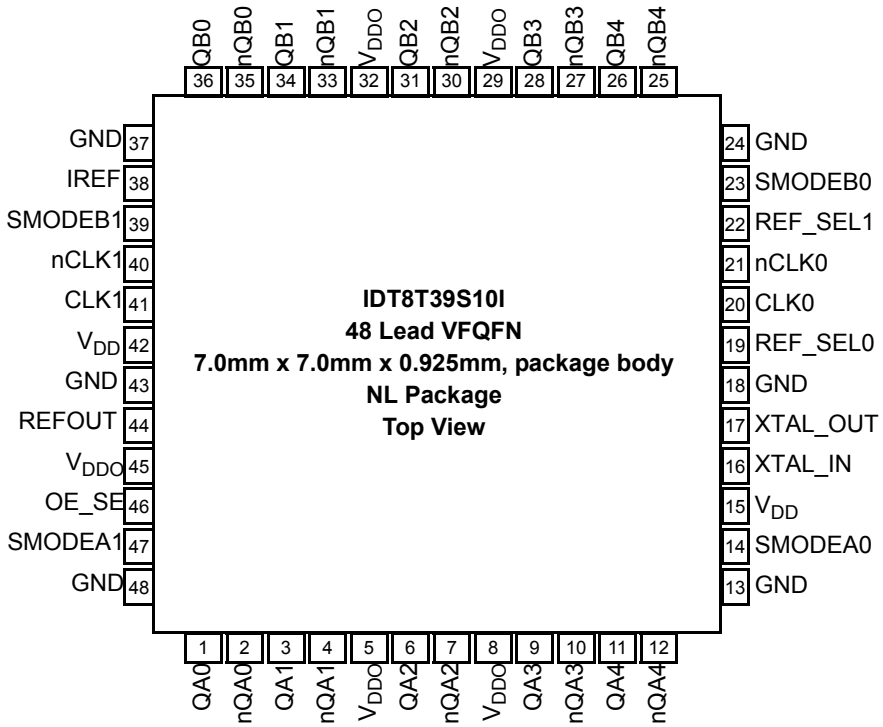


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QA0, nQA0	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
3, 4	QA1, nQA1	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
5, 8, 29, 32, 45	V_{DDO}	Power		Output supply pins
6, 7	QA2, nQA2	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
9, 10	QA3, nQA3	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
11, 12	QA4, nQA4	Output		Differential Bank A clock output pair. LVPECL, LVDS or HCSL interface levels.
13, 18, 24, 37, 43, 48	GND	Power		Power supply ground.
14, 47	SMODEA0, SMODEA1	Input	Pulldown	Output driver select for Bank A outputs. See Table 3D for function. LVCMOS/LVTTL interface levels.
15, 42	V_{DD}	Power		Power supply pins.
16, 17	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
19, 22	REF_SEL0, REF_SEL1	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See Table 3A for function.
20	CLK0	Input	Pulldown	Non-inverting differential clock.
21	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock. Internal resistor bias to $V_{DD}/2$.
23, 39	SMODEB0, SMODEB1	Input	Pulldown	Output driver select for Bank B outputs. See Table 3D for function. LVCMOS/LVTTL interface levels.
25, 26	nQB4, QB4	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
27, 28	nQB3, QB3	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
30, 31	nQB2, QB2	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
33, 34	nQB1, QB1	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
35, 36	nQB0, QB0	Output		Differential Bank B clock output pair. LVPECL, LVDS or HCSL interface levels.
38	IREF	Input		An external fixed precision resistor (475W) from this pin to ground provides a reference current used for differential current-mode QXx, nQXx clock outputs.
40	nCLK1	Input	Pullup/ Pulldown	Non-inverting differential clock. Internal resistor bias to $V_{DD}/2$.
41	CLK1	Input	Pulldown	Inverting differential clock.
44	REFOUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels
46	OE_SE	Input	Pulldown	Output enable. LVCMOS/LVTTL interface levels. See Table 3B.

NOTE: *Pulldown and Pullup* refer to an internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{PULLUP}	Input Pullup Resistor				51		kΩ
C_{PD}	Power Dissipation Capacitance		V_{DDO} = 3.3V		10 *Target		pF
			V_{DDO} = 2.5V		9 *Target		pF
R_{OUT}	Output Impedance	REFOUT	V_{DDO} = 3.3V		15 *Target		Ω
		REFOUT	V_{DDO} = 2.5V		20 *Target		Ω

*NOTE: Design Target Specs.

Function Tables

Table 3A. REF_SELx Function Table

Control Input	Selected Input Reference Clock
REF_SEL[1:0]	
00 (default)	CLK0, nCLK0
01	CLK1, nCLK1
10	XTAL
11	XTAL bypass

Table 3B. OE_SE Function Table

OE_SE	REFOUT
0 (default)	High-Impedance
1	Enabled

NOTE: Synchronous output enable to avoid clock glitch.

Table 3C. Input/Output Operation Table, OE_SE

Input Status			Output State
OE_SE	REF_SEL [1:0]	CLKx and nCLKx	REFOUT
0	Not care	Don't Care	High Impedance
1	10	Don't Care	Fanout crystal oscillator
1	11	Don't Care	Fanout single ended input on XTAL_IN pin
1	00	CLK0 and nCLK0 are both open circuit	Logic low
		CLK0 and nCLK0 are tied to ground	Logic low
		CLK0 is high, nCLK0 is low	Logic High
		CLK0 is low, nCLK0 is high	Logic Low
1	01	CLK1 and nCLK1 are both open circuit	Logic low
		CLK1 and nCLK1 are tied to ground	Logic low
		CLK1 is high, nCLK1 is low	Logic High
		CLK1 is low, nCLK1 is high	Logic Low

NOTE: The device output should support differential input being driven by a single-ended signal.

Table 3D. Input/Output Operation Table, SMODEA

Input Status			Output State
SMODEA[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QA[4:0], nQA[4:0]
11	Not care	Don't Care	High Impedance
00, 01 or 10	10	Don't Care	Fanout crystal oscillator
	11	Don't Care	Fanout single ended input on XTAL_IN pin
00, 01 or 10	00	CLK0 and nCLK0 are both open circuit	QA[4:0]=Low nQA4:0]=High
		CLK0 and nCLK0 are tied to ground	QA[4:0]=Low nQA[4:0]=High
		CLK0 is high, nCLK0 is low	QA[4:0]=High nQA[4:0]=Low
		CLK0 is low, nCLK0 is high	QA[4:0]=Low nQA[4:0]=High
00, 01 or 10	01	CLK1 and nCLK1 are both open circuit	QA[4:0]=Low nQA4:0]=High
		CLK1 and CLK1 are tied to ground.	QA[4:0]=Low nQA[4:0]=High
		CLK1 is high, nCLK1 is low	QA[4:0]=High nQA[4:0]=Low
		CLK1 is low, nCLK1 is high	QA[4:0]=Low nQA4:0]=High

NOTE: The device output should support differential input being driven by a single-ended signal.

Table 3E. Input/Output Operation Table, SMODEB

Input Status			Output State
SMODEB[1:0]	REF_SEL[1:0]	CLKx and nCLKx	QB[4:0], nQB[4:0]
11	Not care	Don't Care	High Impedance
00, 01 or 10	10 or 11	Don't Care	Fanout crystal oscillator
00, 01 or 10	00	CLK0 and nCLK0 are both open circuit	QB[4:0]=Low nQB4:0]=High
		CLK0 and nCLK0 are tied to ground	QB[4:0]=Low nQB[4:0]=High
		CLK0 is high, nCLK0 is low	QB[4:0]=High nQB[4:0]=Low
		CLK0 is low, nCLK0 is high	QB[4:0]=Low nQB[4:0]=High
00, 01 or 10	01	CLK1 and nCLK1 are both open circuit	QB[4:0]=Low nQB[4:0]=High
		CLK1 and nCLK1 are tied to ground	QB[4:0]=Low nQB[4:0]=High
		CLK1 is high, nCLK1 is low	QB[4:0]=High nQB[4:0]=Low
		CLK1 is low, nCLK1 is high	QB[4:0]=Low nQB[4:0]=High

NOTE: The device output should support differential input being driven by a single-ended signal.

Table 3F. Selection Table, QAx = nQAx, x=[0:4]

SMODEA1	SMODEA0	Output Type
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Hi-Z

Table 3G. Selection Table, QBx = nQBx, x=[0:4]

SMODEB1	SMODEB0	Output Type
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Hi-Z

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.63V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O, (HCSL, LVCMOS)	-0.5V to V_{DDO} + 0.5V
Outputs, I_O, (LVPECL) Continuous Current Surge Current	 50mA 100mA
Outputs, I_O, (LVDS) Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	29°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = V_{DDO} = 3.3V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 01				mA
I_{DDO}	Output Supply Current	SMODEA/B[1:0] = 01				mA
I_{EE}	Power Supply Current	SMODEA/B[1:0] = 00 (default)				mA
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 10				mA
I_{DDO}	Power Supply Current	SMODEA/B[1:0] = 10				mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 01				mA
I_{DDO}	Output Supply Current	SMODEA/B[1:0] = 01				mA
I_{EE}	Power Supply Current	SMODEA/B[1:0] = 00 (default)				mA
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 10				mA
I_{DDO}	Power Supply Current	SMODEA/B[1:0] = 10				mA

Table 4C. Power Supply DC Characteristics, V_{DD} = 2.5V±5%, V_{DDO} = 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 01				mA
I_{DDO}	Output Supply Current	SMODEA/B[1:0] = 01				mA
I_{EE}	Power Supply Current	SMODEA/B[1:0] = 00 (default)				mA
I_{DD}	Power Supply Current	SMODEA/B[1:0] = 10				mA
I_{DDO}	Power Supply Current	SMODEA/B[1:0] = 10				mA

Table 4D. LVCMOS/LVTTL DC Characteristics,
V_{DD} = 3.3V±5%, 2.5V±5%, V_{DDO} = 3.3V±5% or 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V±5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V±5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V±5%	-0.3		0.8	V
			V_{DD} = 2.5V±5%	-0.3		0.7	V
I_{IH}	Input High Current	REF_SEL, SMODEA, SMODEB, OE_SE	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	OE_SE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1	REFOUT	V_{DDO} = 3.3V±5%: I_{OH} = -TBDmA	2.6			V
		REFOUT	V_{DDO} = 2.5V±5%: I_{OH} = -TBDmA	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	REFOUT	V_{DDO} = 3.3V±5% or 2.5V±5%: I_{OL} = TBDmA			0.5	V

Table 4E. Differential DC Characteristics, V_{DD} = 3.3V±5% or 2.625V T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK[0:1], nCLK[0:1]	V_{DD} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	CLK[0:1]	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		nCLK[0:1]	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.3		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2. Common mode voltage is defined as V_{IH}.

Table 4F. LVPECL DC Characteristics, V_{DD} = V_{DDO} = 3.3V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} – 1.4		V_{DDO} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} – 2.0		V_{DDO} – 1.7 *Target	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

*NOTE: Design Target Specs.
NOTE 1: Outputs terminated with 50Ω to V_{DDO} – 2V.

Table 4G. LVPECL DC Characteristics, V_{DD} = 3.3V±5% or 2.625V, V_{DDO} = 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} – 1.4		V_{DDO} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} – 2.0		V_{DDO} – 1.4 *Target	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

*NOTE: Design Target Specs.
NOTE 1: Outputs terminated with 50Ω to V_{DDO} – 2V.

Table 4H. LVDS DC Characteristics, V_{DD} = V_{DDO} = 3.3V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			405*Target		mV
ΔV_{OD}	V_{OD} Magnitude Change			50*Target		mV
V_{OS}	Offset Voltage			1.26*Target		V
ΔV_{OS}	V_{OS} Magnitude Change			50*Target		mV

*NOTE: Design Target Specs.

Table 4I. LVDS DC Characteristics, V_{DD} = V_{DDO} = 2.5V±5%, GND = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			405*Target		mV
ΔV_{OD}	V_{OD} Magnitude Change			50*Target		mV
V_{OS}	Offset Voltage			1.26*Target		V
ΔV_{OS}	V_{OS} Magnitude Change			50*Target		mV

*NOTE: Design Target Specs.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		50	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6A. AC Characteristics, V_{DD} = V_{DDO} = 3.3V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Using External Crystal	10*Target		50*Target	MHz
		LVDS, LVPECL output		1500*Target		MHz
		HCSL output			250*Target	MHz
		LVCMOS output			250*Target	MHz
*t*jit	Buffer Additive Phase Jitter, RMS: 156.25MHz Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01	SMODEA/B[1:0] = 00		0.08*Target		ps
		SMODEA/B[1:0] = 01		0.08*Target		ps
		SMODEA/B[1:0] = 10		0.08*Target		ps
tjit(θ)	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz	REF_SEL[1:0] = 10 or 11		0.3*Target		ps
t_{PD}	Propagation Delay; CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs; NOTE 1	SMODEA/B[1:0] = 00		500*Target		ps
		SMODEA/B[1:0] = 01		500*Target		ps
		SMODEA/B[1:0] = 10		500*Target		ps
*t*sk(o)	Output Skew; NOTE 2, 3			32*Target		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			200*Target		ps
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	HCSL Outputs	-100*Target		100*Target	mV
V_{MAX}	Voltage High; NOTE 7, 8	HCSL Outputs			920*Target	mV
V_{MIN}	Voltage Low; NOTE 7, 9	HCSL Outputs	-150*Target		+150*Target	mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	HCSL Outputs	250*Target		520*Target	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	HCSL Outputs			140*Target	mV
	Rise/Fall Edge Rate; NOTE 7, 13	HCSL Outputs; Measured between 150mV to +150mV	0.6*Target		4.0*Target	V/ns
t_R / t_F	Output Rise/Fall Time	SMODEA/B[1:0] = 00; 20% to 80%		175*Target		ps
		SMODEA/B[1:0] = 01; 20% to 80%		175*Target		ps
$MUX_{\_ISOLATION}$	MUX Isolation	156.25MHz		83*Target		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

*NOTE: Design Target Specs

NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

NOTE 5: Measurement taken from differential waveform.

NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.

NOTE 7: Measurement taken from single-ended waveform.

NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 10: Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

Notes continued on next page.

NOTE 11: Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoints for this measurement.
NOTE 12: Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Table 6B. AC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Using External Crystal	10*Target		50*Target	MHz
		LVDS, LVPECL output		500*Target		MHz
		HCSL output		1500*Target	250*Target	MHz
		LVCMOS output			250*Target	MHz
tjit	Additive Phase Jitter: 156.25MHz Integration Range: 12kHz - 20MHz REF_SEL[1:0] = 00 or 10	SMODEA/B[1:0] = 00		0.08*Target		ps
		SMODEA/B[1:0] = 01		0.08*Target		ps
		SMODEA/B[1:0] = 10		0.08*Target		ps
tjit	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz	REF_SEL[1:0] = 10 or 11		0.3*Target		ps
t_{PD}	Propagation Delay; CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs; NOTE 1	SMODEA/B[1:0] = 00		500*Target		ps
		SMODEA/B[1:0] = 01		500*Target		ps
		SMODEA/B[1:0] = 10		500*Target		ps
*t*sk(o)	Output Skew; NOTE 2, 3			32*Target		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			200*Target		ps
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	HCSL Outputs	-100*Target		100*Target	mV
V_{MAX}	Voltage High; NOTE 7, 8	HCSL Outputs			920*Target	mV
V_{MIN}	Voltage Low; NOTE 7, 9	HCSL Outputs	-150*Target		+150*Target	mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	HCSL Outputs	250*Target		520*Target	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	HCSL Outputs			140*Target	mV
	Rise/Fall Edge Rate; NOTE 7, 13	HCSL Outputs; Measured between 150mV to +150mV	0.6*Target		4.0*Target	V/ns
t_R / t_F	Output Rise/Fall Time	SMODEA/B[1:0] = 00; 20% to 80%		175*Target		ps
		SMODEA/B[1:0] = 01; 20% to 80%		175*Target		ps
$MUX_{\_ISOLATION}$	MUX Isolation	156.25MHz		83*Target		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
NOTE 5: Measurement taken from differential waveform.
NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.
Notes continued on next page.

NOTE 7: Measurement taken from single-ended waveform.
NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 10: Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.
NOTE 11: Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoints for this measurement.
NOTE 12: Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

Table 6C. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V±5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Using External Crystal	10*Target		50*Target	MHz
		LVDS, LVPECL output		1500*Target		MHz
		HCSL output			250*Target	MHz
		LVCMOS output			250*Target	MHz
tjit	Additive Phase Jitter:156.25MHz Integration Range 12kHz - 20MHz REF_SEL[1:0] = 00 or 01	SMODEA/B[1:0] = 00		0.08*Target		ps
		SMODEA/B[1:0] = 01		0.08*Target		ps
		SMODEA/B[1:0] = 10		0.08*Target		ps
tjit	RMS Phase Jitter; 25MHz Integration Range: 100Hz - 1MHz	REF_SEL[1:0] = 10 or 11		0.3*Target		ps
t_{PD}	Propagation Delay; CLK0, nCLK0 or CLK1, nCLK1 to any Qx, nQx Outputs; NOTE 1	SMODEA/B[1:0] = 00		500*Target		ps
		SMODEA/B[1:0] = 01		500*Target		ps
		SMODEA/B[1:0] = 10		500*Target		ps
*t*sk(o)	Output Skew; NOTE 2, 3			32*Target		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4			200*Target		ps
V_{RB}	Ring-back Voltage Margin; NOTE 5, 6	HCSL Outputs	-100*Target		100*Target	mV
V_{MAX}	Voltage High; NOTE 7, 8	HCSL Outputs			920*Target	mV
V_{MIN}	Voltage Low; NOTE 7, 9	HCSL Outputs	-150*Target		+150*Target	mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 7, 10, 11	HCSL Outputs	250*Target		520*Target	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 7, 10, 12	HCSL Outputs			140*Target	mV
	Rise/Fall Edge Rate; NOTE 7, 13	HCSL Outputs; Measured between 150mV to +150mV	0.6*Target		4.0*Target	V/ns
t_R / t_F	Output Rise/Fall Time	SMODEA/B[1:0] = 00; 20% to 80%		175*Target		ps
		SMODEA/B[1:0] = 01; 20% to 80%		175*Target		ps
$MUX_{\_ISOLATION}$	MUX Isolation	156.25MHz		83*Target		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
*NOTE: Design Target Specs
NOTE 1: Measured from the differential input crosspoint to the differential output crosspoint.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
Notes continued on next page.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
NOTE 5: Measurement taken from differential waveform.
NOTE 6: T_{STABLE} is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.
NOTE 7: Measurement taken from single-ended waveform.
NOTE 8: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 9: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 10: Measured at crosspoint where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.
NOTE 11: Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoints for this measurement.
NOTE 12: Defined as the total variation of all crossing voltages of rising Qx and falling nQx, This is the maximum allowed variance in Vcross for any particular system.
NOTE 13: Measured from -150mV to +150mV on the differential waveform (Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing

Reliability Information

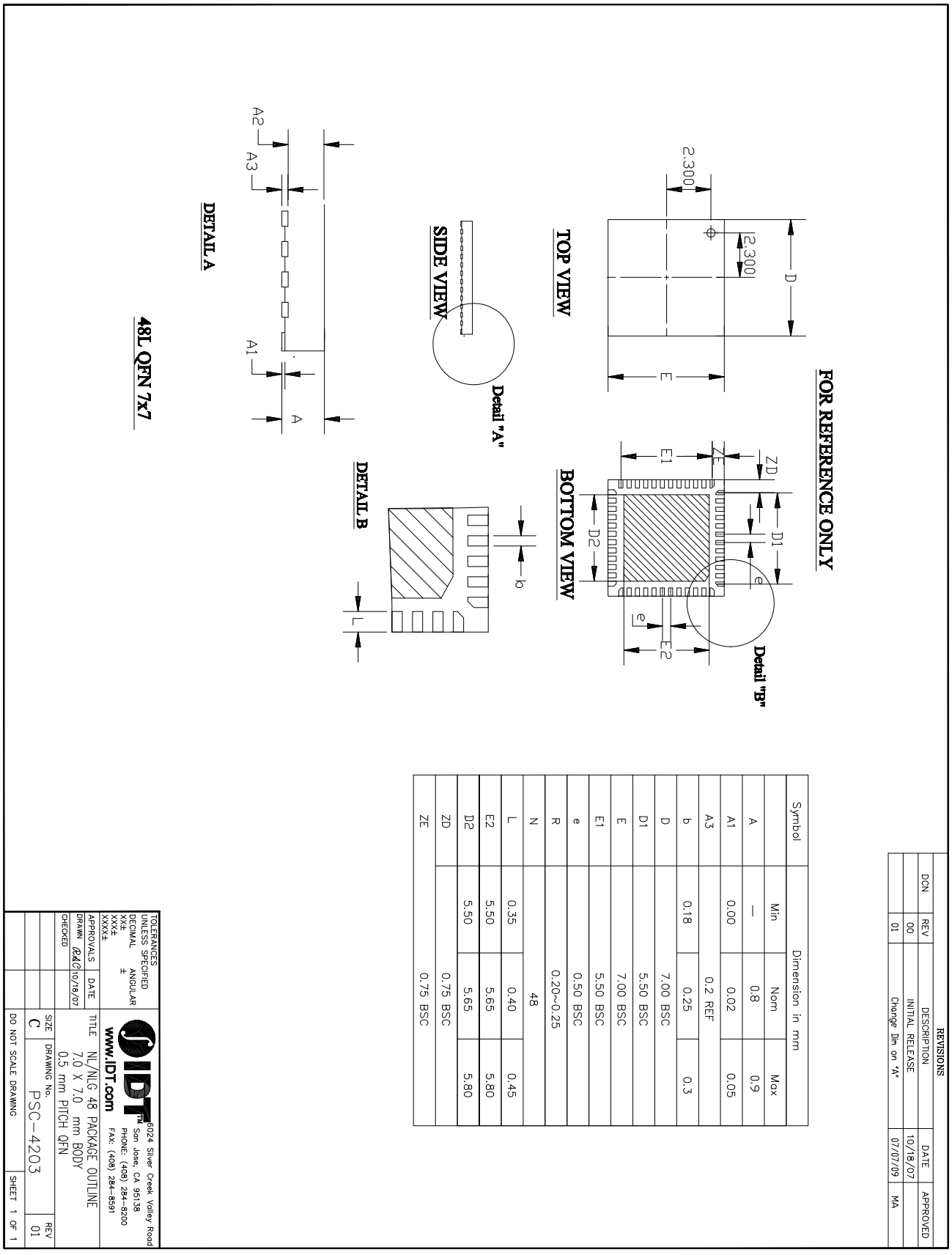
Table 7. θ_{JA} vs. Air Flow Table for a 48 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	30.5°C/W	26.7°C/W	23.9°C/W

Transistor Count

The transistor count for IDT8T39S10I is: TBD

48 VFQFN Package Outline and Package Dimensions



REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	10/18/07	
	01	Change Dim on "A"	07/07/09	MA

Symbol	Dimension in mm		
	Min	Nom	Max
A	—	0.8	0.9
A1	0.00	0.02	0.05
A3		0.2 REF	
b	0.18	0.25	0.3
D		7.00 BSC	
D1		5.50 BSC	
E		7.00 BSC	
E1		5.50 BSC	
e		0.50 BSC	
R		0.20~0.25	
N		48	
L	0.35	0.40	0.45
E2	5.50	5.65	5.80
D2	5.50	5.65	5.80
ZD		0.75 BSC	
ZE		0.75 BSC	

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS DATE
DRAWN RAC 10/18/07
CHECKED

IDT™ 6024 Silver Creek Valley Road San Jose, CA 95138
www.IDT.com PHONE: (408) 284-8200 FAX: (408) 284-8591

TITLE NL/NLG 48 PACKAGE OUTLINE 7.0 X 7.0 mm BODY 0.5 mm PITCH QFN

SIZE C
DRAWING No. PSC-4203
REV 01

DO NOT SCALE DRAWING
SHEET 1 OF 1

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T39S10BNLGI	TBD	Lead-Free, 48 Lead VFQFN	Tray	-40°C to 85°C
8T39S10BNLGI8	TBD	Lead-Free, 48 Lead VFQFN	Tape & Reel	-40°C to 85°C

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