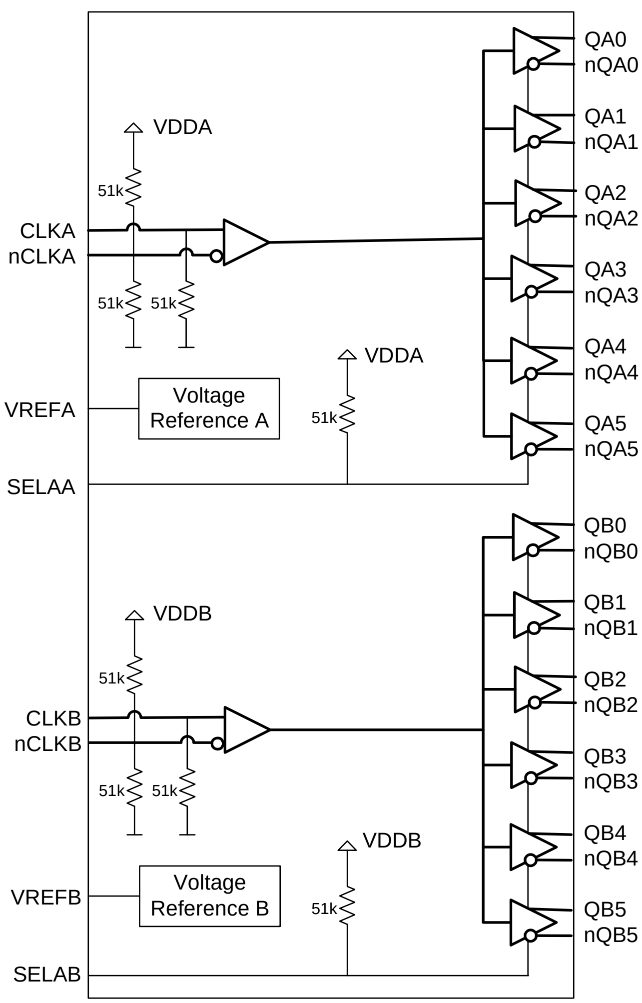
General Description

The 8P34S2106 is a high-performance, low-power, differential dual 1:6 LVDS Output 1.8V Fanout Buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. Two independent buffer channels are available, each channel has six low skew outputs. High isolation between channels minimizes noise coupling. AC characteristics such as propagation delay are matched between channels. Guaranteed output-to-output and part-to-part skew characteristics make the 8P34S2106 ideal for those clock distribution applications demanding well-defined performance and repeatability. The device is characterized to operate from a 1.8V power supply. The integrated bias voltage references enable easy interfacing of AC-coupled signals to the device inputs.

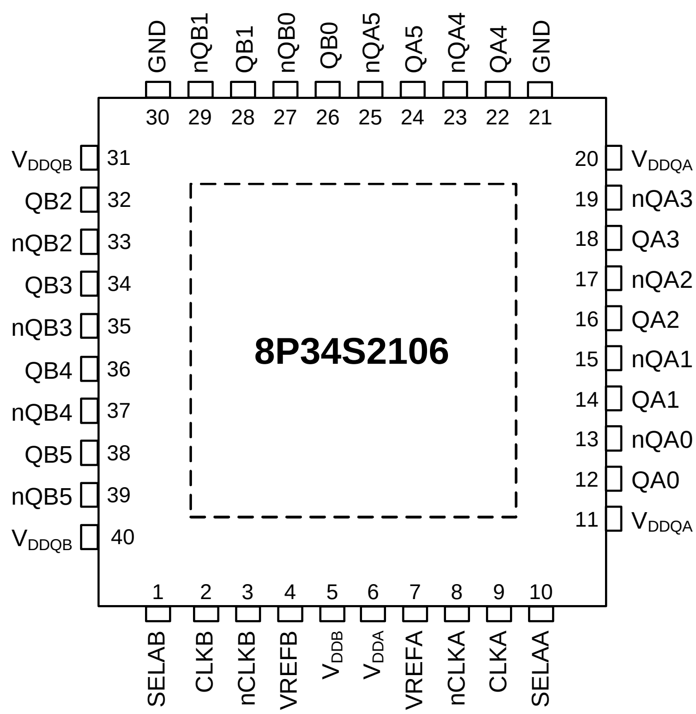
Features

- Dual 1:6 low skew, low additive jitter LVDS fanout buffers
- Matched AC characteristics across both channels
- High isolation between channels
- Low power consumption
- Both differential CLKA, nCLKA and CLKB, nCLKB inputs accept LVDS, LVPECL and single-ended LVCMOS levels
- Maximum input clock frequency: 2GHz
- Output amplitudes: 350mV, 500mV (selectable)
- Output bank skew: 10ps typical
- Output skew: 20ps typical
- Low additive phase jitter, RMS: 45fs typical, (f_{REF} = 156.25MHz, 12kHz - 20MHz)
- Full 1.8V supply voltage mode
- Lead-free (RoHS 6), 40-lead VFQFN packaging
- -40°C to 85°C ambient operating temperature
- Supports case temperature up to 105°C

Block Diagram



Pin Assignment



40-pin, 6mm x 6mm VFQFN

Pin Descriptions and Characteristics

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
1	SELAB	Input	Pullup	Control input. Output amplitude select for channel B.
2	CLKB	Input	Pulldown	Non-inverting differential clock/data input for channel B.
3	nCLKB	Input	Pulldown/ Pullup	Inverting differential clock/data input for channel B.
4	VREFB	Output		Bias voltage reference for the CLKB, nCLKB input pairs.
5	V_{DDB}	Power		Power supply pin for the core and inputs of channel B.
6	V_{DDA}	Power		Power supply pin for the core and inputs of channel A.
7	VREFA	Output		Bias voltage reference for the CLKA, nCLKA input pairs.
8	nCLKA	Input	Pulldown/ Pullup	Inverting differential clock/data input for channel A.
9	CLKA	Input	Pulldown	Non-inverting differential clock/data input for channel A.
10	SELAA	Input	Pullup	Control input. Output amplitude select for channel A.
11	V_{DDQA}	Power		Power supply pin for the channel A outputs QA[0:5]
12	QA0	Output		Differential output pair A0. LVDS interface levels.
13	nQA0	Output		Differential output pair A0. LVDS interface levels.
14	QA1	Output		Differential output pair A1. LVDS interface levels.
15	nQA1	Output		Differential output pair A1. LVDS interface levels.
16	QA2	Output		Differential output pair A2. LVDS interface levels.
17	nQA2	Output		Differential output pair A2. LVDS interface levels.
18	QA3	Output		Differential output pair A3. LVDS interface levels.
19	nQA3	Output		Differential output pair A3. LVDS interface levels.
20	V_{DDQA}	Power		Power supply pin for the channel A outputs QA[0:5]
21	GND	Power		Power supply ground.
22	QA4	Output		Differential output pair A4. LVDS interface levels.
23	nQA4	Output		Differential output pair A4. LVDS interface levels.
24	QA5	Output		Differential output pair A5. LVDS interface levels.
25	nQA5	Output		Differential output pair A5. LVDS interface levels.
26	QB0	Output		Differential output pair B0. LVDS interface levels.
27	nQB0	Output		Differential output pair B0. LVDS interface levels.
28	QB1	Output		Differential output pair B1. LVDS interface levels.
29	nQB1	Output		Differential output pair B1. LVDS interface levels.
30	GND	Power		Power supply ground.
31	V_{DDQB}	Power		Power supply pin for the channel B outputs QB[0:5].
32	QB2	Output		Differential output pair B2. LVDS interface levels.
33	nQB2	Output		Differential output pair B2. LVDS interface levels.
34	QB3	Output		Differential output pair B3. LVDS interface levels.
35	nQB3	Output		Differential output pair B3. LVDS interface levels.
36	QB4	Output		Differential output pair B4. LVDS interface levels.
37	nQB4	Output		Differential output pair B4. LVDS interface levels.
38	QB5	Output		Differential output pair B5. LVDS interface levels.
39	nQB5	Output		Differential output pair B5. LVDS interface levels.
40	V_{DDQB}	Power		Power supply pin for the channel B outputs QB[0:5].
ePad	G_{ND_EPAD}	Power		Exposed pad of package. Connect to ground.

NOTE 1. *Pulldown* and *Pullup* refers to an internal input resistors. See Table 2 *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3A. SELAA Bank A Output Amplitude Selection

SELAA	QA Output Amplitude (mV)
0	350
1 (default)	500

Table 3B. SELAB Bank B Output Amplitude Selection

SELAB	QB Output Amplitude (mV)
0	350
1 (default)	500

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}[1]	3.6V
Inputs, V_I	-0.5V to 3.6V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Input Sink/Source, IREF	±2mA
Operating Junction Temperature, $T_{J,MAX}$	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[2]	2000V
ESD - Charged Device Model[2]	1500V

NOTE 1. V_{DD} denotes, V_{DDA}, V_{DDB}.
NOTE 2. According to JEDEC JS-001-2012/JESD22-C101E.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DDA} = V_{DDB} = V_{DDQB} = V_{DDQA} = 1.8V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{DDA}, V_{DDB}	Power Supply Voltage			1.71	1.8	1.89	V
V_{DDQA}, V_{DDQB}	Output Supply Voltage			1.71	1.8	1.89	V
I_{DDA} + I_{DDB} + I_{DDQA} + I_{DDQB}	Core and Output Supply Current	QA[0:5], QB[0:5] Outputs Terminated 100Ω between Qx, nQx	500mV Amplitude			390	mA
			350mV Amplitude			275	mA

Table 4B. LVCMOS Inputs DC Characteristics, $V_{DDA} = V_{DDB} = V_{DDQB} = V_{DDQA} = 1.8V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	SELAA, SELAB		0.75 · V_{DD}[1]		V_{DD}[1] + 0.3	V
V_{IL}	Input Low Voltage	SELAA, SELAB		-0.3		0.25 · V_{DD}[1]	V
I_{IH}	Input High Current	SELAA, SELAB	$V_{IN} = V_{DD}$[1] = 1.89V			10	µA
I_{IL}	Input Low Current	SELAA, SELAB	V_{IN} = 0V, V_{DD}[1] = 1.89V	-150			µA

NOTE 1. V_{DD} denotes, V_{DDA}, V_{DDB}.

Table 4C. Differential Inputs Characteristics, $V_{DDA} = V_{DDB} = V_{DDQB} = V_{DDQA}$ = 1.8V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLKA, nCLKA CLKB, nCLKB	$V_{IN} = V_{DD}$[1] = 1.89V			150	µA
I_{IL}	Input Low Current	CLKA, CLKB	V_{IN} = 0V, V_{DD}[1] = 1.89V	-10			µA
		nCLKA, nCLKB	V_{IN} = 0V, V_{DD}[1] = 1.89V	-150			µA
VREFA, B	Reference Voltage[2]		IREF = +100µA, V_{DD}[1] = 1.8V	0.9		1.30	V

NOTE 1. V_{DD} denotes, V_{DDA}, V_{DDB}.
NOTE 2. VREF[A:B] specification is applicable to the AC-coupled input interfaces shown in Figure 2B and Figure 2C.

Table 4D. LVDS DC Characteristics, $V_{DDA} = V_{DDB} = V_{DDQB} = V_{DDQA}$ = 1.8V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

Table 5. AC Electrical Characteristics, $V_{DDA} = V_{DDB} = V_{DDQB} = V_{DDQA} = 1.8V \pm 5\%$, T_A = -40°C to 85°C [1]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency				2	GHz
$\Delta V/\Delta t$	Input Edge Rate		1.5			V/ns
t_{PD}	Propagation Delay[2, 3]	CLKA to any QAx, CLKB to any nQBx	100	255	400	ps
*t*sk(o)	Output Skew[4, 5]			20	40	ps
*t*sk(b)	Output Bank Skew[5, 6]			10	25	ps
*t*sk(p)	Pulse Skew[7]	f_{REF} = 100MHz		5	25	ps
*t*sk(pp)	Part-to-Part Skew[5, 8]				200	ps
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; 500mV Output Amplitude	f_{REF} = 156.25MHz Integration Range: 1kHz – 40MHz		60	80	fs
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; 500mV Output Amplitude	f_{REF} = 156.25MHz Square Wave, V_{PP} = 1V, Integration Range: 12kHz – 20MHz		45	60	fs
$\Phi_N(\geq 30M)$	Clock Single-side Band Phase Noise	≥30MHz Offset from Carrier and Noise Floor		< -160		dBc/Hz
$t_{JIT, SP}$	Spurious Suppression, Coupling between Channels	f_{QA} = 491.52MHz, f_{QB} = 61.44MHz, Measured between Neighboring Outputs		-55		dB
$t_{JIT, SP}$	Spurious Suppression, Coupling between Channels	f_{QA} = 491.52MHz, f_{QB} = 15.36MHz, Measured between Neighboring Outputs		-65		dB
t_R / t_F	Output Rise/ Fall Time	10% to 90%, Outputs Loaded with 100Ω		150	400	ps
t_R / t_F	Output Rise/ Fall Time	20% to 80%, Outputs Loaded with 100Ω		90	160	ps
V_{PP}	Input Voltage Amplitude; CLKA, CLKB		0.15		1.2	V
V_{PP_DIFF}	Differential Input Voltage Amplitude; CLKA, CLKB		0.3		2.4	V
V_{CMR}	Common Mode Input Voltage[9]		1.1		V_{DD}[10] – (V_{PP}/2)	V
V_{OD}	Differential Output Voltage	SELAA, SELAB = 0, Outputs Loaded with 100Ω	247	350	454	mV
V_{OD}	Differential Output Voltage	SELAA, SELAB = 1, Outputs Loaded with 100Ω	350	500	650	mV
V_{OS}	Offset Voltage	SELAA, SELAB = 0		0.8		V
V_{OS}	Offset Voltage	SELAA, SELAB = 1		0.7		V

NOTE 1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2. Measured from the differential input crossing point to the differential output crossing point.

NOTE 3. Input V_{PP} = 400mV.

NOTE 4. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 5. This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6. Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

NOTE 7. Output pulse skew is the absolute value of the difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

NOTE 8. Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 9. Common Mode Input Voltage is defined as the cross-point voltage.

NOTE 10. V_{DD} denotes, V_{DDA}, V_{DDB}.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pullup resistors. Additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

VREFX

The unused VREFA and VREFB pins can be left floating. We recommend that there is no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 1.8V and V_{DD} = 1.8V, R1 and R2 value should be adjusted to set V_1 at 0.9V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω.

The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

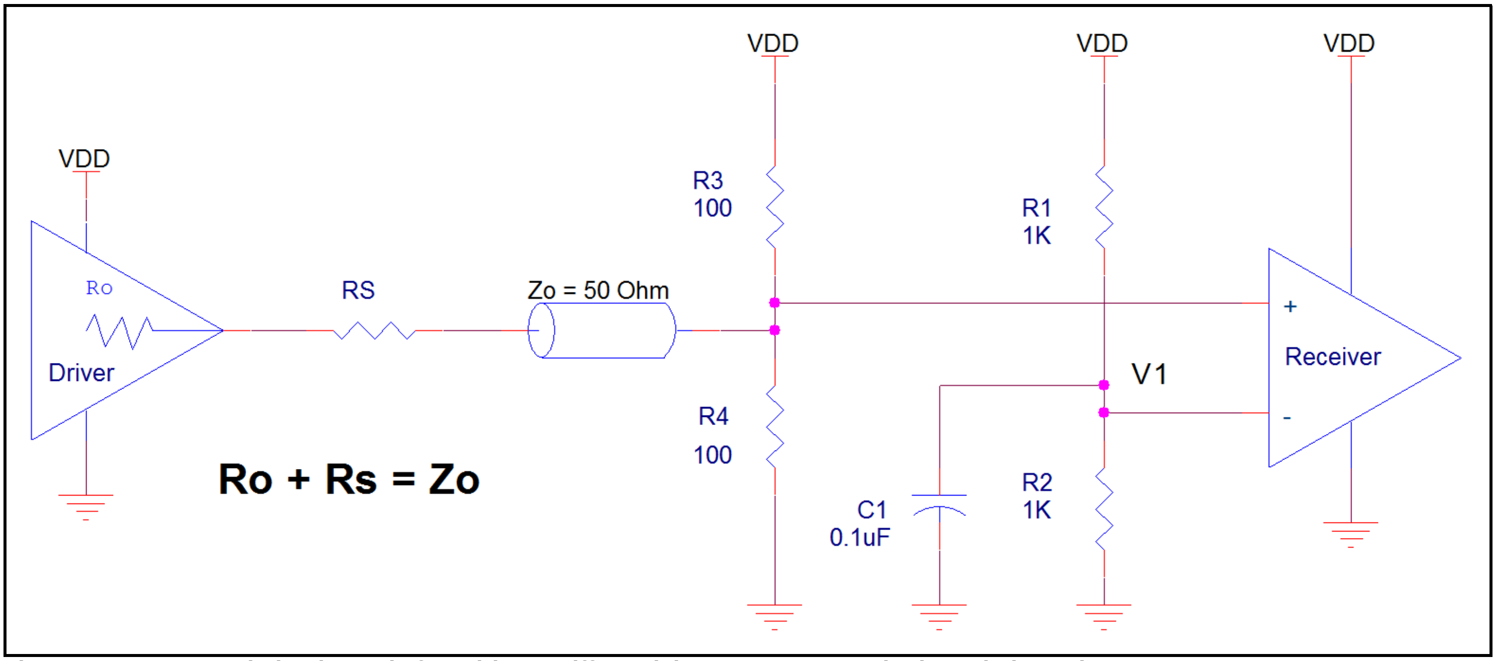


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

1.8V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. The differential input signal must meet both the V_{PP} and V_{CMR} input requirements. Figure 2A *to* Figure 2C show interface examples for the CLK /nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

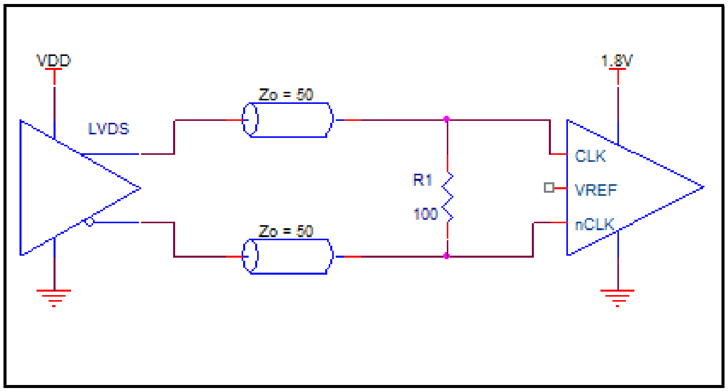


Figure 2A. Differential Input Driven by an LVDS Driver - DC Coupling

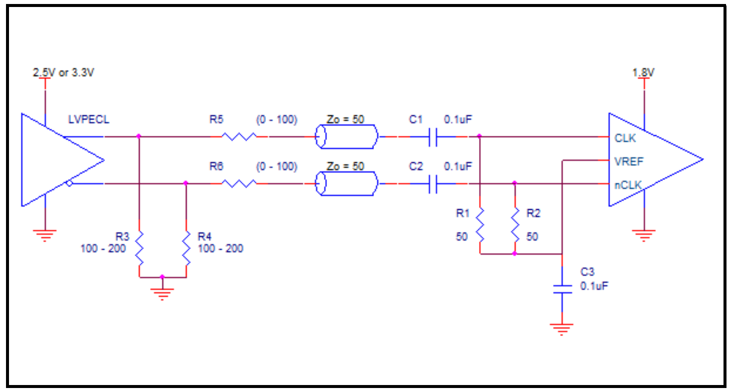


Figure 2C. Differential Input Driven by an LVPECL Driver - AC Coupling

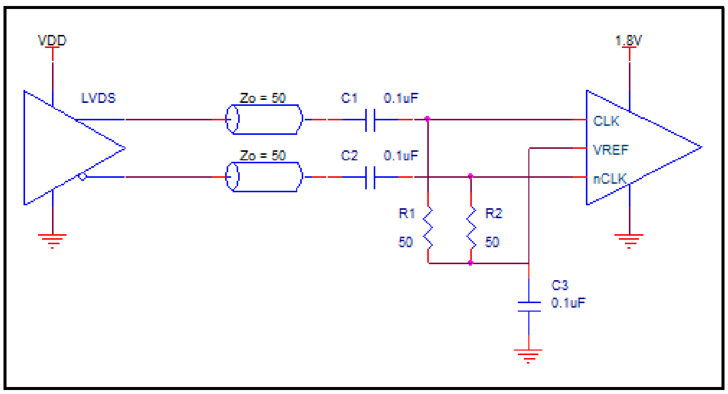


Figure 2B. Differential Input Driven by an LVDS Driver - AC Coupling

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 3A can be used with either type of output structure. Figure 3B, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

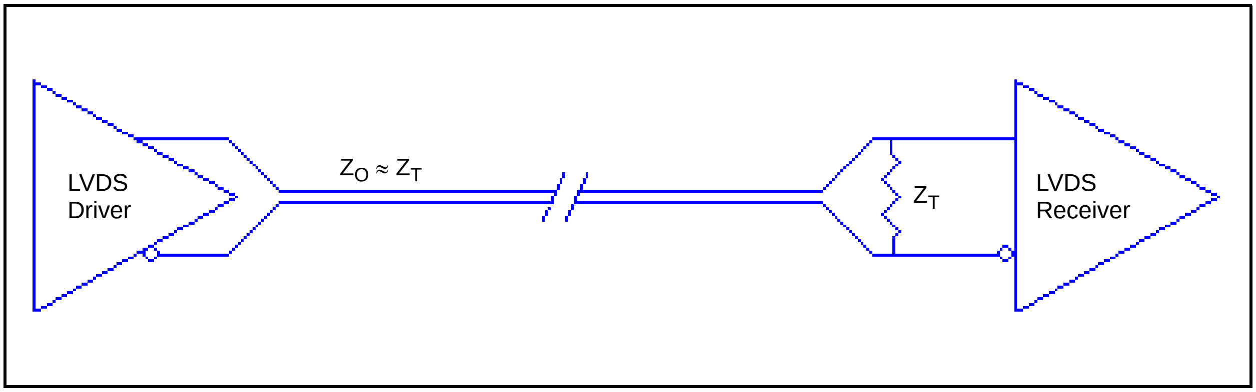


Figure 3A. Standard LVDS Termination

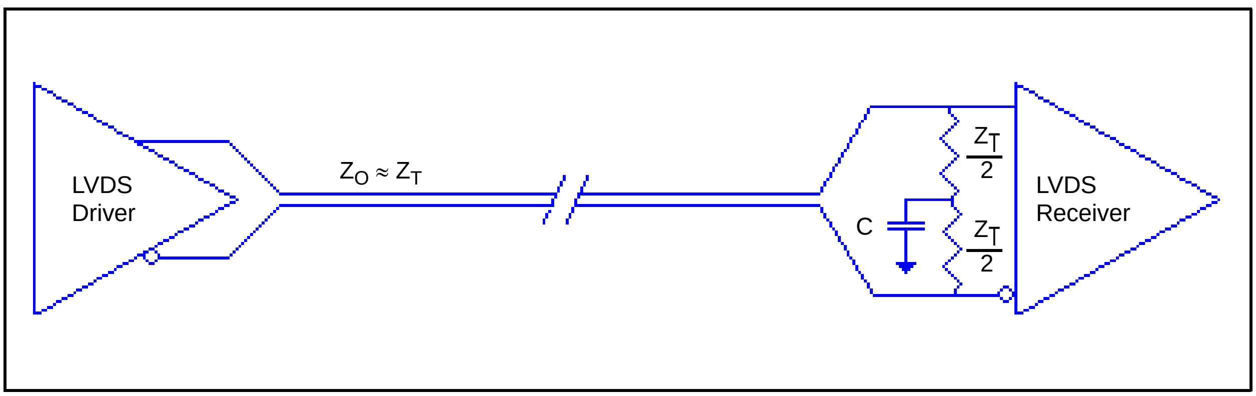


Figure 3B. Optional LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 4. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

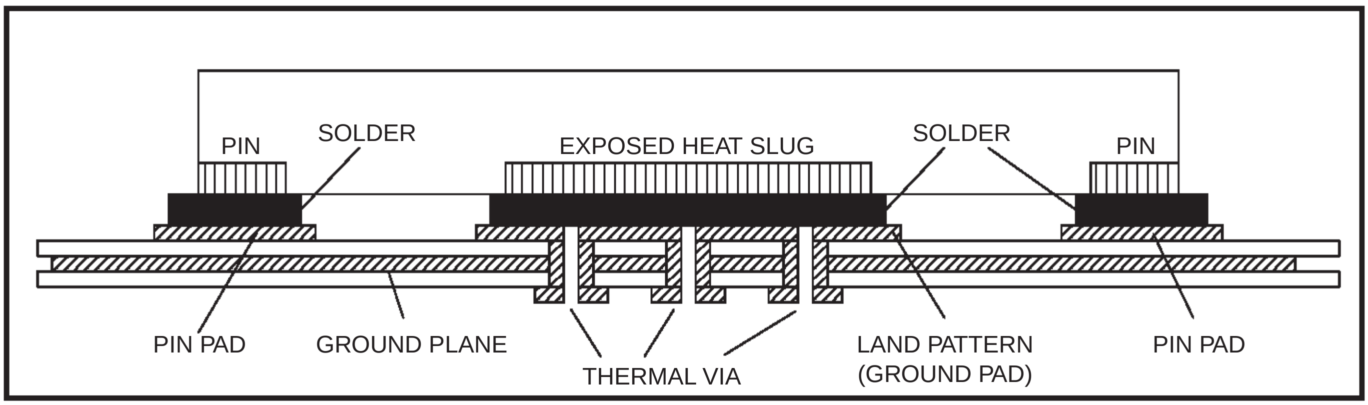


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter Ψ_{JB} (Psi-JB) to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter, $\Psi_{JB,}$ is calculated using the following equation:

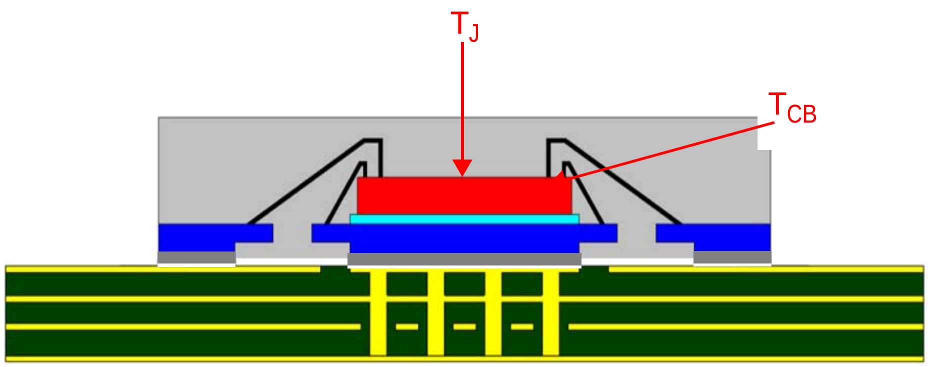
$T_J = T_{CB} + \Psi_{JB} \times P_{D,}$ where

T_J = Junction temperature at steady state condition in (^oC).

T_{CB} = Case temperature (Bottom) at steady state condition in (^oC).

Ψ_{JB} = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

P_D = power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature (T_{CB}). A good connection ensures that temperature at the exposed pad (T_{CB}) and the board temperature (T_B) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature (T_J): $T_J = T_{CB} + \Psi_{JB} \times P_D$

Package type	40 VFQFN
Body size (mm)	6 x 6 x 0.9
ePad size (mm)	4.65 x 4.65
Thermal Via	4x4 Matrix
Ψ_{JB}	1.5C/W
T_{CB}	105^{o}C
P_D	0.71W

For the variables above, the junction temperature is equal to 106.1^{o}C. Since this is below the maximum junction temperature of 125^{o}C, there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 115^{o}C, this device can function without the degradation of the specified AC or DC parameters.

Power Considerations

This section provides information on power dissipation and junction temperature for the 8P34S2106.
Equations and example calculations are also provided.

1. Power Dissipation.

The following is the power dissipation for V_{DD} = 1.8V + 5% = 1.89V, which gives worst case results.

Maximum current at 85°C: V_{DD_MAX} = 390mA

- Power$_{_MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 1.89V * 390mA = **737.1mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 24.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.7371W * 24.6°C/W = 103.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 40 Lead VFQFN, Forced Convection

θ_{JA} (°C/W) vs. Air Flow (m/s)			
Meters per Second	**0**	**1**	**2**
40-Lead VFQFN Multi-Layer PCB, JEDEC Standard Test Boards	24.6	21.2	19.6

Reliability Information

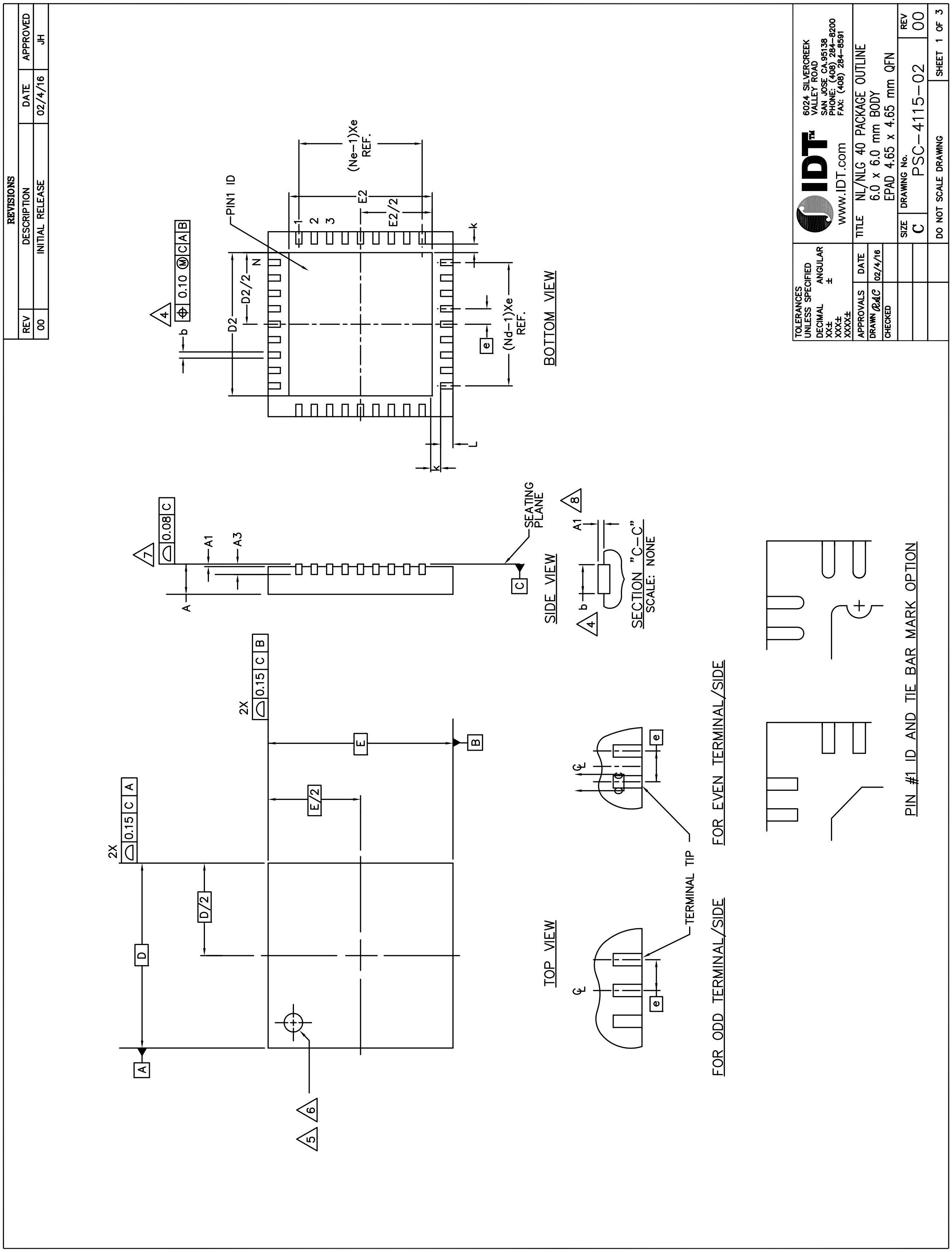
Table 7. Thermal Resistance θ_{JA} for 40-Lead VFQFN vs. Forced Convection

θ_{JA} (°C/W) vs. Air Flow (m/s)			
Meters per Second	**0**	**1**	**2**
40-Lead VFQFN Multi-Layer PCB, JEDEC Standard Test Boards	24.6	21.2	19.6

Transistor Count

The transistor count for 8P34S2106 is: 1113

40-Lead VFQFN Package Outline and Package Dimensions



40-Lead VFQFN Package Outline and Package Dimensions

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	02/4/16	JH

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. (△) DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. (△) THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. (△) EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. (△) APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. (△) APPLIED ONLY FOR TERMINALS.
9. THIS OUTLINES CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–220, VARIATION VJJC–3 & VJJD–5 WITH THE EXCEPTION OF D2 & E2.

SYMBOL	DIMENSION MIN	DIMENSION NOM	DIMENSION MAX	NOTE
b	0.18	0.25	0.30	4
D		6.00 BSC		
E		6.00 BSC		
D2	4.50	4.65	4.75	
E2	4.50	4.65	4.75	
L	0.30	0.40	0.50	
e		0.50 BSC		
k		0.275 REF.		2
N		40		2
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	7
A3		0.2 REF		
Nd		10		2
Ne		10		2

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX± ANGULAR ±

APPROVALS	DATE
DRAWN RAC	02/4/16
CHECKED	

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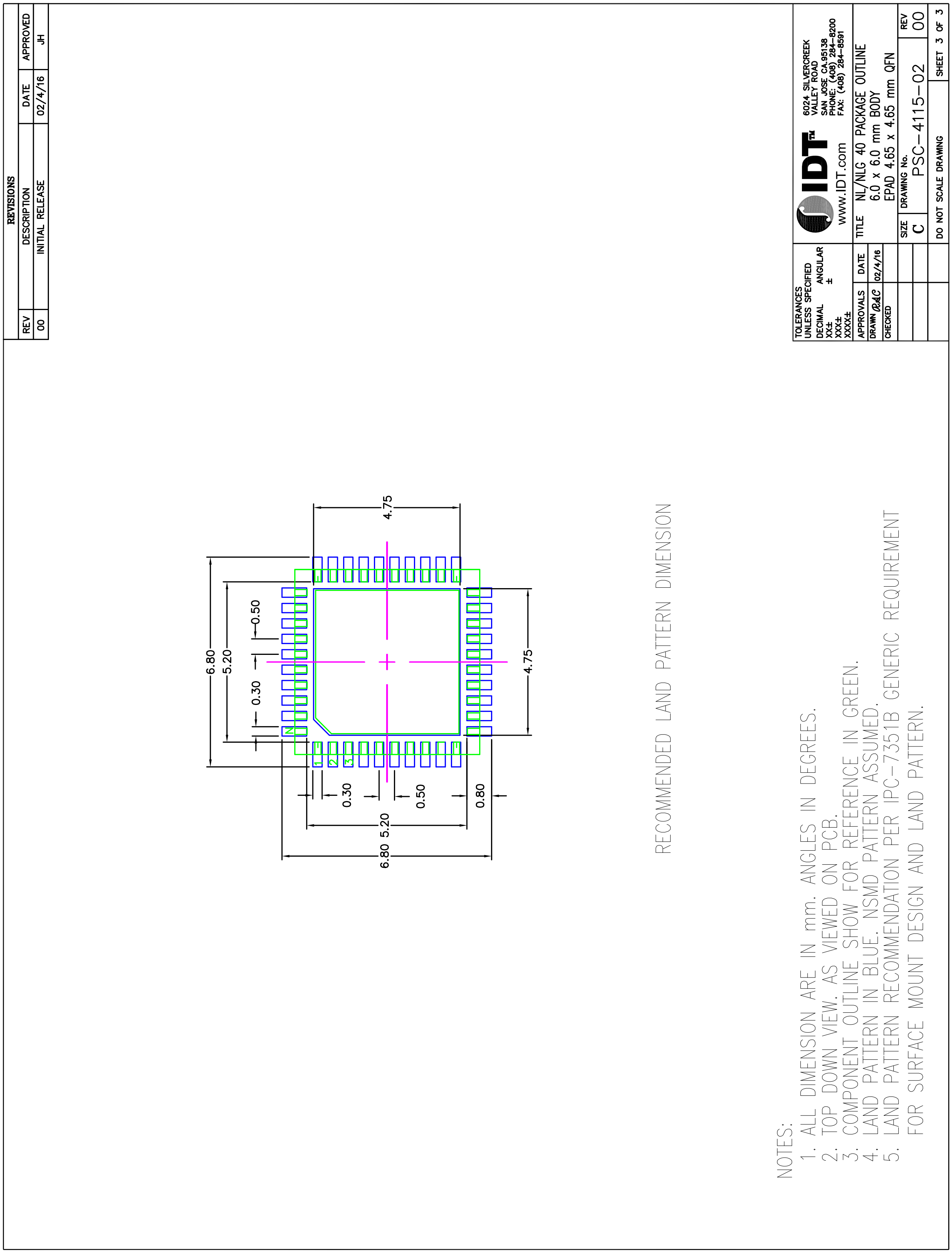
TITLE: NL/NLG 40 PACKAGE OUTLINE 6.0 x 6.0 mm BODY EPAD 4.65 x 4.65 mm QFN

SIZE: C | DRAWING No.: PSC–4115–02 | REV: 00

DO NOT SCALE DRAWING | SHEET 2 OF 3

40-Lead VFQFN Package Outline and Package Dimensions

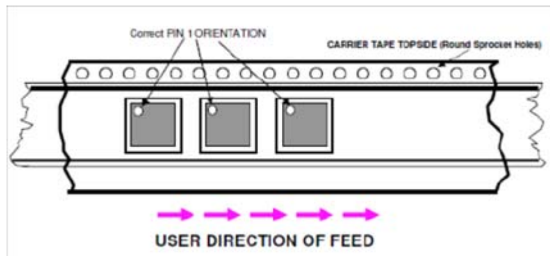
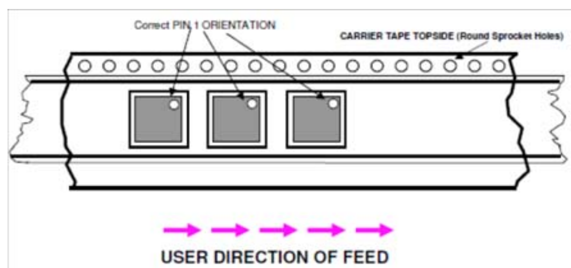


Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8P34S2106NLGI	IDT8P34S2106NLGI	40-Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
8P34S2106NLGI8	IDT8P34S2106NLGI		Tape & Reel, Pin 1 Orientation: EIA-481-C	
8P34S2106NLGI/W	IDT8P34S2106NLGI		Tape & Reel, Pin 1 Orientation: EIA-481-D/E	

Table 9. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D/E)	

Revision History Sheet

Table	Page	Description of Change	Date
	1	Features section - corrected phase jitter bullet spec from <50fs to 45fs.	7/28/16
		Initial Final Datasheet	7/8/16

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