Octal 2:1 and 1:2 Differential-to-LVDS Multiplexer

ICS854S54I-08

DATA SHEET

General Description

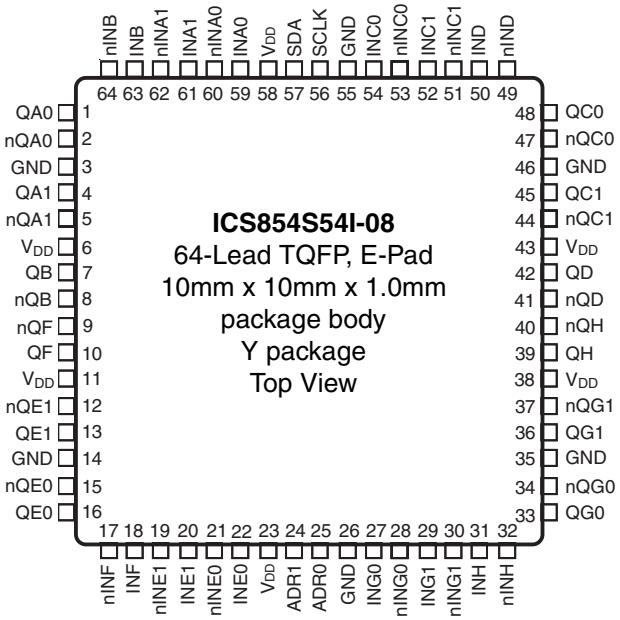
The ICS854S54I-08 is an octal 2:1 and 1:2 Multiplexer. The device contains four individually controlled banks of LVDS outputs. The 2:1 Multiplexer allows one of 2 inputs to be selected onto one output pin and the 1:2 MUX switches one input to one of two outputs. This device is useful for multiplexing multi-rate Ethernet PHYs which have 100M bit and 1000M bit transmit/receive pairs onto an optical SFP module which has a single transmit/receive pair. See Application Section for further information.

The ICS854S54I-08 is optimized for ATCA backplane swtich applications requiring very high performance and has a maximum operating frequency of 1.3GHz. The device is packaged in a small, 10mm x 10mm TQFP package, making it ideal for use on space-constrained boards.

Features

- Four banks of three LVDS output pairs
- Twelve differential data intputs
- Serial 1^2C Interface
- Data pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 1.3GHz
- Propagation delay: 1ns (maximum)
- Additive phase jitter, RMS: 0.066ps (typical)
- Part-to-part skew: 475ps (maximum)
- Full 3.3V supply voltage
- Available in both standard (R0HS 5) and lead-free (RoHS 6) packages
- -40°C to 85°C ambient operating temperature

Pin Assignment



Block Diagram

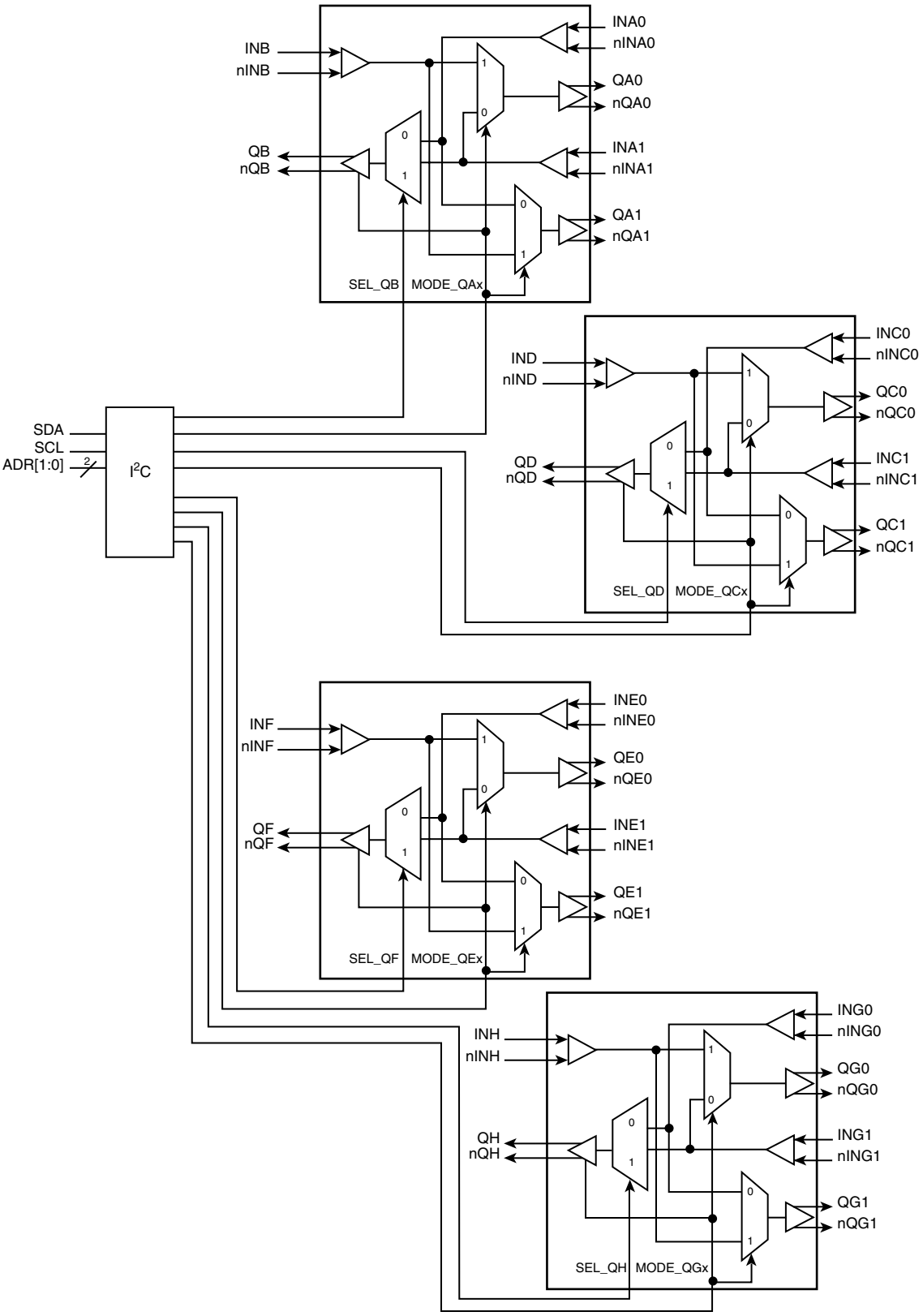


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2 4, 5	QA0, nQA0 QA1, nQA1	Output		Differential output pair. LVDS interface levels.
3, 14, 26, 35, 46, 55	GND	Power		Power supply ground.
6, 11, 23, 38, 43, 58	V_{DD}	Power		Power supply pins.
7, 8	QB, nQB	Output		Differential output pair. LVDS interface levels.
9, 10	nQF, QF	Output		Differential output pair. LVDS interface levels.
12, 13 15, 16	nQE1, QE1 nQE0, QE0	Output		Differential output pair. LVDS interface levels.
17	nINF	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{DD}/2 default when left floating.
18	INF	Input	Pulldown	Non-inverting differential LVPECL clock input.
19, 21	nINE1, nINE0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{DD}/2 default when left floating.
20, 22	INE1, INE0	Input	Pulldown	Non-inverting differential LVPECL clock input.
24, 25	ADR1, ADR0	Input	Pulldown	Serial address select pins. LVCMOS / LVTTL interface levels.
27, 29	ING0, ING1	Input	Pulldown	Non-inverting differential LVPECL clock input.
28, 30	nING0, nING1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{DD}/2 default when left floating.
31	INH	Input	Pulldown	Non-inverting differential LVPECL clock input.
32	nINH	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{DD}/2 default when left floating.
33, 34 36, 37	QG0, nQG0 QG1, nQG1	Output		Differential output pair. LVDS interface levels.
39, 40	QH, nQH	Output		Differential output pair. LVDS interface levels.
41, 42	nQD, QD	Output		Differential output pair. LVDS interface levels.
44, 45 47, 48	nQC1, QC1 nQC0, QC0	Output		Differential output pair. LVDS interface levels.
49	nIND	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{DD}/2 default when left floating.
50	IND	Input	Pulldown	Non-inverting differential LVPECL clock input.
51, 53	nINC1, nINC0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{DD}/2 default when left floating.
52, 54	INC1, INC0	Input	Pulldown	Non-inverting differential LVPECL clock input.
56	SCLK	Input	Pullup	I^2C Serial address select pin. LVCMOS/LVTTL interface levels.
57	SDA	Input	Pullup	I^2C Shift register serial input. Data sampled on the rising edge of SCLK. LVCMOS/LVTTL interface levels.
59, 61	INA0, INA1	Input	Pulldown	Non-inverting differential LVPECL clock input.
60, 62	nINA0, nINA1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{DD}/2 default when left floating.
63	INB	Input	Pulldown	Non-inverting differential LVPECL clock input.
64	nINB	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{DD}/2 default when left floating.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			50		kΩ
R_{PULLUP}	Input Pullup Resistor			50		kΩ
$R_{VDD/2}$	Pullup/Pulldown Resistors			50		kΩ

Function Tables

Table 3A. Internal Control Input Function Table, SEL_QB, MODE_QAx

I^2C Bits		Outputs		
SEL_QB	MODE_QAx	QB, nQB	QA0, nQA0	QA1, nQA1
0	1	Follows INA0, nINA0 input	Follows INB, nINB input	Follows INB, nINB input
1	1	Follows INA1, nINA1 input	Follows INB, nINB input	Follows INB, nINB input
X	0	High-Impedance	Follows INA1, nINA1 input	Follows INA0, nINA0 input

Table 3B. Internal Control Input Function Table, SEL_QD, MODE_QCx

I^2C Bits		Outputs		
SEL_QD	MODE_QCx	QB, nQB	QA0, nQA0	QA1, nQA1
0	1	Follows INC0, nINC0 input	Follows IND, nIND input	Follows IND, nIND input
1	1	Follows INC1, nINC1 input	Follows IND, nIND input	Follows IND, nIND input
X	0	High-Impedance	Follows INC1, nINC1 input	Follows INC0, nINC0 input

Table 3C. Internal Control Input Function Table, SEL_QF, MODE_QEx

I^2C Bits		Outputs		
SEL_QF	MODE_QEx	QB, nQB	QA0, nQA0	QA1, nQA1
0	1	Follows INE0, nINE0 input	Follows INF, nINF input	Follows INF, nINF input
1	1	Follows INE1, nINE1 input	Follows INF, nINF input	Follows INF, nINF input
X	0	High-Impedance	Follows INE1, nINE1 input	Follows INE0, nINE0 input

Table 3D. Internal Control Input Function Table, SEL_QH, MODE_QGx

I^2C Bits		Outputs		
SEL_QH	MODE_QGx	QB, nQB	QA0, nQA0	QA1, nQA1
0	1	Follows ING0, nING0 input	Follows INH, nINH input	Follows INH, nINH input
1	1	Follows ING1, nING1 input	Follows INH, nINH input	Follows INH, nINH input
X	0	High-Impedance	Follows ING1, nING1 input	Follows ING0, nING0 input

I²C Control Description

The ICS854S54I-08 uses an industry standard I²C interface to control the direction of the 4 separate 2:1, 1:2 mux switch blocks. Each individual block is controlled by two bits of the 8 bit Data Byte. The Data Byte bit pairs are summarized as follows:

Control Signals

Bit Pair 1 – INA0/nINA0, INA1/nINA1, INB/nINB, QB/nQB
SEL_QB:MODE_QAx

Bit Pair 2 – INC0/nINC0, INC1/nINC1, IND/nIND, QD/nQD
SEL_QD:MODE_QCx

Bit Pair 3 – INE0/nINE0, INE1/nINE1, INF/nINF, QF/nQF
SEL_QF:MODE_QEx

Bit Pair 4 – ING0/nING0, ING1/nING1, INH/nINH, QH/nQH
SEL_QH:MODE_QGx

Data Byte 0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control Bit	MODE_QGx	SEL_QH	MODE_QEx	SEL_QF	MODE_QCx	SEL_QD	MODE_QAx	SEL_QB
Power-up Default Value	1	0	1	0	1	0	1	0

I²C Addressing

The ICS854S54I-08 can be set to decode one of four addresses to minimize the chance of address conflict on the I²C bus. The address that is decoded is controlled by the setting of the ADR_1, ADR_0 (pins 24 and 25).

ADR_SEL (pins 24 & 25) = Default (1, 1)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	0	1	1	1	1	R/W

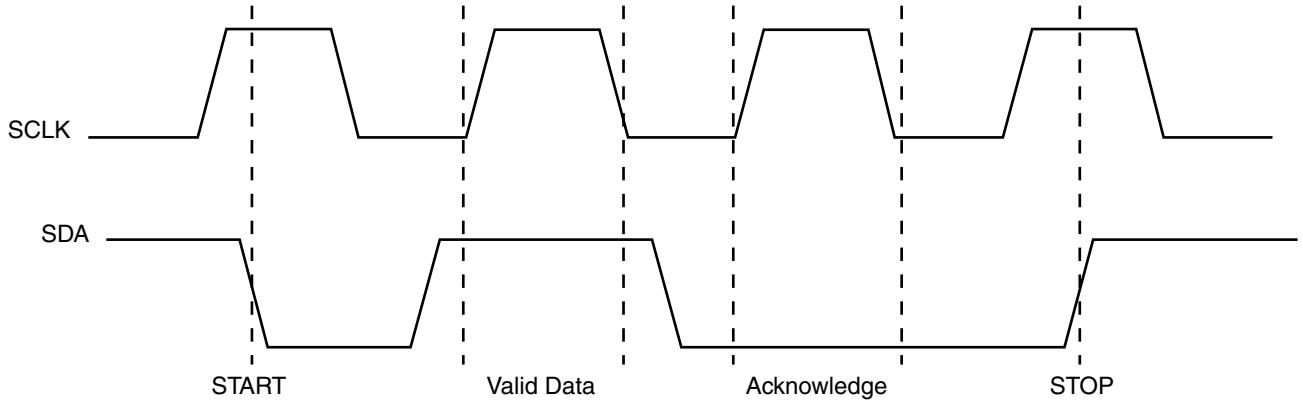
ADR_SEL (pins 24 & 25) = Default (1, 0)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	0	1	1	1	0	R/W

ADR_SEL (pins 24 & 25) = Default (0, 1)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	0	1	1	0	1	R/W

ADR_SEL (pins 24 & 25) = Default (0, 0)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	0	1	1	0	0	R/W

SECURE I²C INTERFACE - PROTOCOL

The ICS854S54I-08 is a slave-only device and uses the standard I²C protocol as shown in the below diagrams. The maximum SCLK frequency is greater than 400kHz which is more than sufficient for standard I²C clock speeds.



START (ST) – Defined as high-to-low transition on SDA while holding SCLK HIGH.

DATA – Between START and STOP cycles, SDA is synchronous with SCLK.
Data may change only when SCLK is LOW and must be stable when SCLK is HIGH.

ACKNOWLEDGE (AK) – SDA is driven LOW before the SCLK rising edge and held LOW until the SCLK falling edge.

STOP (SP) – defined as low-to-high transition on SDA while holding SCLK HIGH.

Serial Interface – A Write Example

A serial transfer to the ICS854S54I-08 always consists of an address cycle followed by a single data byte. Any additional data bytes will not be acknowledged and the ICS854S54I-08 will leave the data bus HIGH. These extra bits will not be loaded into the serial control register. Once the Data Byte is loaded and the master generates a stop condition, the values in the serial control register are latched into the mux control bit outputs and each mux will switch into the new state.

ST	Slave Address: 7 Bits	R/W	AK
1 Bit	Refer to page 5 for address choices based on ADDR_SEl pin setting	1 Bit	1 Bit

Data Byte 0: 8 Bits								AK	SP
MODE_QGx	SEL_QH	MODE_QEx	SEL_QF	MODE_QCx	SEL_QD	MODE_QAx	SEL_QB	1 Bit	1 Bit

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}	25.6°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				392	mA

Table 4B. LVCMOS/LVTTL Input DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SDA, SCLK	$V_{DD} = V_{IN}$ = 3.465V			10	µA
		ADR0, ADR1	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	SDA, SCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		ADR0, ADR1	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	INA[0:1], INB, INC[0:1], IND, INE[0:1], INF, ING[0:1], INH	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nINA[0:1], nINB, INC[0:1], nIND, nINE[0:1], nINF, nING[0:1], nINH	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	INA[0:1], INB, INC[0:1], IND, INE[0:1], INF, ING[0:1], INH	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nINA[0:1], nINB, INC[0:1], nIND, nINE[0:1], nINF, nING[0:1], nINH	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage: NOTE 1, 2			1.2		V_{DD}	V

NOTE 1: V_{IL} cannot be less than -0.3V.
NOTE 2: Common mode voltage is define as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		325	425	525	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.25	1.35	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

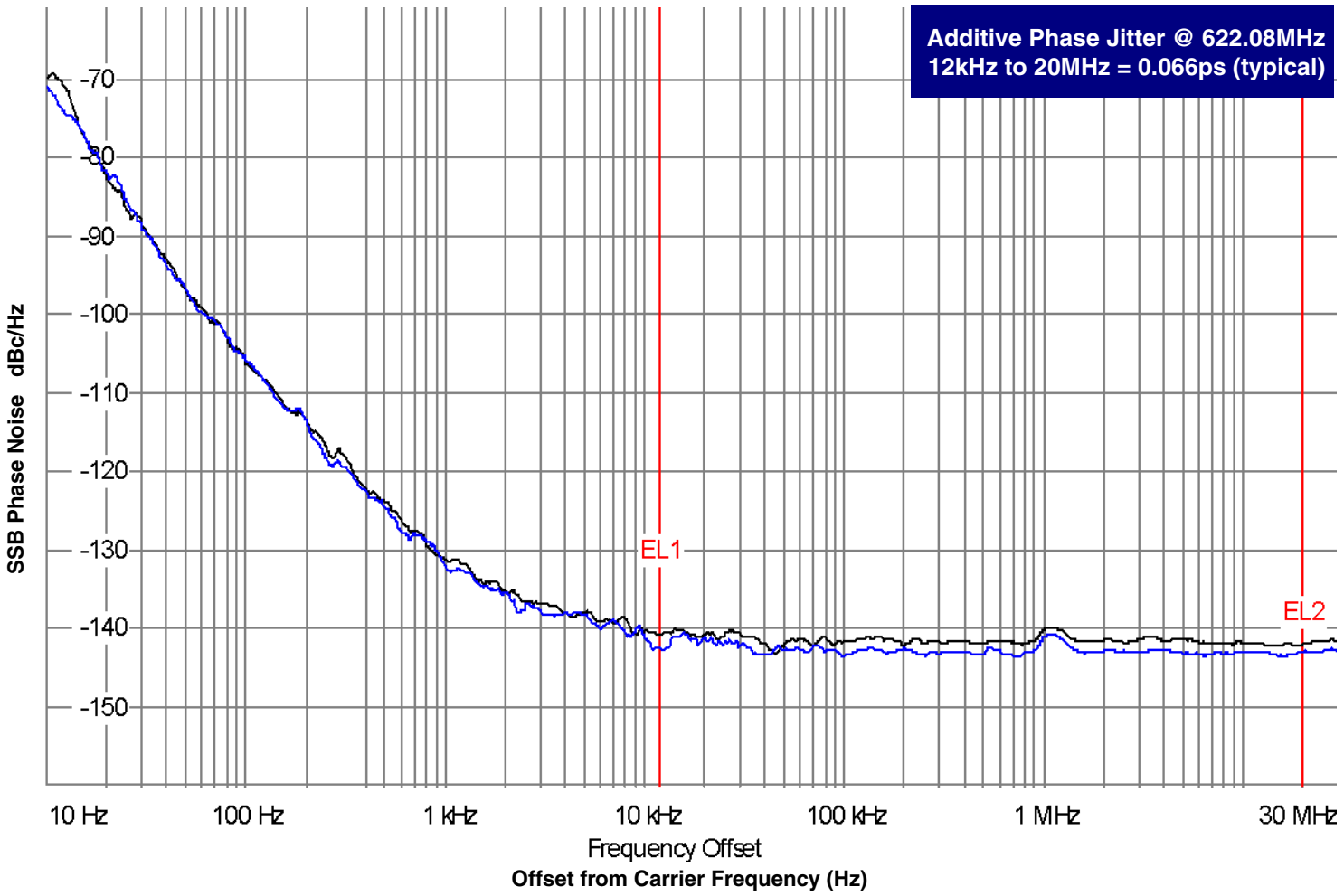
Table 5. AC Electrical Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					1.3	GHz
t_{PD}	Propagation Delay; NOTE 1	All Outputs		0.525		1.0	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section		622.08MHz, Integration Range: 12kHz – 20MHz		0.066		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					475	ps
$MUX_{ISOLATION}$	MUX Isolation; NOTE 4				45		dB
t_R / t_F	Output Rise/ Fall Time		20% to 80%	50		385	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Measured using standard LVDS input at 622MHz.

Additive Phase Jitter

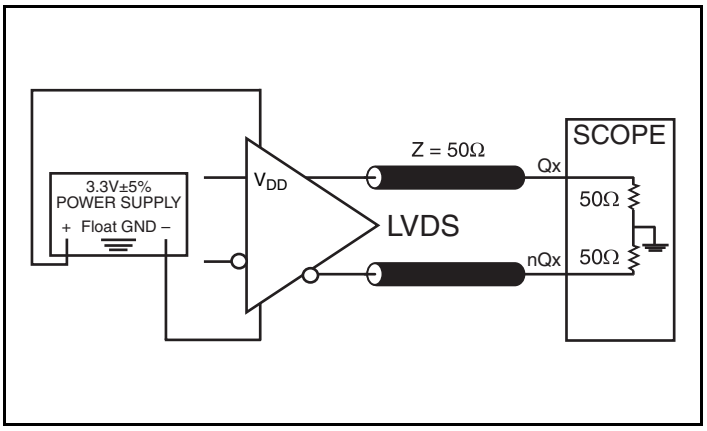
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



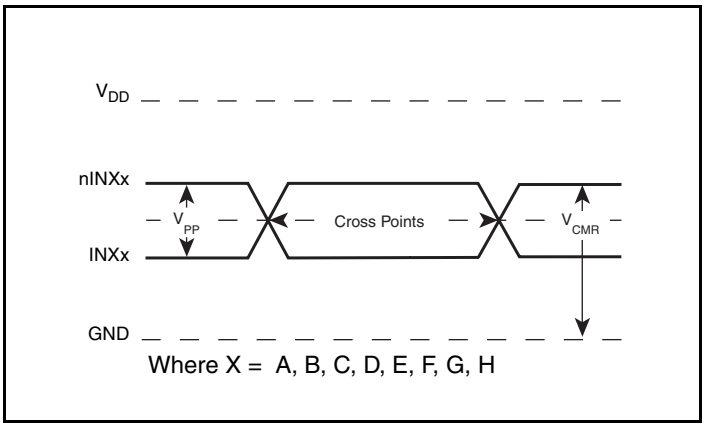
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator "IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator".

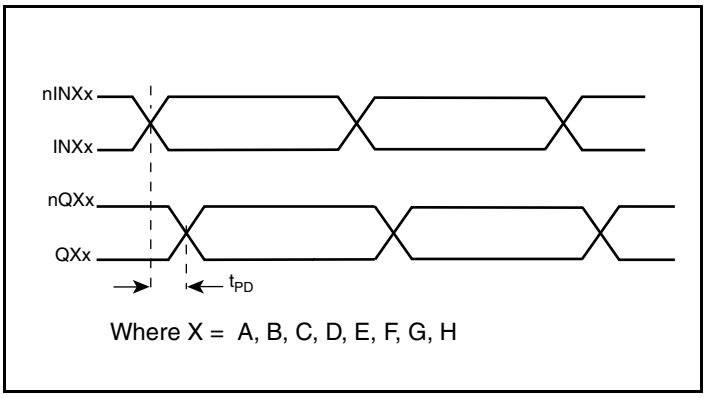
Parameter Measurement Information



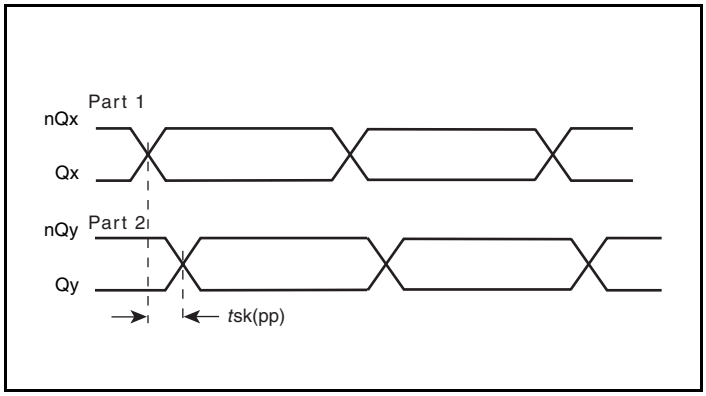
Output Load AC Test Circuit



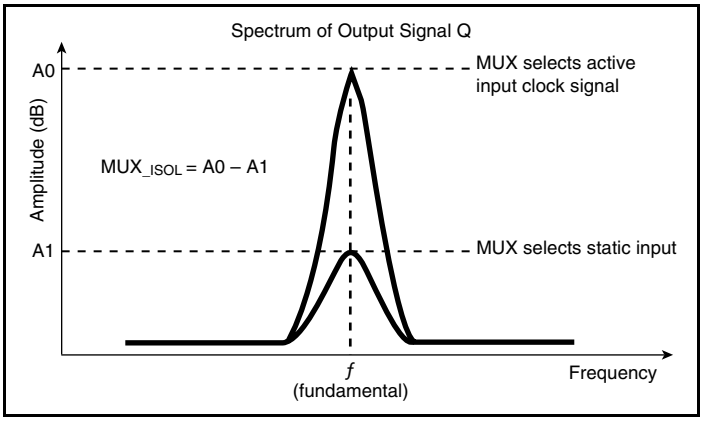
Differential Input Levels



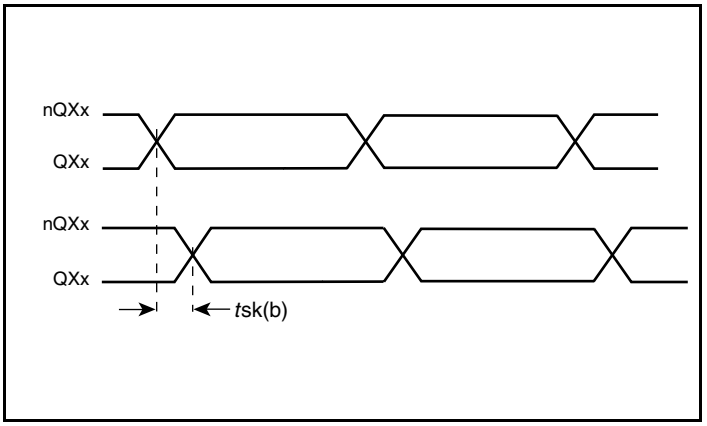
Propagation Delay



Part-to-Part Skew

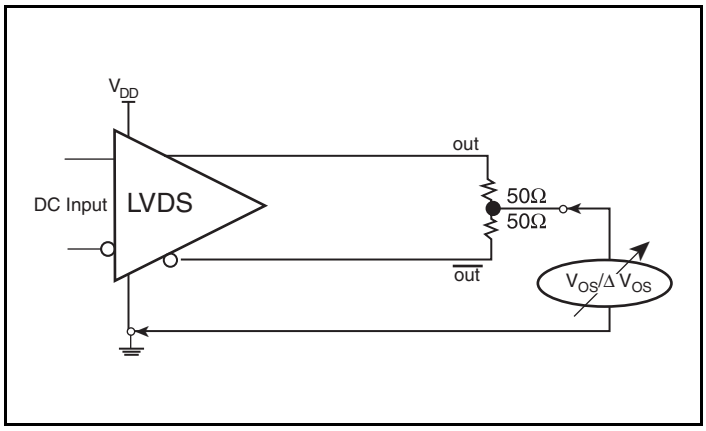


MUX Isolation

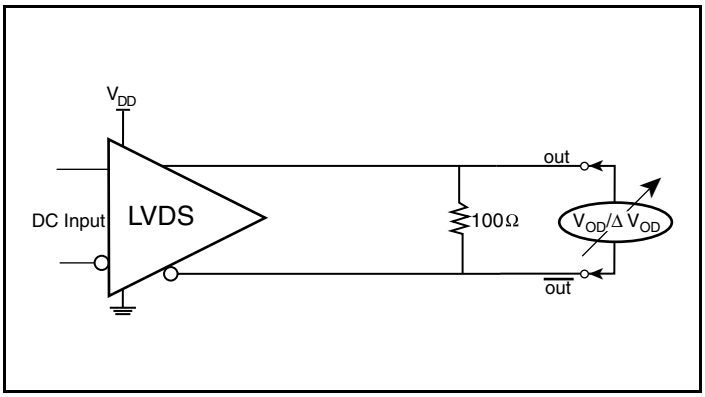


Output Rise/Fall Time

Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

IN/nIN Inputs

For applications not requiring the use of a differential input, both the IN and nIN pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from IN to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

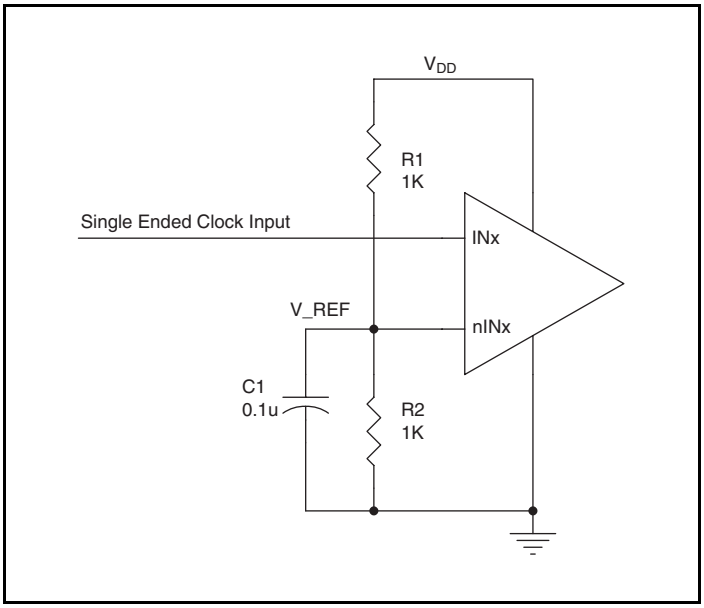


Figure 1. Single-Ended Signal Driving Differential Input

LVPECL Differential Clock Input Interface

The IN /nIN accepts LVPECL, CML, LVDS and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2D* show interface examples for the IN /nIN input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

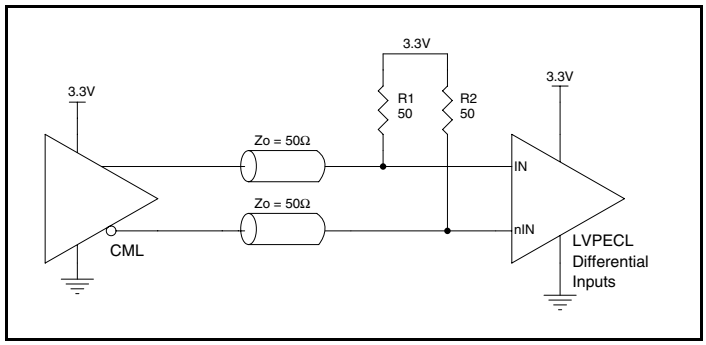


Figure 2A. IN/nIN Input Driven by an Open Collector CML Driver

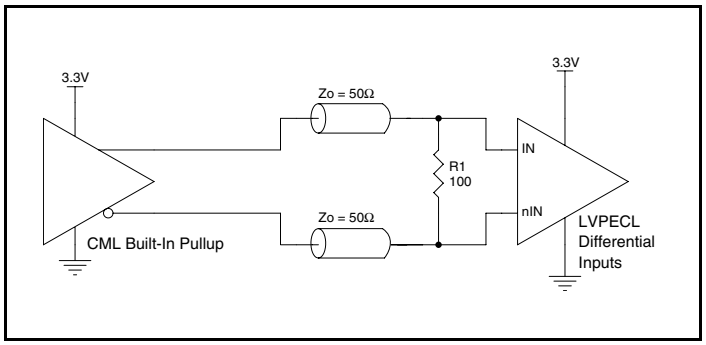


Figure 2B. IN/nIN Input Driven by a Built-In Pullup CML Driver

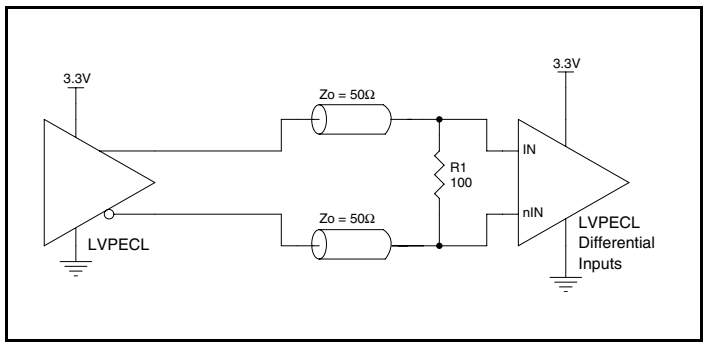


Figure 2C. HiPerClockS IN/nIN Input Driven by a 3.3V LVPECL Driver

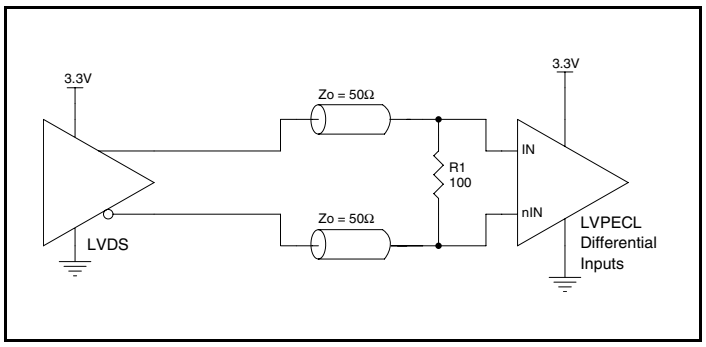


Figure 2D. IN/nIN Input Driven by a 3.3V LVDS Driver

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

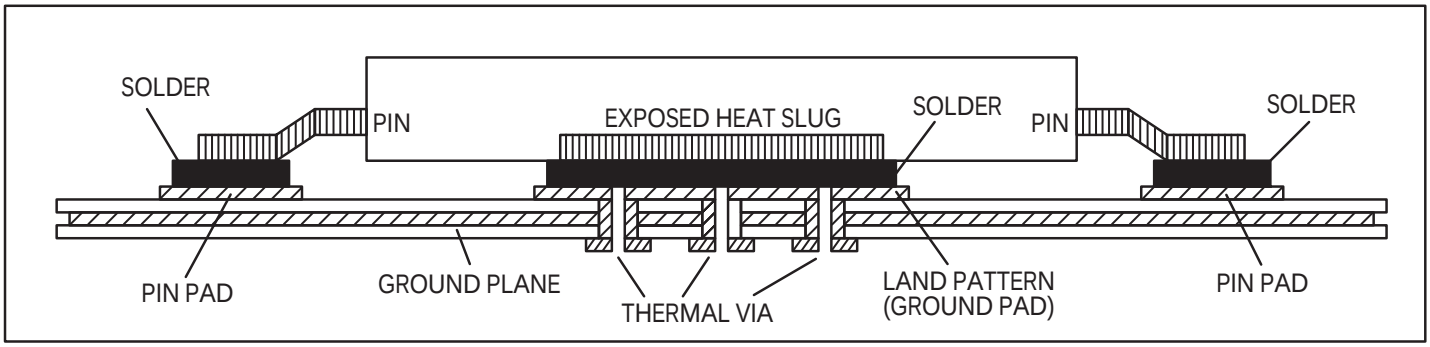


Figure 3. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

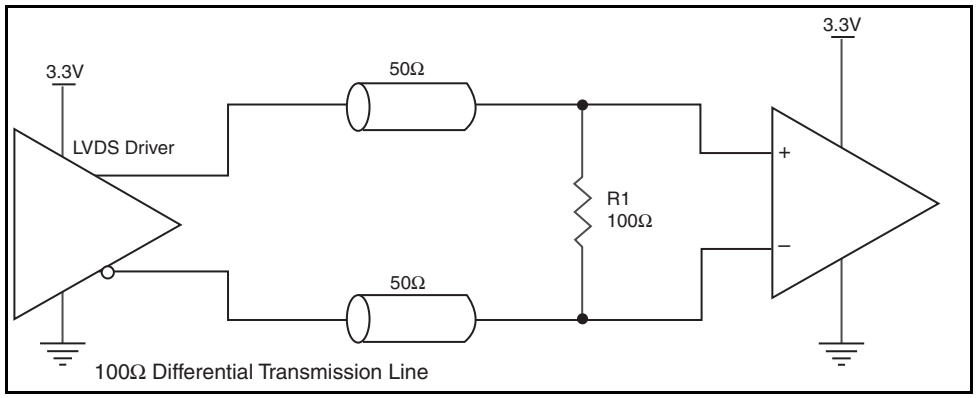
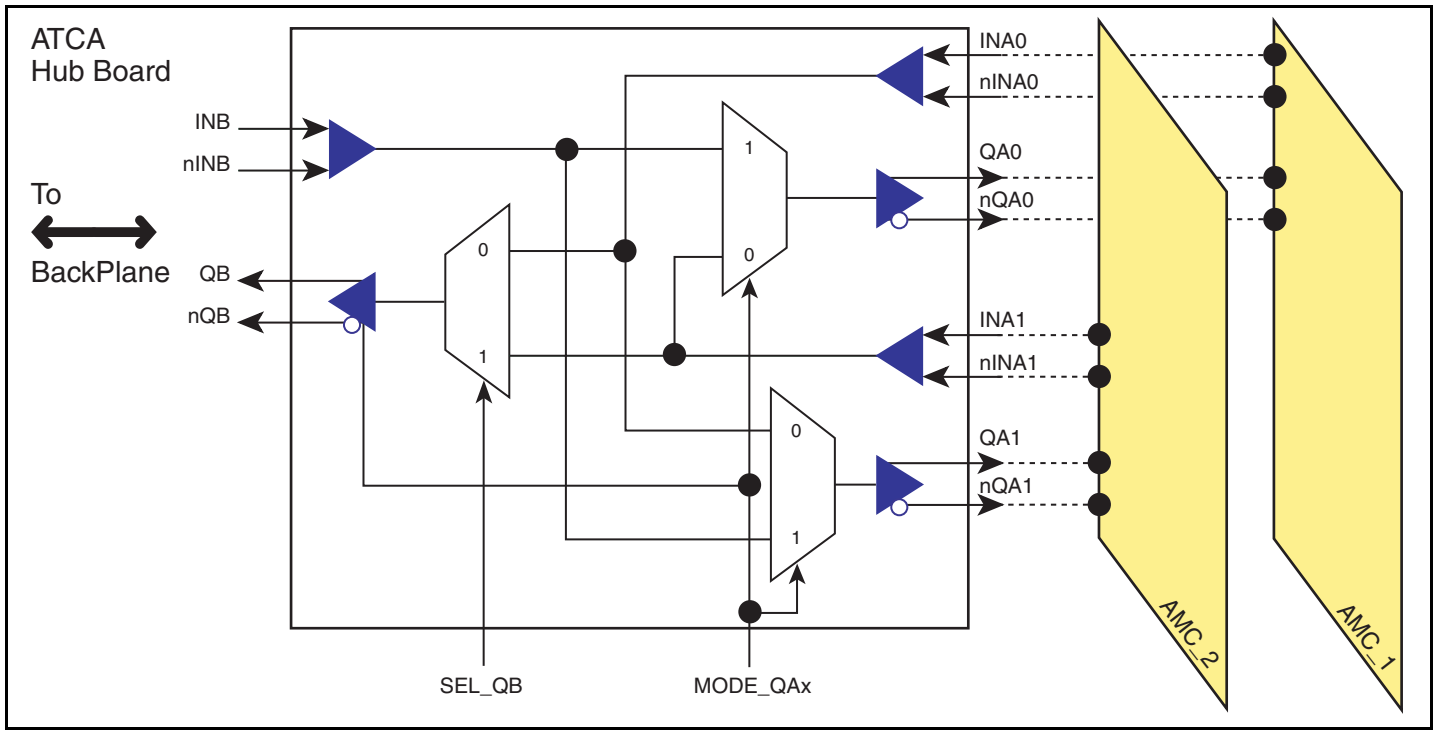


Figure 4. Typical LVDS Driver Termination

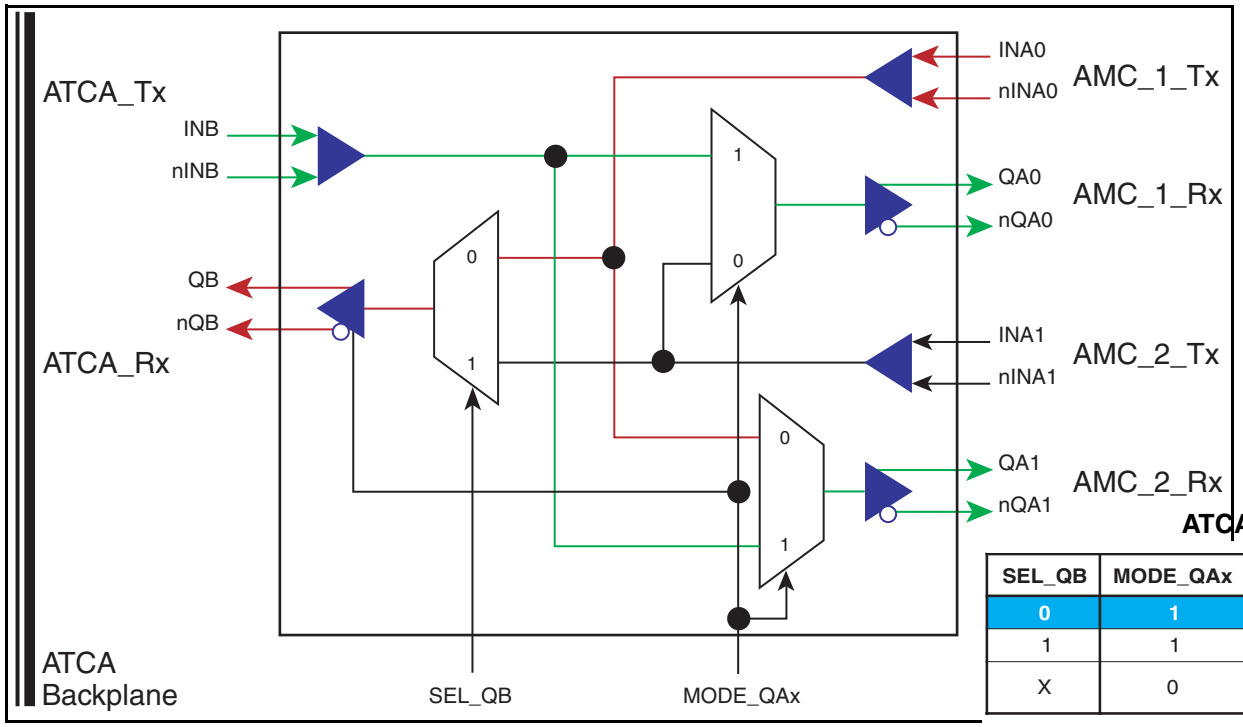
A Typical Application Using One Bank of the ICS854S54I-08

Used to connect Advanced Mezzanine Cards to ATCA Backplane.
Also provdes ability to cross connect individual AMC's to each other.
Problem Addressed: How to allow communication between AMC cards while backplane channels are disabled.



Mode 1 (SEL_QB = 0, MODE_QAx = 1), AMC_1 to ATCA Backplane Communication

ATCA Tx (INB, nINB) connected to (QA0/nQA0, QA1/nQA1) AMC_1_Rx and AMC_2_Rx respectively.
ATCA_Rx (QB, nQB) connected to AMC_1, Tx (INA0, nINA0).

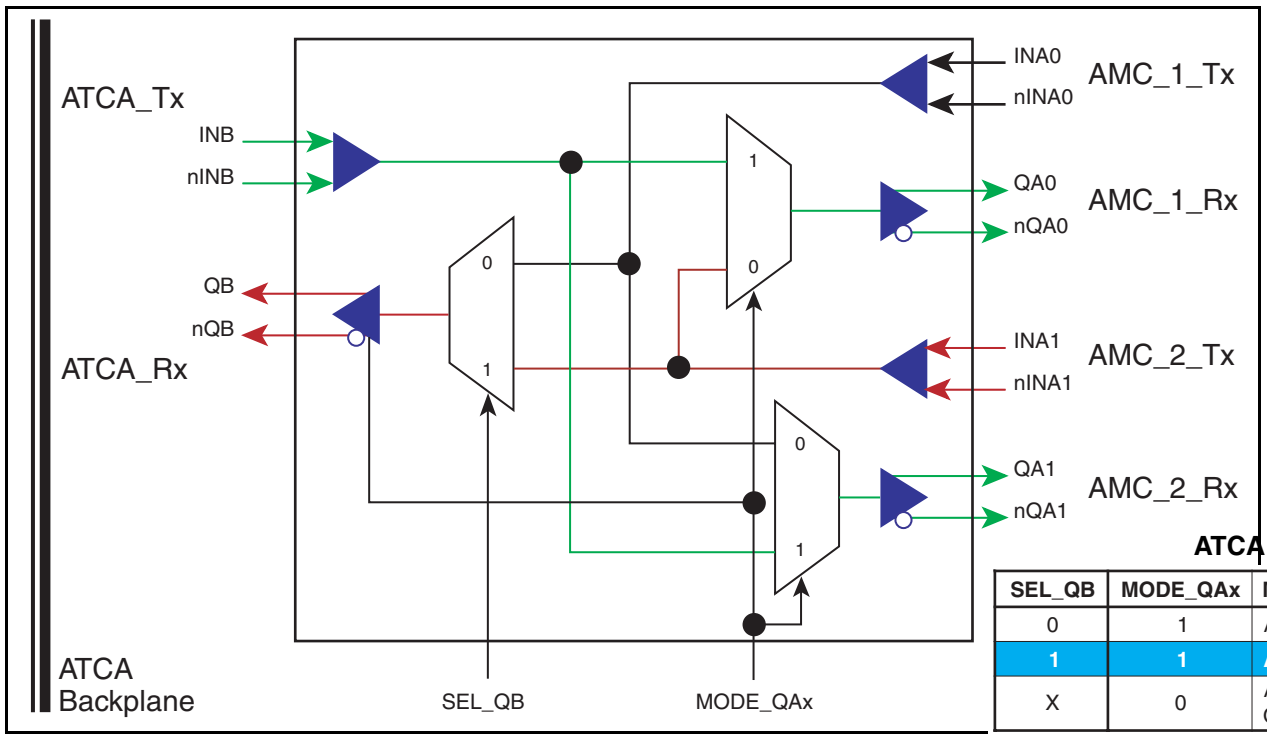


ATCA Communication Path

SEL_QB	MODE_QAx	Mode Selected
0	1	AMC1 selected
1	1	AMC2 selected
X	0	AMC1 & AMC2 connected, QB/nQB = Hi-Z

Mode 2 (SEL_QB = 1, MODE_QAx = 1), AMC_2 to ATCA Backplane Communication

TCA Tx (INB, nINB) connected to (QA0/nQA0, QA1/nQA1) AMC_1_Rx and AMC_2_Rx respectively.
ATCA_Rx (QB, nQB) connected to AMC_2, Tx (INA1, nINA1).

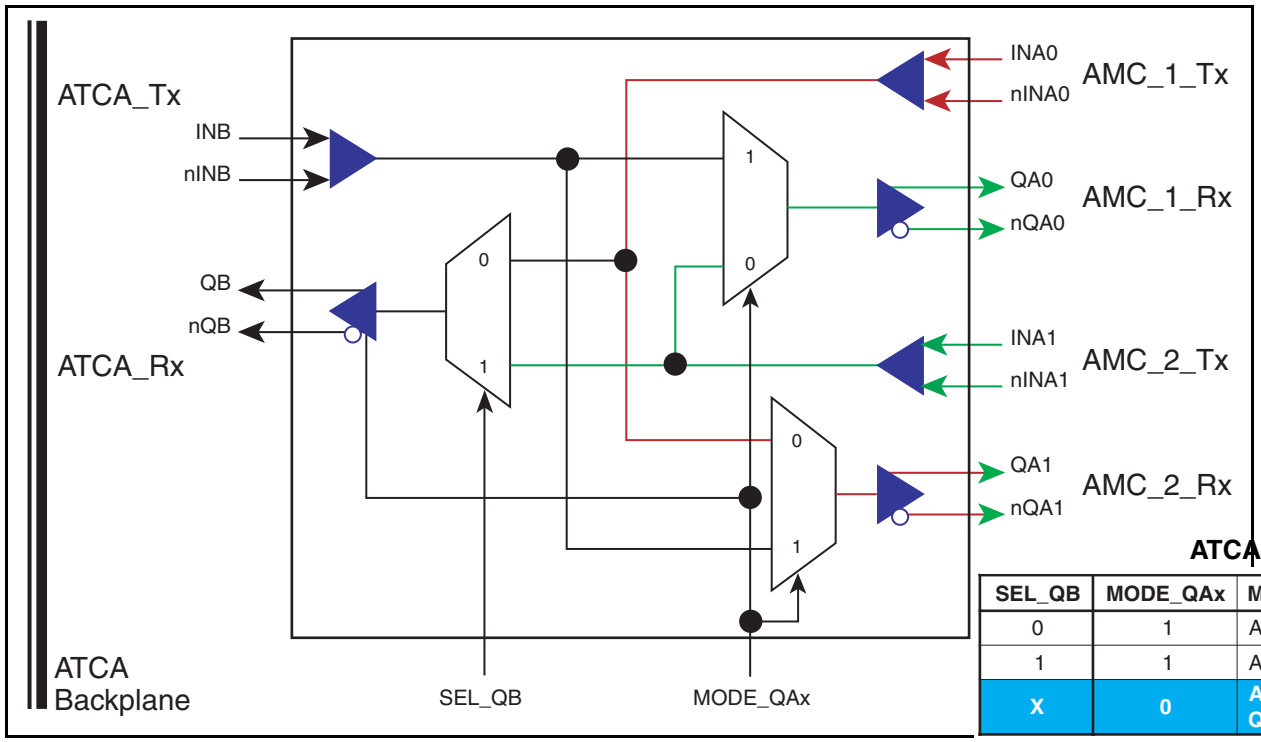


ATCA Communication Path

SEL_QB	MODE_QAx	Mode Selected
0	1	AMC1 selected
1	**1**	**AMC2 selected**
X	0	AMC1 & AMC2 connected, QB/nQB = Hi-Z

Mode 3 (SEL_QB = X, MODE_QAx = 0), AMC_1 to AMC_2 Communication

ATCA_Rx disabled: (QB and nQB = Hi-Z) AMC_1 Tx (INA0, nINA0) connected to AMC_2 Rx (QA1, nQA1),
AMC_2 Tx (INA1, nINA1) connected to AMC_1 Rx (QA0, nQA0).



ATCA Communication Path

SEL_QB	MODE_QAx	Mode Selected
0	1	AMC1 selected
1	1	AMC2 selected
X	**0**	**AMC1 & AMC2 connected, QB/nQB = Hi-Z**

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS854S54I-08.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS854S54I-08 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 365mA = **1264.725mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 25.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.265W * 25.6°C/W = 117.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 64 Lead TQFP, E-Pad Forced Convection

θ_{JA} **by Velocity**	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	25.6°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 64 Lead TQFP, E-Pad

θ_{JA} vs. Air Flow	
Meters per Second	**0**
Multi-Layer PCB, JEDEC Standard Test Boards	25.6°C/W

Transistor Count

The transistor count for ICS854S54I-08 is: 6233

Package Outline and Package Dimensions

Package Outline - Y Suffix for 64 Lead TQFP, E-Pad

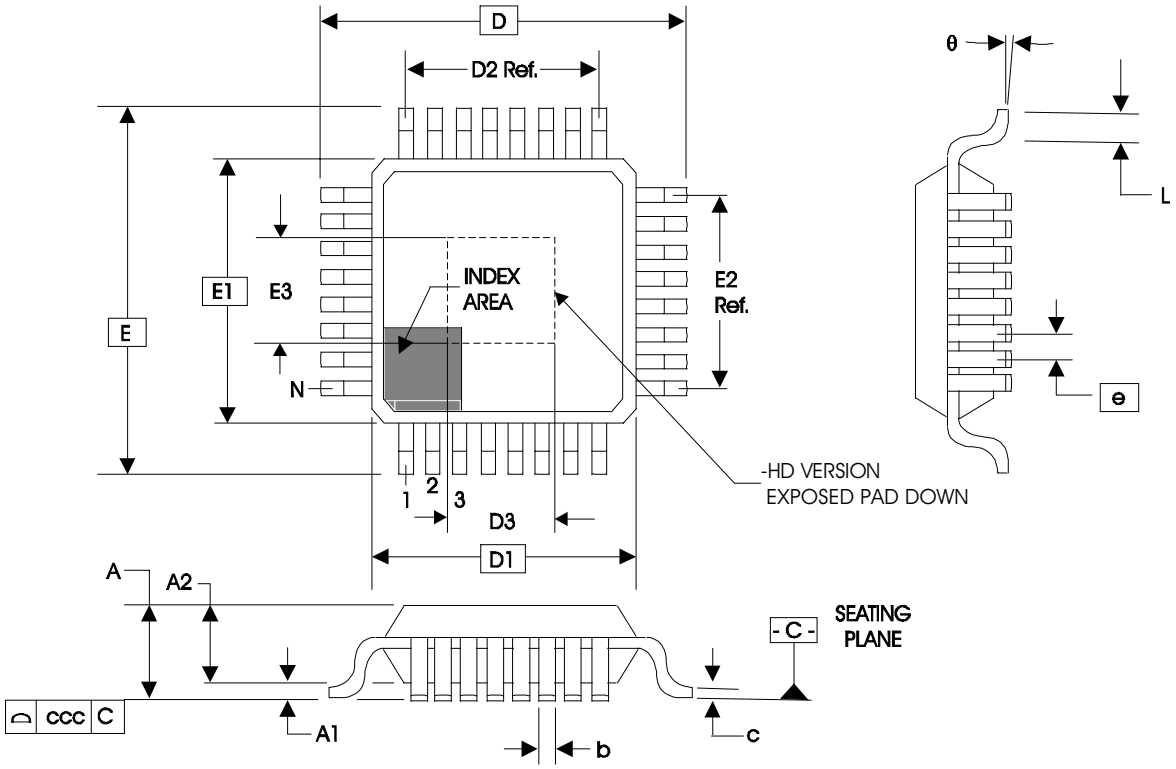


Table 8. Package Dimensions for 64 Lead TQFP, E-Pad

JEDEC Variation: ACD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		64	
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09		0.20
D & E		12.00 Basic	
D1 & E1		10.00 Basic	
D2 & E2		7.50 Ref.	
D3 & E3	4.5		5.5
e		0.50 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854S54AYI-08	ICS854S54AYI08	Lead-Free, 64 Lead TQFP, E-Pad	Tray	-40°C to 85°C
854S54AYI-08T	ICS854S54AYI08	Lead-Free, 64 Lead TQFP, E-Pad	500 Tape & Reel	-40°C to 85°C
854S54AYI-08LF	ICS854S54AI08L	Lead-Free, 64 Lead TQFP, E-Pad	Tray	-40°C to 85°C
854S54AYI-08LF	ICS854S54AI08L	Lead-Free, 64 Lead TQFP, E-Pad	500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056