# ICS843011
## FEMTOCLOCKS™ CRYSTAL-TO- 3.3V LVPECL CLOCK GENERATOR

## GENERAL DESCRIPTION

The ICS843011 is a Fibre Channel Clock Generator. The ICS843011 uses a 26.5625MHz crystal to synthesize 106.25MHz or a 25MHz crystal to synthesize 100MHz. The ICS843011 has excellent <1ps phase jitter performance, over the 637kHz – 10MHz integration range. The ICS843011 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

## FEATURES

- One differential 3.3V LVPECL output

- Crystal oscillator interface designed for 26.5625MHz 18pF parallel resonant crystal

- Output frequency: 106.25MHz or 100MHz

- VCO range: 560MHz - 680MHz

- RMS phase jitter @ 100MHz, using a 25MHz crystal (637kHz - 10MHz): 0.80ps (typical)
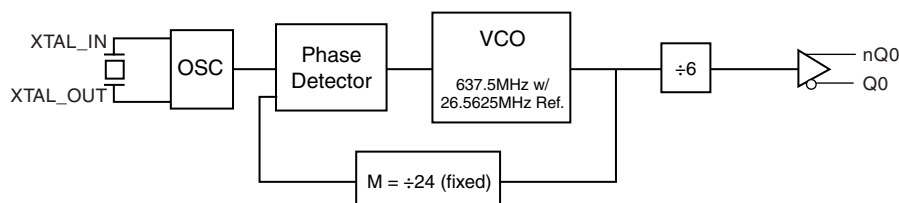
- RMS phase noise at 106.25MHz

  Phase noise:

  | Offset | Noise Power |
  |--------|-------------|
  | 100Hz | -92.8 dBc/Hz |
  | 1kHz | -119.6 dBc/Hz |
  | 10kHz | -129.5 dBc/Hz |
  | 100kHz | -130.5 dBc/Hz |

- 3.3V operating supply

- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

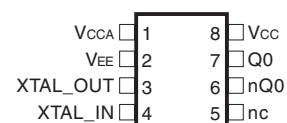- -40°C to 85°C ambient operating temperature

### FREQUENCY TABLE

| Crystal (MHz) | Output Frequency (MHz) |
|---------------|------------------------|
| 26.5625 | 106.25 |
| 25 | 100 |

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**ICS843011**
**8-Lead TSSOP**
4.40mm x 3.0mm x 0.925mm package body
**G Package**
Top View

### TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|------|------|---|-------------|
| 1 | $V_{CCA}$ | Power | | Analog supply pin. |
| 2 | $V_{EE}$ | Power | | Negative supply pin. |
| 3, 4 | XTAL_OUT, XTAL_IN | Input | | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| 5 | nc | Unused | | No connect. |
| 6, 7 | nQ0, Q0 | Output | | Differential clock outputs. LVPECL interface levels. |
| 8 | $V_{CC}$ | Power | | Core supply pin. |

### TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$      4.6V

Inputs, $V_I$      -0.5V to $V_{CC}$ + 0.5V

Outputs, $I_O$
  Continuous Current      50mA
  Surge Current      100mA

Package Thermal Impedance, $\theta_{JA}$      101.7°C/W (0 mps)

Storage Temperature, $T_{STG}$      -65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC}$ = 3.3V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{CCA}$ | Analog Supply Current | included in $I_{EE}$ | | | 12 | mA |
| $I_{EE}$ | Power Supply Current | | | | 93 | mA |

### TABLE 3B. LVPECL DC CHARACTERISTICS, $V_{CC}$ = 3.3V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CC}$ - 1.4 | | $V_{CC}$ - 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CC}$ - 2.0 | | $V_{CC}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CC}$ - 2V.
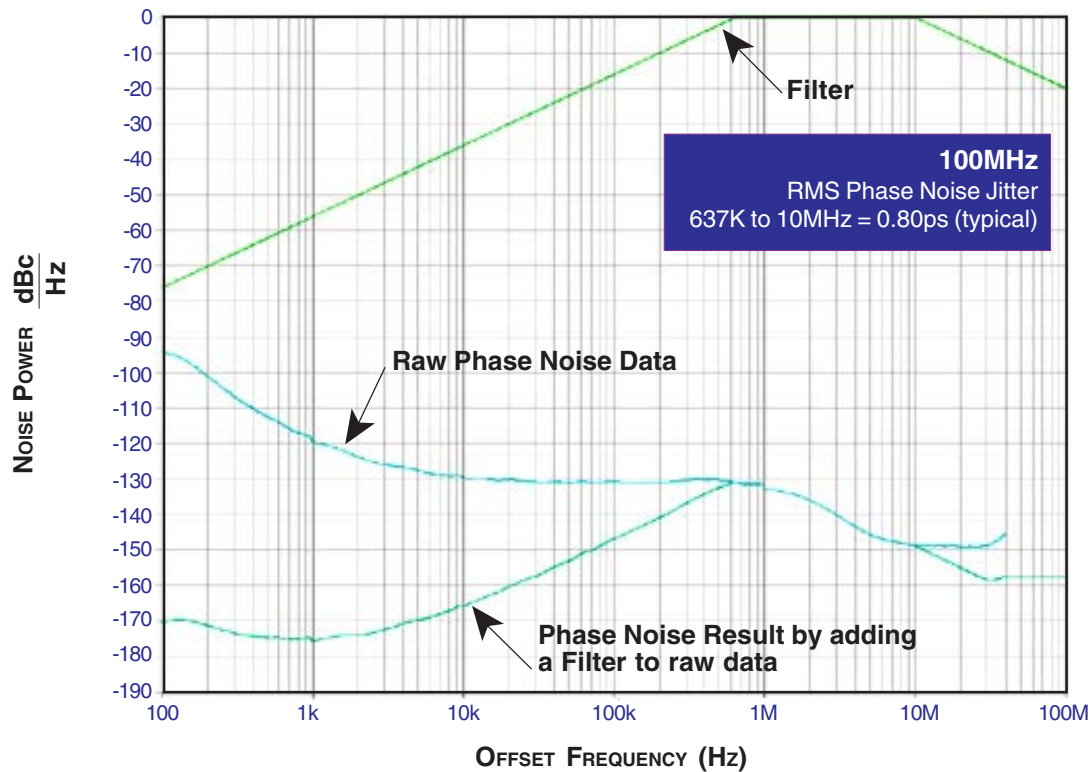
### TABLE 4. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 25 | | 26.5625 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

### TABLE 5. AC CHARACTERISTICS, $V_{CC}$ = 3.3V±5%, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $F_{OUT}$ | Output Frequency | | 93.33 | | 113.33 | MHz |
| tjit(Ø) | RMS Phase Jitter (Random); NOTE 1 | 106.25MHz; Integration Range: 637KHz - 10MHz | | 0.80 | | ps |
| | | 100MHz; Integration Range: 637KHz - 10MHz | | 0.80 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 600 | ps |
| odc | Output Duty Cycle | | 48 | | 52 | % |

NOTE 1: Please refer to the Phase Noise Plot.

## TYPICAL PHASE NOISE AT 100MHz

Filter

**100MHz**
RMS Phase Noise Jitter
637K to 10MHz = 0.80ps (typical)

**Raw Phase Noise Data**

**Phase Noise Result by adding
a Filter to raw data**

NOISE POWER $\dfrac{dBc}{Hz}$

OFFSET FREQUENCY (Hz)

## TYPICAL PHASE NOISE AT 106.25MHz

Fibre Channel Filter

**106.25MHz**
RMS Phase Noise Jitter
637K to 10MHz = 0.80ps (typical)

**Raw Phase Noise Data**

**Phase Noise Result by adding
Fibre Channel Filter to raw data**

NOISE POWER $\dfrac{dBc}{Hz}$

OFFSET FREQUENCY (Hz)
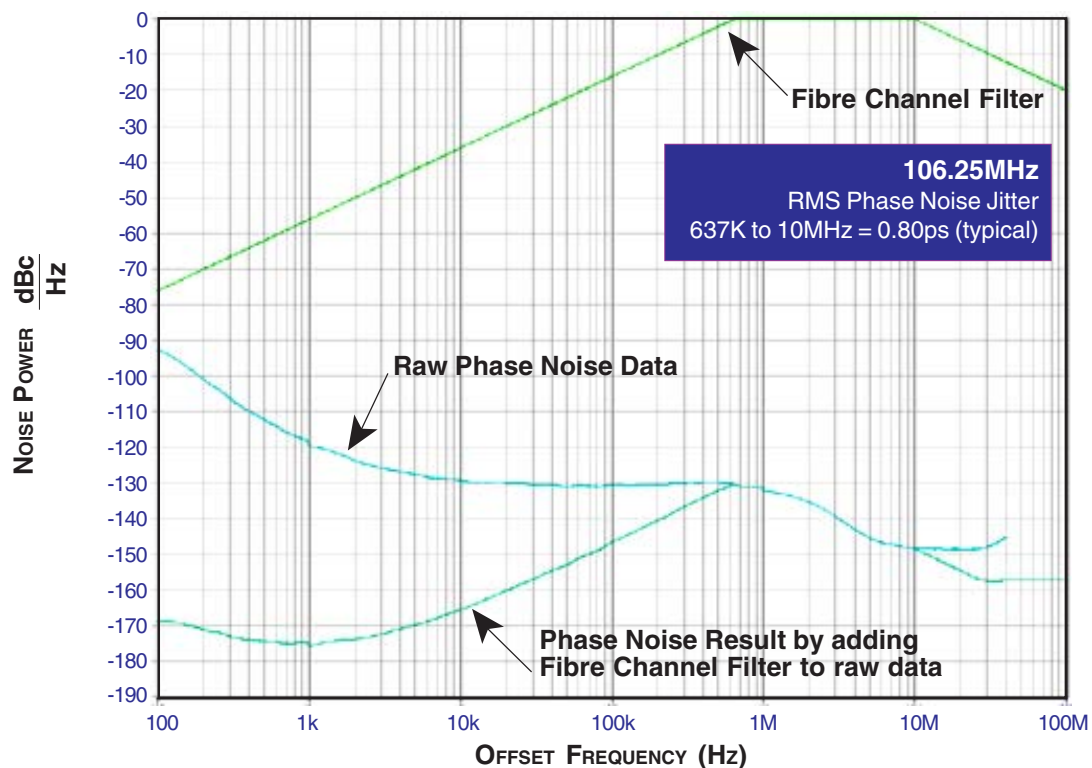
# PARAMETER MEASUREMENT INFORMATION
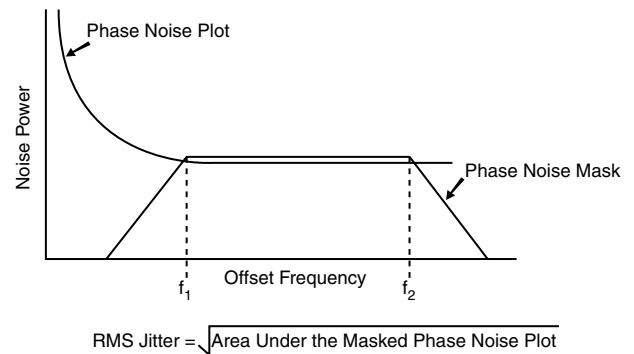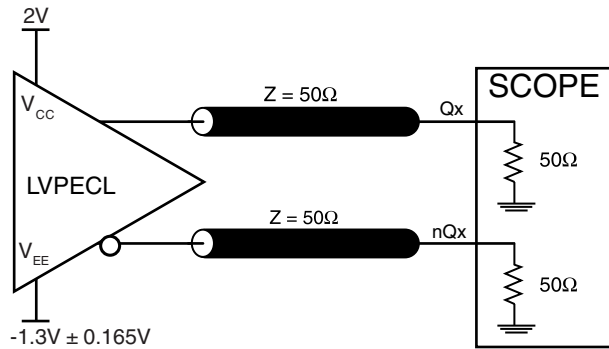


**3.3V OUTPUT LOAD AC TEST CIRCUIT**



$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

**RMS PHASE JITTER**



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}}$$
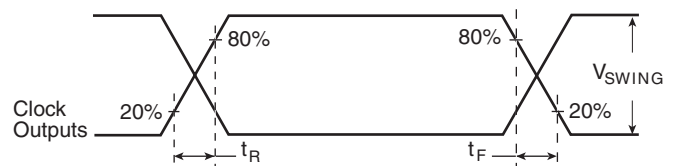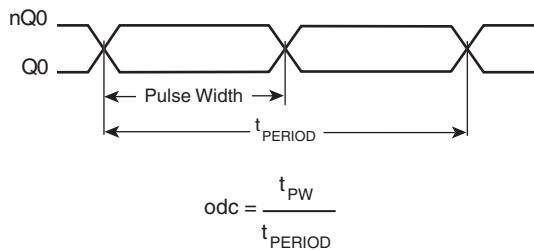
**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**OUTPUT RISE/FALL TIME**

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843011 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$, and $V_{CCA}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each $V_{CCA}$ pin.
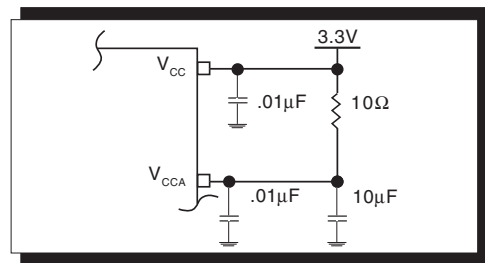


**FIGURE 1. POWER SUPPLY FILTERING**

## CRYSTAL INPUT INTERFACE

The ICS843011 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 26.5625MHz, 18pF par-allel resonant crystal and were chosen to minimize the ppm er-ror. The optimum C1 and C2 values can be slightly adjusted for different board layouts.
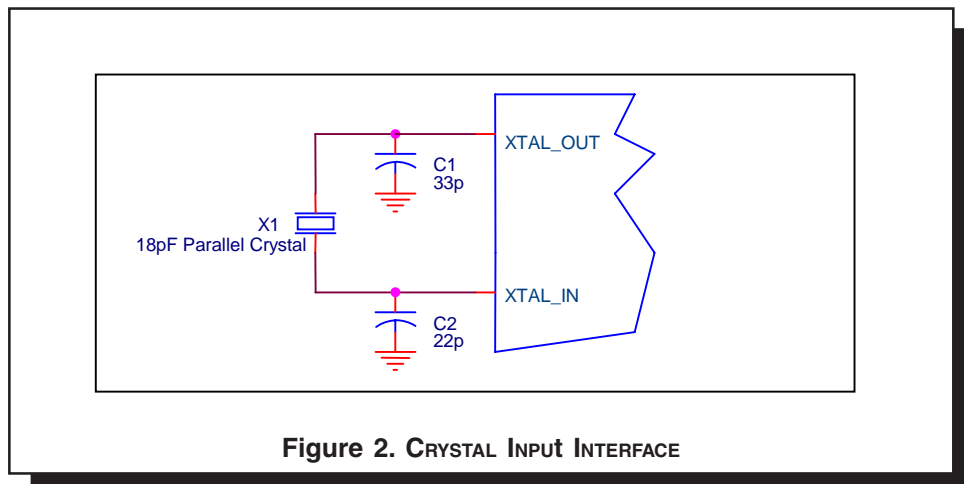


**Figure 2. CRYSTAL INPUT INTERFACE**

## APPLICATION SCHEMATIC

*Figure 3A* shows a schematic example of the ICS843011. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18 pF parallel resonant 26.5625MHz crystal is used for generating 106.25MHz output frequency. The C1 = 27pF and C2 = 33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 values may be slightly adjusted for optimizing frequency accuracy.
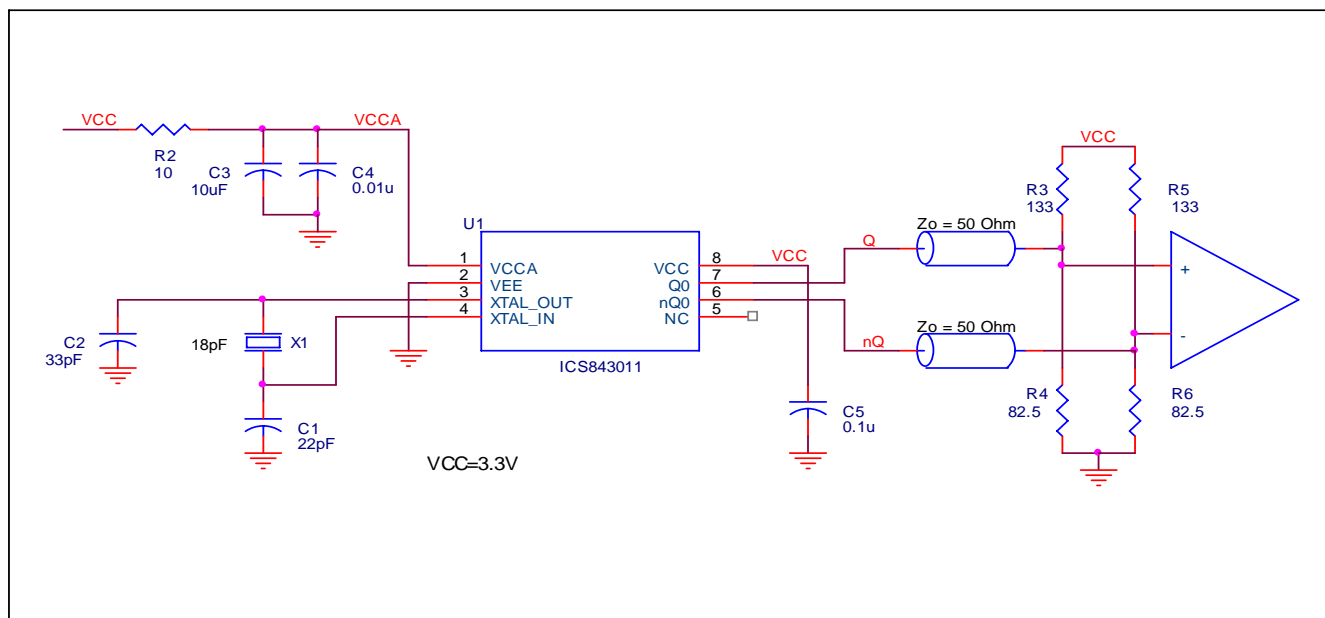


**FIGURE 3A. ICS843011 SCHEMATIC EXAMPLE**

## PC BOARD LAYOUT EXAMPLE

*Figure 3B* shows an example of ICS843011 P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 6.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

**TABLE 6. FOOTPRINT TABLE**

| Reference | Size |
|-----------|------|
| C1, C2 | 0402 |
| C3 | 0805 |
| C4, C5 | 0603 |
| R2 | 0603 |

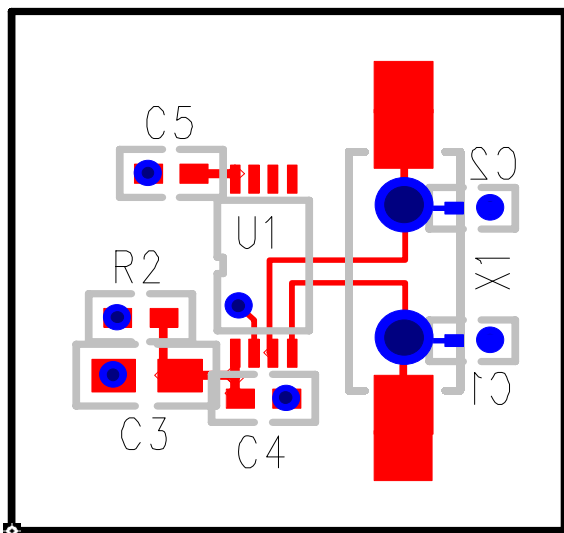NOTE: Table 6, lists component sizes shown in this layout example.



**FIGURE 3B. ICS843011 PC BOARD LAYOUT EXAMPLE**

# POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843011.
Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the ICS843011 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.
**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 93mA = **322.2mW**

- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

    **Total Power$_{\_MAX}$** (3.465V, with all outputs switching) = 322.2mW + 30mW = **352.2mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
        85°C + 0.352W * 90.5°C/W = 116.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE $\theta_{JA}$ FOR 8-PIN TSSOP, FORCED CONVECTION**

| | $\theta_{JA}$ by Velocity (Meters per Second) | | |
|---|:---:|:---:|:---:|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

*3. Calculations and Equations.*

The purpose of this section is to derive the power dissipated into the load.

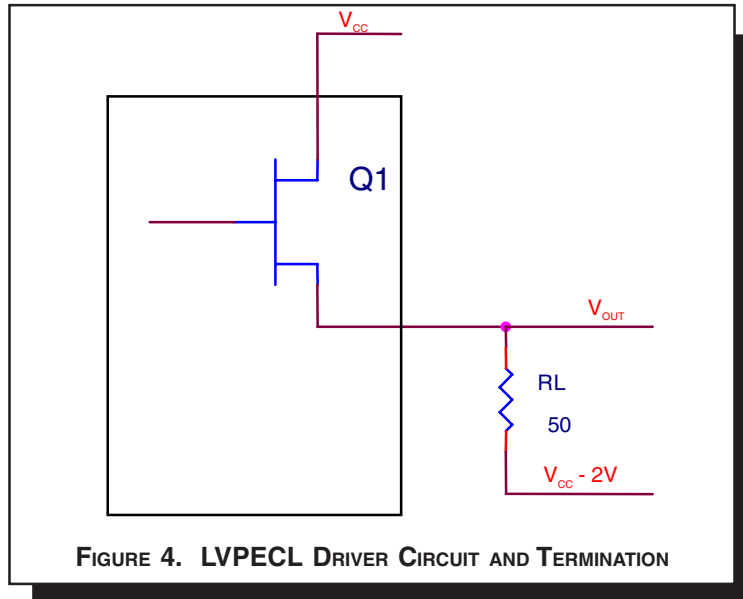LVPECL output driver circuit and termination are shown in *Figure 4.*



**FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC}$ - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

# RELIABILITY INFORMATION

**TABLE 7. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 8 LEAD TSSOP**

| $\theta_{JA}$ by Velocity (Meters per Second) | | | |
|---|---|---|---|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

**TRANSISTOR COUNT**

The transistor count for ICS843011 is: 2436

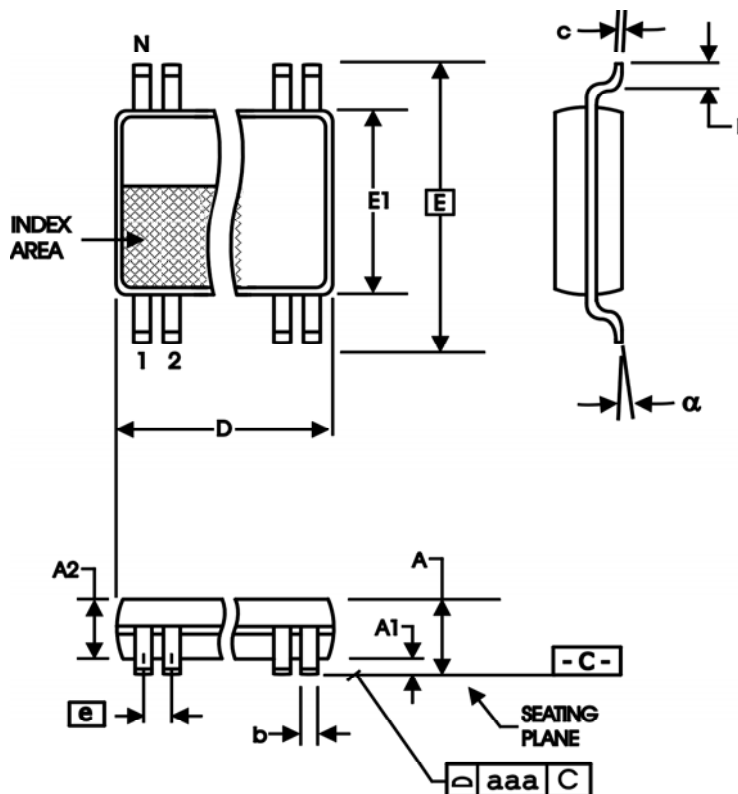**PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP**



**TABLE 8. PACKAGE DIMENSIONS**

| SYMBOL | Millimeters | |
| --- | --- | --- |
| | Minimum | Maximum |
| N | 8 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 2.90 | 3.10 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

Tᴀʙʟᴇ 9. Oʀᴅᴇʀɪɴɢ Iɴꜰᴏʀᴍᴀᴛɪᴏɴ

| Part/Order Number | Marking | Package | Shipping Package | Temperature |
|---|---|---|---|---|
| 843011AG | 3011A | 8 lead TSSOP | tube | -40°C to 85°C |
| 843011AGT | 3011A | 8 lead TSSOP | 2500 tape & reel | -40°C to 85°C |
| 843011AGLF | 011AL | 8 lead "Lead-Free" TSSOP | tube | -40°C to 85°C |
| 843011AGLFT | 011AL | 8 lead "Lead-Free" TSSOP | 2500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

| REVISION HISTORY SHEET | | | | |
|---|---|---|---|---|
| **Rev** | **Table** | **Page** | **Description of Change** | **Date** |
| B | 3A | 3 | Power Supply DC Characteristics Table - added $I_{CCA}$ spec. | 8/23/04 |
| B | T9 | 12 | Ordering Information Table - corrected count from 154 to 100. | 10/13/04 |
| B | T9 | 12 | Ordering Information Table - corrected Lead-Free marking from 3011AL to 011AL. | 10/20/04 |
| B |  | 1 | Changed ambient operating temperature bullet from -30°C to 85°C to -40°C to 85°C and throughout data sheet. | 12/10/04 |
| | | 6 | Crystal Input Interface - changed capacitor C2 value from 27p to 22p. | |
| | | 7 | Application Schematic - corrected schematic to reflect Crystal Input Interface change. | |
| B | T9 | 12 | Ordering Information Table - deleted tube count in Shipping Packaging column. | 1/26/07 |
| B | T9 | 12 | Updated datasheet's header/footer with IDT from ICS. | 7/26/10 |
| | | | Removed ICS prefix from Part/Order Number column. | |
| | | 14 | Added Contact Page. | |

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