

LOW SKEW, 1-TO-4 MULTIPLEXED DIFFERENTIAL/ LVCMOS-TO-LVCMOS FANOUT BUFFER

ICS8305-02

GENERAL DESCRIPTION



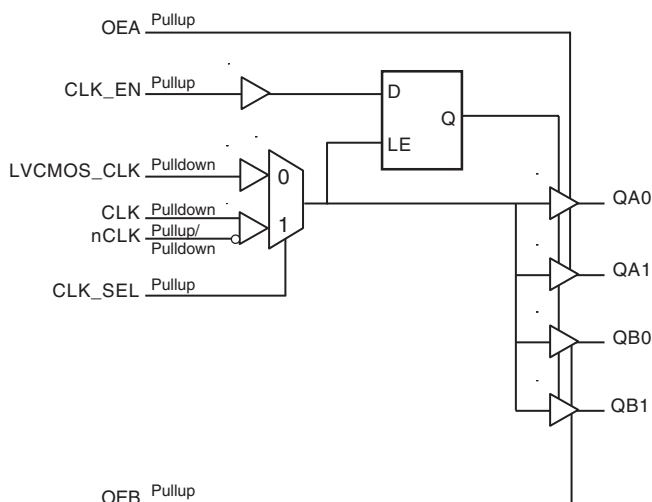
The ICS8305-02 is a low skew, 1-to-4, Differential/LVCMOS-to-LVCMOS/LVTTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8305-02 has selectable clock inputs that accept either differential or single ended input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. Outputs are forced LOW when the clock is disabled. A separate output enable pin controls whether the outputs are in the active or high impedance state.

Guaranteed output and part-to-part skew characteristics make the ICS8305-02 ideal for those applications demanding well defined performance and repeatability.

FEATURES

- Four LVCMOS/LVTTL outputs (two banks of two LVCMOS outputs)
- Selectable differential or LVCMOS/LVTTL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- LVCMOS_CLK supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Output skew: TBD
- Part-to-part skew: TBD
- Additive phase jitter, RMS: 0.18ps (typical)
- Power supply modes:
Core/Output
3.3V/3.3V
3.3V/2.5V
3.3V/1.8V
3.3V/1.5V
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT

OEA	1	16	QA0
OEB	2	15	VDDO_A
VDD	3	14	QA1
CLK_EN	4	13	GND
CLK	5	12	QB0
nCLK	6	11	VDDO_B
CLK_SEL	7	10	QB1
LVCMOS_CLK	8	9	GND

ICS8305-02

16-Lead TSSOP

4.4mm x 5.0mm x 0.92mm package body

G Package

Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	OEA	Input	Pullup	Output enable for Bank A outputs. When LOW, QAx outputs are in HIGH impedance state. When HIGH, QAx outputs are active. LVCMOS / LVTTL interface levels.
2	OEB	Input	Pullup	Output enable for Bank B outputs. When LOW, QBx outputs are in HIGH impedance state. When HIGH, QBx outputs are active. LVCMOS / LVTTL interface levels.
3	V _{DD}	Power		Power supply pin.
4	CLK_EN	Input	Pullup	Synchronizing clock enable. When LOW, the output clocks are disabled. When HIGH, output clocks are enabled. LVCMOS / LVTTL interface levels.
5	CLK	Input	Pulldown	Non-inverting differential clock input.
6	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V _{DD} /2 default when left floating.
7	CLK_SEL	Input	Pullup	Clock select input. When HIGH, selects CLK, nCLK inputs. When LOW, selects LVCMOS_CLK input. LVCMOS / LVTTL interface levels.
8	LVCMOS_CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
9, 13	GND	Power		Power supply ground.
10, 12	QB1, QB0	Output		Bank B clock outputs. LVCMOS / LVTTL interface levels.
11	V _{DDO_B}	Power		Output supply pin for Bank B outputs.
14, 16	QA1, QA0	Output		Bank A clock outputs. LVCMOS / LVTTL interface levels.
15	V _{DDO_A}	Power		Analog supply pin for Bank A outputs.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
C _{PD}	Power Dissipation Capacitance (per output)			13		pF
R _{OUT}	Output Impedance			7		Ω

TABLE 3. CONTROL INPUT FUNCTION TABLE

Inputs				Outputs
OEA, OEB	CLK_EN	CLK_SEL	Selected Source	QA _x , QB _x
1	0	0	LVC MOS_CLK	Disabled; LOW
1	0	1	CLK, nCLK	Disabled; LOW
1	1	0	LVC MOS_CLK	Enabled
1	1	1	CLK, nCLK	Enabled
0	X	X		HiZ

NOTE: After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

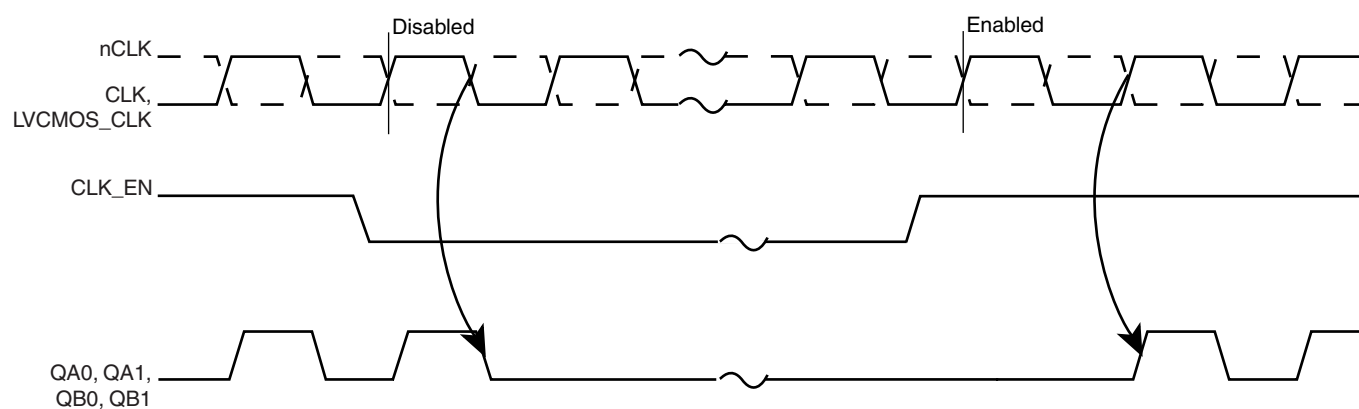


FIGURE 1. CLK_EN TIMING DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO_X} + 0.5V$
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO_A} = V_{DDO_B} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO_A}, V_{DDO_B}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.65	1.8	1.95	V
			1.425	1.5	1.575	V
I_{DD}	Power Supply Current			17		mA
I_{DDO_A}, I_{DDO_B}	Output Supply Current			2		mA

TABLE 4B. LVC MOS/LVTTL DC CHARACTERISTICS, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN, CLK_SEL, OEA, OEB	$V_{DD} = V_{IN} = 3.465V$			5	μA
		LVC MOS_CLK	$V_{DD} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	CLK_EN, CLK_SEL, OEA, OEB	$V_{DD} = 3.465V, V_{IN} = 0V$	-150			μA
		LVC MOS_CLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO_X} = 3.3V \pm 5\%$	2.6			V
			$V_{DDO_X} = 2.5V \pm 5\%$	1.8			V
			$V_{DDO_X} = 1.8V \pm 0.15V$	1.5			V
			$V_{DDO_X} = 1.5V \pm 5\%$	$V_{DDO} - 0.3$			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO_X} = 3.3V \pm 5\%$			0.5	V
			$V_{DDO_X} = 2.5V \pm 5\%$			0.5	V
			$V_{DDO_X} = 1.8V \pm 0.15V$			0.4	V
			$V_{DDO_X} = 1.5V \pm 5\%$			0.35	V
I_{OZL}	Output Tristate Current Low			-5			μA
I_{OZH}	Output Tristate Current High					5	μA

NOTE 1: Outputs terminated with 50Ω to $V_{DDO_X}/2$. See Parameter Measurement Information, Output Load Test Circuit.

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $T_A = 0^{\circ}\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK $V_{IN} = V_{DD} = 3.465\text{V}$			150	μA
		CLK $V_{IN} = V_{DD} = 3.465\text{V}$			150	μA
I_{IL}	Input Low Current	nCLK $V_{IN} = 0\text{V}, V_{DD} = 3.465\text{V}$	-150			μA
		CLK $V_{IN} = 0\text{V}, V_{DD} = 3.465\text{V}$	-5			μA
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{DD} + 0.3\text{V}$.NOTE 2: Common mode voltage is defined as V_{IH} .TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO_A} = V_{DDO_B} = 3.3\text{V} \pm 5\%$, $T_A = 0^{\circ}\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{pLH}	Propagation Delay, Low to High	LVCMOS_CLK; NOTE 1A CLK, nCLK; NOTE 1B		2.3		ns
$tsk(o)$	Output Skew; NOTE 2, 4	Measured on the Rising Edge		TBD		ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4			TBD		ps
$tsk(b)$	Bank Skew; NOTE 4, 5			TBD		ps
t_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 6	155.52MHz, 12kHz - 20MHz		0.18		ps
t_R / t_F	Output Rise/Fall Time; NOTE 7	20% to 80%		450		ps
odc	Output Duty Cycle	Ref = CLK/nCLK		50		%
		Ref = LVCMOS_CLK, $f \leq 180\text{MHz}$		50		%
t_{EN}	Output Enable Time; NOTE 7				5	ns
t_{DIS}	Output Disable Time; NOTE 7				5	ns

All parameters measured at $f \leq 250\text{MHz}$ unless noted otherwise.NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.NOTE 1B: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

NOTE 6: Driving only one input clock.

NOTE 7: These parameters are guaranteed by characterization. Not tested in production.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO_A} = V_{DDO_B} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{pLH}	Propagation Delay, Low to High	LVC MOS_CLK; NOTE 1A CLK, nCLK; NOTE 1B		2.5		ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4	Measured on the Rising Edge		TBD		ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4			TBD		ps
$t_{sk(b)}$	Bank Skew; NOTE 4, 5			TBD		ps
t_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 6	155.52MHz, 12kHz - 20MHz		0.18		ps
t_R / t_F	Output Rise/Fall Time; NOTE 7	20% to 80%		450		ps
odc	Output Duty Cycle	Ref = CLK/nCLK		50		%
		Ref = LVC MOS_CLK, $f \leq 180MHz$		50		%
t_{EN}	Output Enable Time; NOTE 7				5	ns
t_{DIS}	Output Disable Time; NOTE 7				5	ns

All parameters measured at $f \leq 250MHz$ unless noted otherwise.

NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 1B: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

NOTE 6: Driving only one input clock.

NOTE 7: These parameters are guaranteed by characterization. Not tested in production.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO_A} = V_{DDO_B} = 1.8V \pm 0.15V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{pLH}	Propagation Delay, Low to High	LVC MOS_CLK; NOTE 1A CLK, nCLK; NOTE 1B		3		ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4	Measured on the Rising Edge		TBD		ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4			TBD		ns
$t_{sk(b)}$	Bank Skew; NOTE 4, 5			TBD		ps
t_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 6	155.52MHz, 12kHz - 20MHz		0.18		ps
t_R / t_F	Output Rise/Fall Time; NOTE 7	20% to 80%		450		ps
odc	Output Duty Cycle	Ref = CLK/nCLK		50		%
		Ref = LVC MOS_CLK, $f \geq 166MHz$		50		%
		Ref = LVC MOS_CLK, $f > 166MHz$		50		%
t_{EN}	Output Enable Time; NOTE 7				5	ns
t_{DIS}	Output Disable Time; NOTE 7				5	ns

See notes in Table 5B.

TABLE 5D. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO_A} = V_{DDO_B} = 1.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{pLH}	Propagation Delay, Low to High	LVC MOS_CLK; NOTE 1A CLK, nCLK; NOTE 1B		3.3		ns
$t_{sk(o)}$	Output Skew; NOTE 2, 4	Measured on the Rising Edge		TBD		ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4			TBD		ps
$t_{sk(b)}$	Bank Skew; NOTE 4, 5			TBD		ps
t_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section, NOTE 6	155.52MHz, 12kHz - 20MHz		0.18		ps
t_R / t_F	Output Rise/Fall Time; NOTE 7	20% to 80%		450		ps
odc	Output Duty Cycle	Ref = CLK/nCLK		50		%
		Ref = LVC MOS_CLK, $f \geq 166MHz$		50		%
		Ref = LVC MOS_CLK, $f > 166MHz$		50		%
t_{EN}	Output Enable Time; NOTE 7				5	ns
t_{DIS}	Output Disable Time; NOTE 7				5	ns

All parameters measured at $f \leq 250MHz$ unless noted otherwise.

NOTE 1A: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 1B: Measured from the differential input crossing point to $V_{DDO}/2$ of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

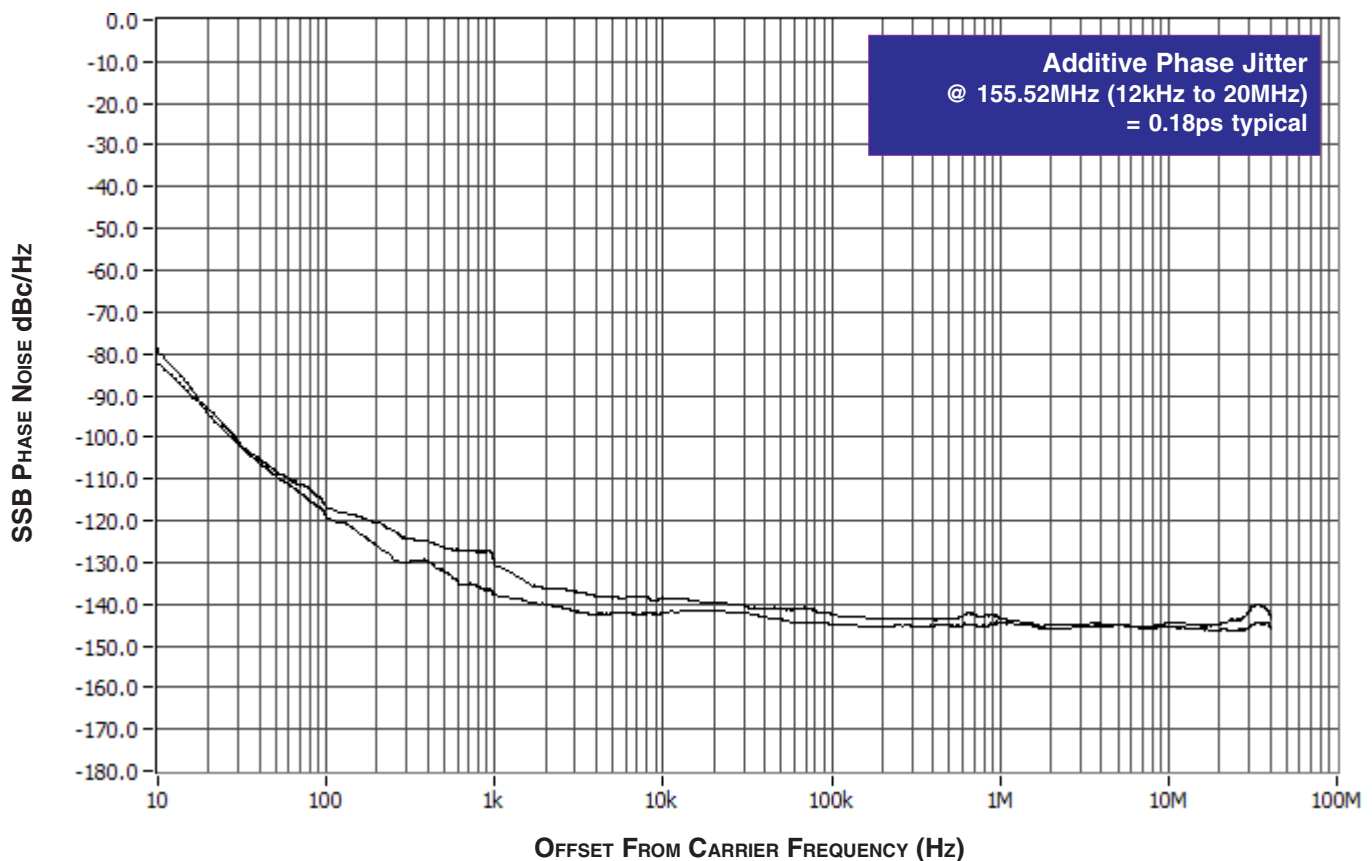
NOTE 6: Driving only one input clock.

NOTE 7: These parameters are guaranteed by characterization. Not tested in production.

ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz

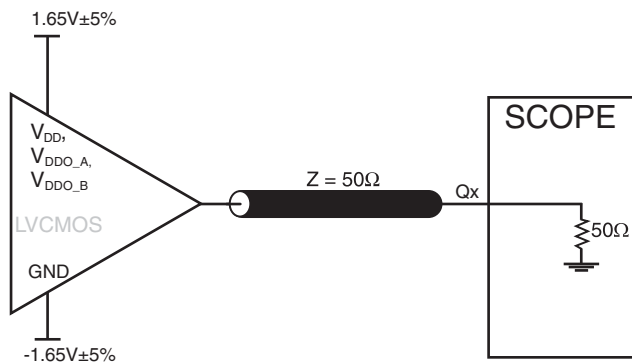
band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



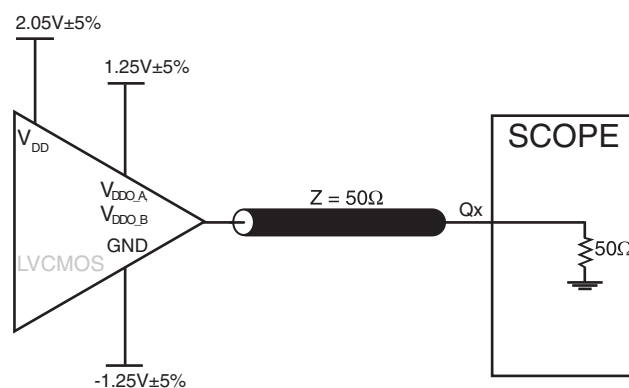
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device

meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

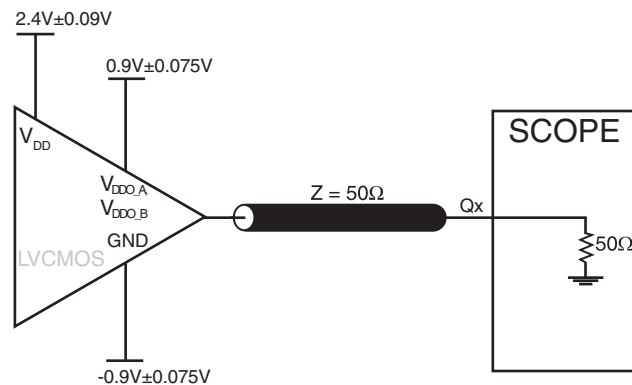
PARAMETER MEASUREMENT INFORMATION



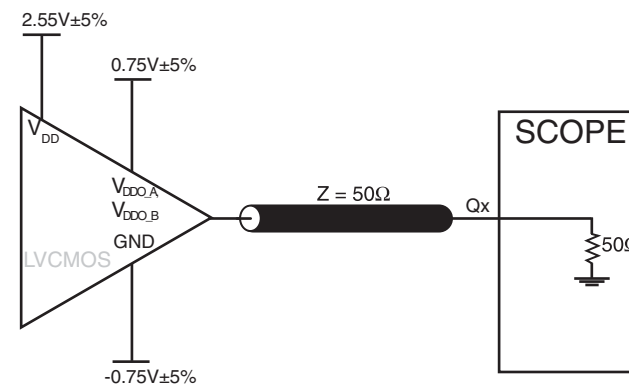
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



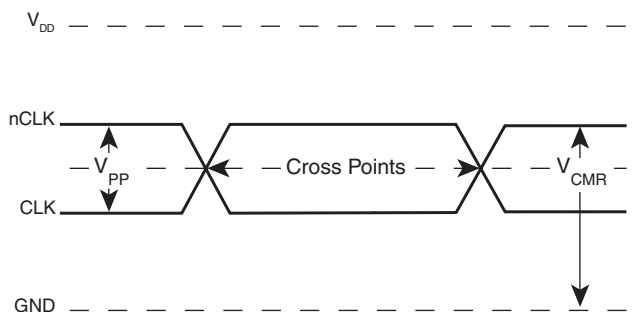
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



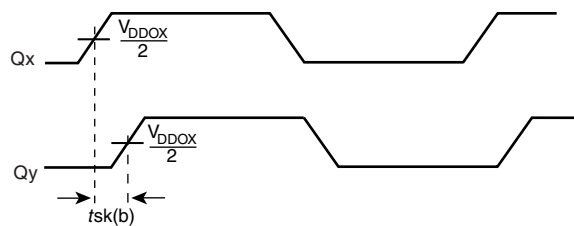
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



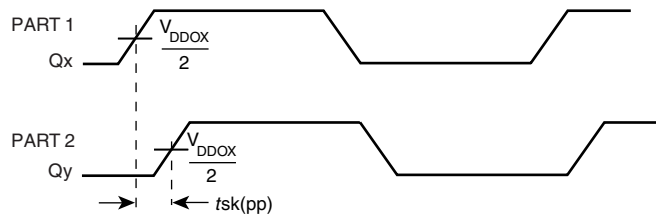
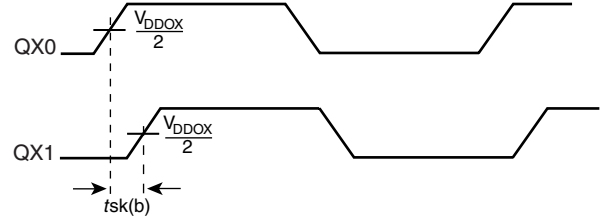
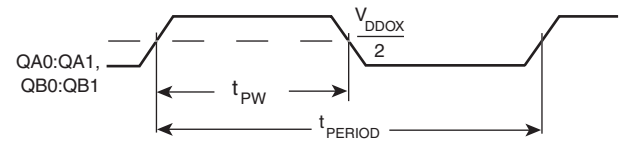
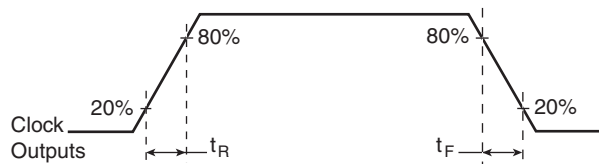
3.3V CORE/1.5V OUTPUT LOAD AC TEST CIRCUIT



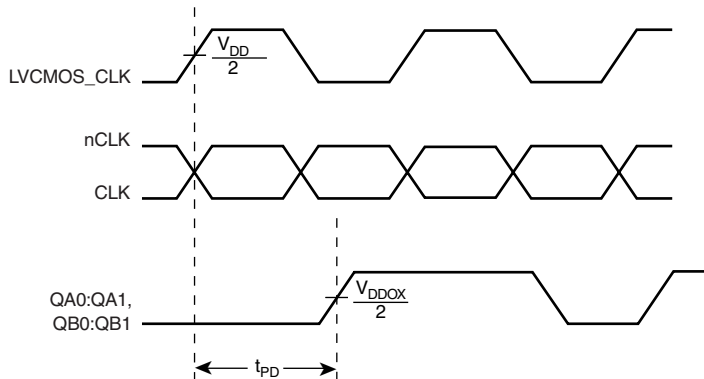
DIFFERENTIAL INPUT LEVEL



OUTPUT SKEW

**PART-TO-PART SKEW****BANK SKEW (where X denotes outputs in the same bank)**

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT RISE/FALL TIME**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD****PROPAGATION DELAY**

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

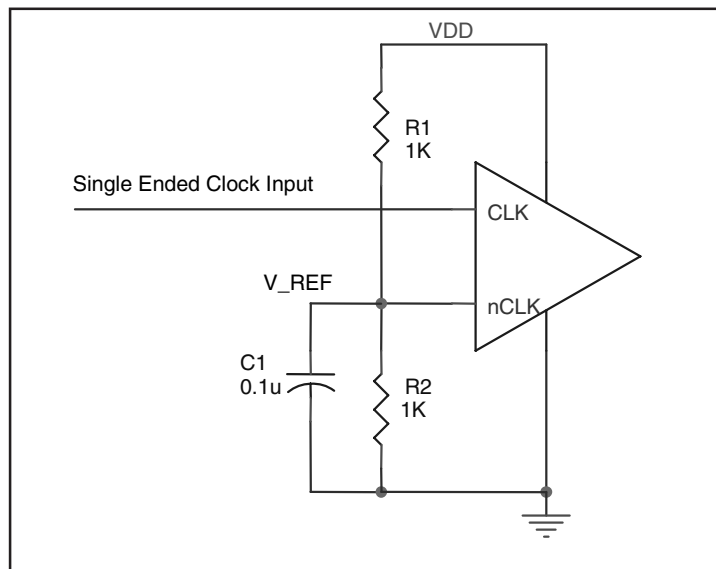


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK INPUT:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from the CLK input to ground.

CLK/nCLK INPUT:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from CLK to ground.

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

OUTPUTS:

LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. There should be no trace attached.

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are

examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

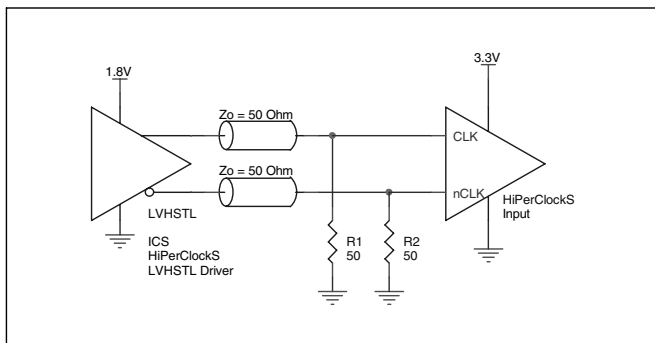


FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY IDT HiPerClockS LVHSTL DRIVER

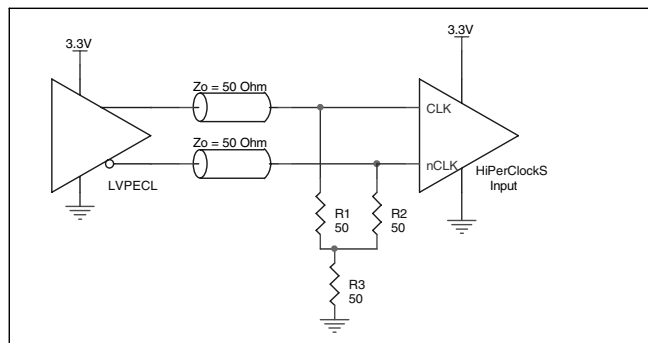


FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

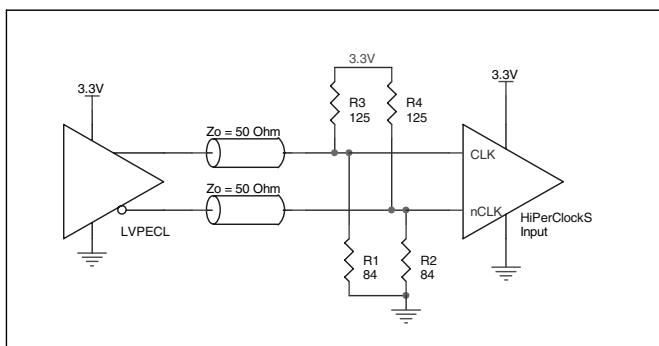


FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

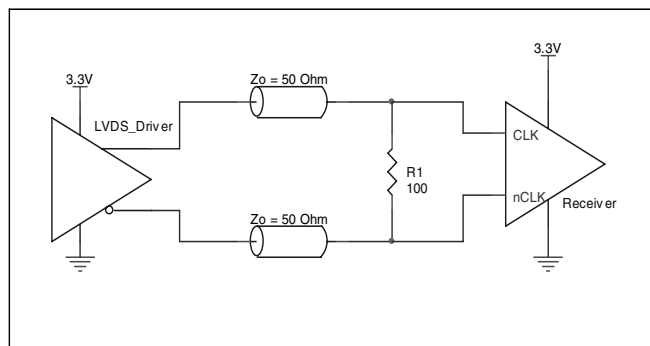


FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

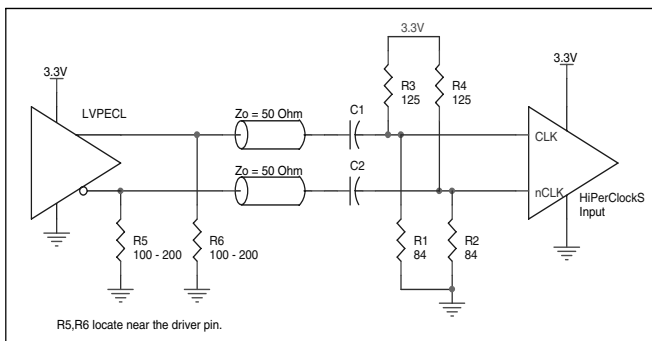


FIGURE 3E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for ICS8305-02 is: 538

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

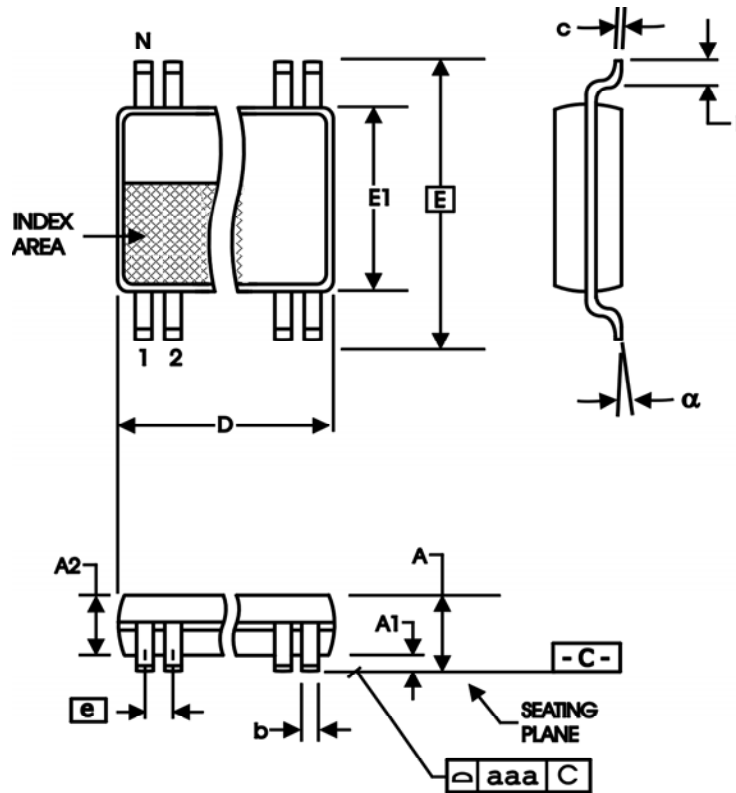


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8305AG-02	8305AG02	16 Lead TSSOP	tube	0°C to 70°C
ICS8305AG-02T	8305AG02	16 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS8305AG-02LF	8305A02L	16 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS8305AG-02LFT	8305A02L	16 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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