Synchronous Equipment Timing Source for Synchronous Ethernet

82P33714

SHORT FORM DATA SHEET

HIGHLIGHTS

- Synchronous Equipment Timing Source (SETS) for Synchronous Ethernet (SyncE) per ITU-T G.8264
- DPLL1 generates ITU-T G.8262 compliant SyncE clocks, Telcordia GR-1244-CORE/GR-253-CORE, and ITU-T G.813 compliant SONET/SDH clocks
- DPLL2 performs rate conversions for synchronization interfaces or for other general purpose timing applications
- DPLL1 can be configured as a Digitally Controlled Oscillators (DCOs) for PTP clock synthesis
- DCO frequency resolution is [(77760 / 1638400) * 2^-48] or ~1.686305041e-10 ppm
- APLL1 and APLL2 generate clocks with jitter < 1 ps RMS (12 kHz to 20 MHz) for: 1000BASE-T and 1000BASE-X
- Fractional-N input dividers support a wide range of reference frequencies
- Locks to 1 Pulse Per Second (PPS) references
- DPLLs, APLL1 and APLL2 can be configured from an external EEPROM after reset

FEATURES

- Differential reference inputs (IN1 to IN4) accept clock frequencies between 1 PPS and 650 MHz
- Single ended inputs (IN5 to IN6) accept reference clock frequencies between 1 PPS and 162.5 MHz
- Loss of Signal (LOS) pins (LOS0 to LOS3) can be assigned to any clock reference input
- Reference monitors qualify/disqualify references depending on activity, frequency and LOS pins
- Automatic reference selection state machines select the active reference for each DPLL based on the reference monitors, priority tables, revertive and non-revertive settings and other programmable settings
- Fractional-N input dividers enable the DPLLs to lock to a wide range of reference clock frequencies including: 10/100/1000 Ethernet, 10G Ethernet, OTN, SONET/SDH, PDH, TDM, GSM, CPRI, and GNSS frequencies
- Any reference inputs (IN1 to IN6) can be designated as external sync pulse inputs (1 PPS, 2 kHz, 4 kHz or 8 kHz) associated with a selectable reference clock input
- FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS output sync pulses that are aligned with the selected external input sync pulse input and frequency locked to the associated reference clock input
- DPLL1 can be configured with bandwidths between 0.09 mHz and 567 Hz
- DPLL1 locks to input references with frequencies between 1 PPS and 650 MHz
- DPLL2 locks to input references with frequencies between 8 kHz and 650 MHz
- DPLL1 complies with ITU-T G.8262 for Synchronous Ethernet Equipment Clock (EEC), and G.813 for Synchronous Equipment Clock (SEC); and Telcordia GR-253-CORE/ GR-1244-CORE for Stratum 3 and SONET Minimum Clock (SMC)
- DPLL1 generates clocks with PDH, TDM, GSM, CPRI/OBSAI, 10/100/1000 Ethernet and GNSS frequencies; these clocks are directly available on OUT1 and OUT8
- DPLL2 generates N x 8 kHz clocks up to 100 MHz that are output on OUT9 and OUT10
- APLL1 and APLL2 are connected to DPLL1
- APLL1 and APLL2 generate 10/100/1000 Ethernet, 10G Ethernet, or SONET/SDH frequencies
- Any of eight common TCXO/OCXO frequencies can be used for the System Clock: 10 MHz, 12.8 MHz, 13 MHz, 19.44 MHz, 20 MHz, 24.576 MHz, 25 MHz or 30.72 MHz
- The I2C slave, SPI or the UART interface can be used by a host processor to access the control and status registers
- The I2C master interface can automatically load a device configuration from an external EEPROM after reset
- Differential outputs OUT3 to OUT6 output clocks with frequencies between 1 PPS and 650 MHz
- Single ended outputs OUT1, OUT2, OUT7 and OUT8 output clocks with frequencies between 1 PPS and 125 MHz
- Single ended outputs OUT9 and OUT10 output clocks N*8 kHz multiples up to 100 MHz
- DPLL1 supports independent programmable delays for each of IN1 to IN6; the delay for each input is programmable in steps of 0.61 ns with a range of ~±78 ns
- The input to output phase delay of DPLL1 is programmable in steps of 0.0745 ps with a total range of ±20 µs
- The clock phase of each of the output dividers for OUT1 (from APLL1) to OUT8 is individually programmable in steps of ~200 ps with a total range of +/-180°
- 1149.1 JTAG Boundary Scan
- 72-pin QFN green package

APPLICATIONS

- Access routers, edge routers, core routers
- Carrier Ethernet switches
- Multiservice access platforms
- PON OLT
- LTE eNodeB
- ITU-T G.8264 Synchronous Equipment Timing Source (SETS)
- ITU-T G.8262 Synchronous Ethernet Equipment Clock (EEC)
- ITU-T G.813 Synchronous Equipment Clock (SEC)
- Telcordia GR-253-CORE/GR1244-CORE Stratum 3 Clock (S3) and SONET Minimum Clock (SMC)

DESCRIPTION

The 82P33714 Synchronous Equipment Timing Source (SETS) for Synchronous Ethernet (SyncE) provides tools to manage timing references, clock generation and timing paths for SyncE based clocks, per ITU-T G.8264 and ITU-T G.8262. 82P33714 meets the requirements of ITU-T G.8262 for synchronous Ethernet Equipment Clocks (EECs) and ITU-T G.813 for Synchronous Equipment Clocks (SEC). The device outputs low-jitter clocks that can directly synchronize Ethernet interfaces; as well as SONET/SDH and PDH interfaces.

The 82P33714 accepts four differential reference inputs and two single ended reference inputs that can operate at common GNSS, Ethernet, SONET/SDH and PDH frequencies that range from 1 Pulse Per Second (PPS) to 650 MHz. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. All of the references are available to both Digital PLLs (DPLLs). The active reference for each DPLL is determined by forced selection or by automatic selection based on user programmed priorities and locking allowances and based on the reference monitors and LOS inputs.

The 82P33714 can accept a clock reference and an associated phase locked sync signal as a pair. DPLL1 can lock to the clock reference and align the frame sync and multi-frame sync outputs with the paired sync input. The device allows any of the differential or single ended reference inputs to be configured as sync inputs that can be associated with any of the other differential or single ended reference inputs. The input sync signals can have a frequency of 1 PPS, 2 kHz, 4 kHz or 8 kHz. This feature enables DPLL1 to phase align its frame sync and multi-frame sync outputs with a sync input without the need use a low bandwidth setting to lock directly to the sync input.

The DPLLs support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode the DPLLs synthesize clocks based on the system clock alone. In Locked mode the DPLLs filter reference clock jitter with the selected bandwidth. In Locked mode, the long-term output frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode, the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available.

DPLL1 also supports DCO mode. In DCO mode the DPLL control loop is opened and the DCO can be controlled by an IEEE 1588 clock recovery servo running on an external processor to synthesize IEEE 1588 clocks.

The 82P33714 requires a system clock for its reference monitors and other digital circuitry. The frequency accuracy of the system clock determines the frequency accuracy of the DPLLs in Free-Run mode. The frequency stability of the system clock determines the frequency stability of the DPLLs in Free-Run mode and in Holdover mode; and it affects the wander generation of the DPLLs in Locked mode.

When used with a suitable system clock, DPLL1 meets the frequency accuracy, pull-in, hold-in, pullout, noise generation, noise tolerance, transient response, and holdover performance requirements of the following applications: ITU-T G.8262/G.813 EEC/SEC options 1 and 2, Telcordia GR-1244 Stratum 3 (S3), Telcordia GR-253-CORE S3 and SONET Minimum Clock (SMC).

DPLL1 can be configured with a range of selectable filtering bandwidths from 0.09 mHz to 567 Hz. The 17 mHz bandwidth can be used to lock the DPLL directly to a 1 PPS reference. The 92 mHz bandwidth can be used for G.8262/G.813 Option 2, or Telcordia GR-253-CORE S3, or SMC applications. The bandwidths in the range 1.1 Hz to 8.9 Hz can be used for G.8262/G.813 Option 1 applications. The bandwidth of 1.1 Hz or 2.2 Hz can be used for Telcordia GR-1244-CORE S3 applications. Bandwidths above 10 Hz can be used in jitter attenuation and rate conversion applications.

DPLL2 is a wideband (BW > 25Hz) frequency translator that can be used, for example, to convert a recovered line clock to a 1.544 MHz or 2.048 MHz synchronization interface clock.

For SETS applications per ITU-T G.8264, DPLL1 is configured as an EEC/SEC to output clocks for the T0 reference point and DPLL2 is used to output clocks for the T4 reference point.

Clocks generated by DPLL1 can be passed through APLL1 or APLL2 which are LC based jitter attenuating Analog PLLs (APLLs). The output clocks generated by APLL1 and APLL2 are suitable for serial GbE and lower rate interfaces.

All 82P33714 control and status registers are accessed through an I2C slave, SPI or UART interface. For configuring the DPLLs, APLL1 and APLL2, the I2C master interface can automatically load a configuration from an external EEPROM after reset.

FUNCTIONAL BLOCK DIAGRAM

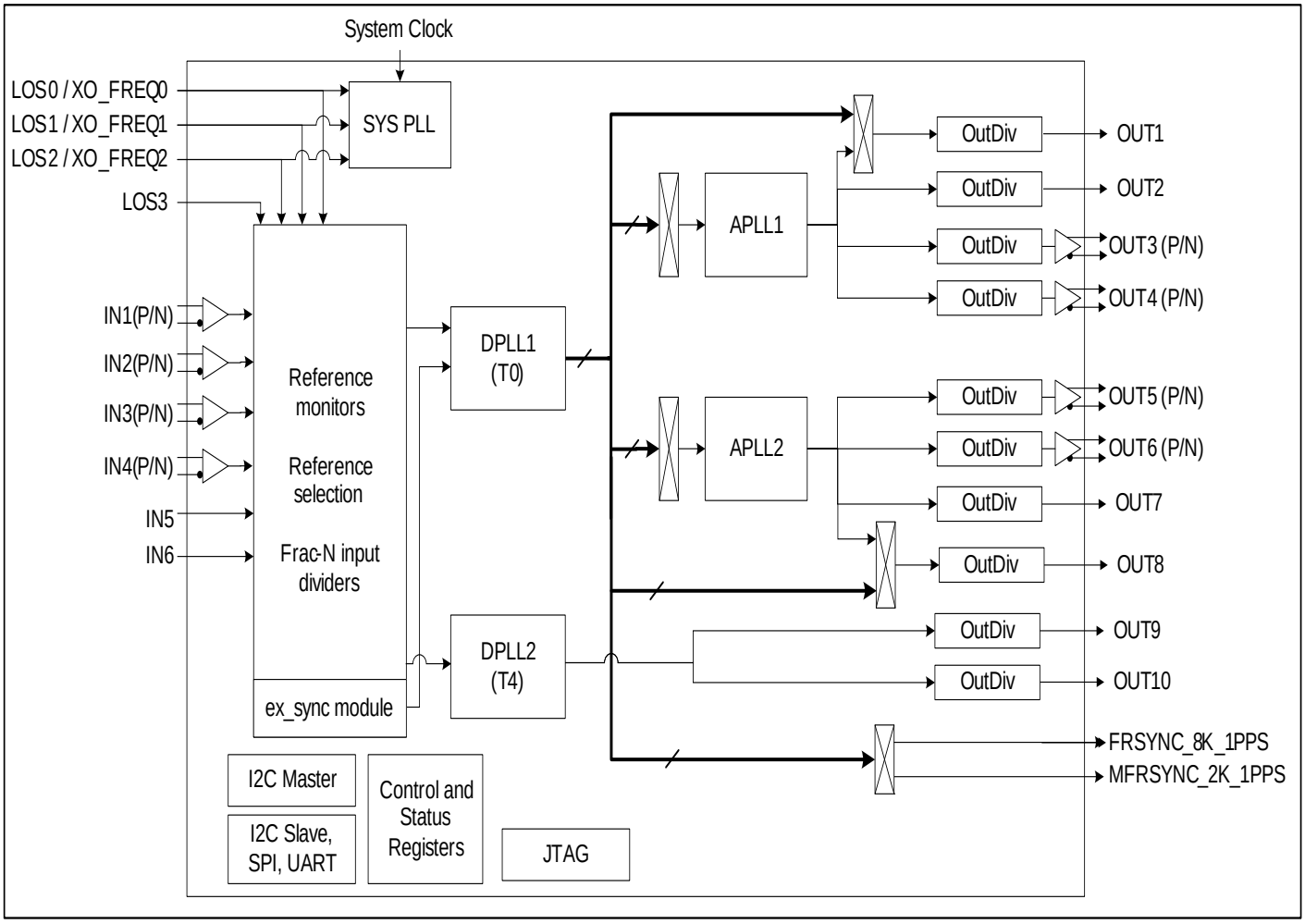

Figure 1. Functional Block Diagram

1 PIN ASSIGNMENT

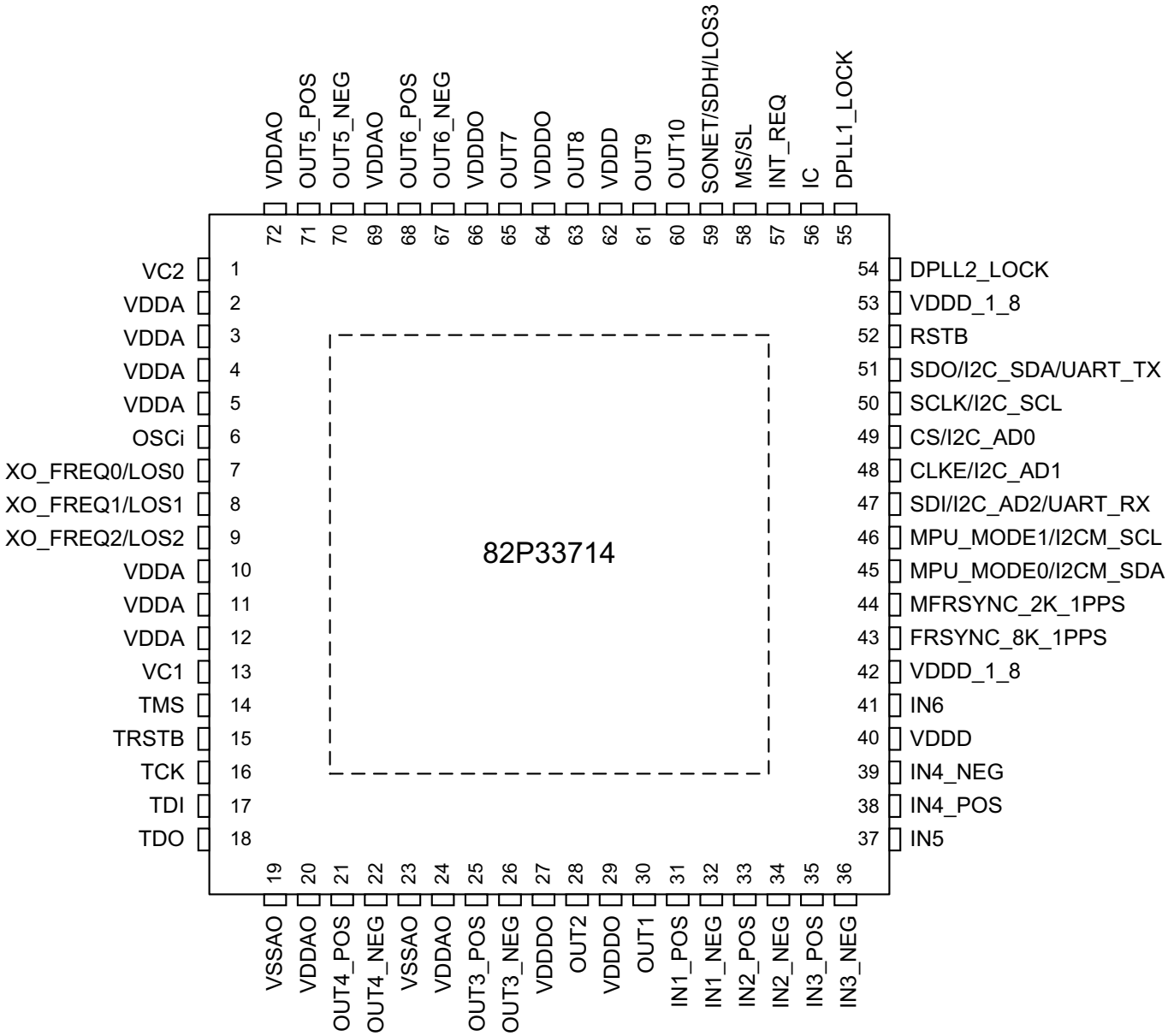

Figure 2. Pin Assignment (Top View)

1 PIN DESCRIPTION

Table 1: Pin Description

Pin No.	Name	I/O	Type	Description
Global Control Signal				
6	OSCI	I	CMOS	OSCI: Crystal Oscillator System Clock A clock provided by a crystal oscillator is input on this pin. It is the system clock for the device. The oscillator frequency is selected via pins XO_FREQ0 ~ XO_FREQ2
58	MS/SL	I pull-up	CMOS	MS/SL: Master / Slave Selection This pin, together with the MS_SL_CTRL bit, controls whether the device is configured as the Master or as the Slave. The signal level on this pin is reflected by the MASTER_SLAVE bit.
59	SONET/SDH/ LOS3	I pull-down	CMOS	SONET/SDH: SONET / SDH Frequency Selection During reset, this pin determines the default value of the IN_SONET_SDH bit: High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, the value on this pin takes no effect. LOS3- This pin is used to disqualify input clocks. See input clocks section for more details.
52	RSTB	I pull-up	CMOS	RSTB: Reset A low pulse of at least 50 µs on this pin resets the device. If loading from an EEPROM, the maximum time from RSTB de-assert to have stable clocks is 100ms. If not loading from EEPROM the maximum time from RSTB de-assert to have stable clocks is 10 ms.
7 8 9	XO_FREQ0/ LOS0 XO_FREQ1/ LOS1 XO_FREQ2/ LOS2	I pull-down	CMOS	XO_FREQ0 ~ XO_FREQ2: These pins set the oscillator frequency. XO_FREQ[2:0] Oscillator Frequency (MHz) 000 10.000 001 12.800 010 13.000 011 19.440 100 20.000 101 24.576 110 25.000 111 30.720 LOS0 ~ LOS2 - These pins are used to disqualify input clocks. See input clocks section for more details. After reset, this pin takes on the operation of LOS0-LOS2
Input Clock and Frame Synchronization Input Signal				
31 32	IN1_POS IN1_NEG	I	PECL/LVDS	IN1_POS / IN1_NEG: Positive / Negative Input Clock 1 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
33 34	IN2_POS IN2_NEG	I	PECL/LVDS	IN2_POS / IN2_NEG: Positive / Negative Input Clock 1 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
35 36	IN3_POS IN3_NEG	I	PECL/LVDS	IN3_POS / IN3_NEG: Positive / Negative Input Clock 3 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
38 39	IN4_POS IN4_NEG	I	PECL/LVDS	IN4_POS / IN4_NEG: Positive / Negative Input Clock 4 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
37	IN5	I pull-down	CMOS	IN5: Input Clock 5 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
41	IN6	I pull-down	CMOS	IN6: Input Clock 6 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
Output Frame Synchronization Signal				
43	FRSYNC _8K_1PPS	O	CMOS	FRSYNC_8K_1PPS: 8 kHz Frame Sync Output An 8 kHz signal or a 1PPS sync signal is output on this pin.
44	MFRSYNC _2K_1PPS	O	CMOS	MFRSYNC_2K_1PPS: 2 kHz Multiframe Sync Output A 2 kHz signal or a 1PPS sync signal is output on this pin.
Output Clock				
30 28	OUT1 OUT2	O	CMOS	OUT1 ~ OUT2: Output Clock 1 ~ 2
25 26	OUT3_POS OUT3_NEG	O	PECL/LVDS	OUT3_POS / OUT3_NEG: Positive / Negative Output Clock 3 This output is set to LVDS by default.
21 22	OUT4_POS OUT4_NEG	O	PECL/LVDS	OUT4_POS / OUT4_NEG: Positive / Negative Output Clock 4 This output is set to LVDS by default.
71 70	OUT5_POS OUT5_NEG	O	PECL/LVDS	OUT5_POS / OUT5_NEG: Positive / Negative Output Clock 5 This output is set to LVDS by default.
68 67	OUT6_POS OUT6_NEG	O	PECL/LVDS	OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6 This output is set to LVDS by default.
65 63	OUT7 OUT8	O	CMOS	OUT7 ~ OUT8: Output Clock 7 ~ 8
61 60	OUT9 OUT10	O	CMOS	OUT9 ~ OUT10: Output Clock 9 ~ 10
Miscellaneous				
13	VC1	O	Analog	VC1: APLL1 VC Output An external RC filter (a resistor in series with a capacitor to ground, and another capacitor in parallel) should be connected to this pin.
1	VC2	O	Analog	VC2: APLL2 VC Output An external RC filter (a resistor in series with a capacitor to ground, and another capacitor in parallel) should be connected to this pin.
Lock Signal				
54	DPLL2_LOCK	O	CMOS	DPLL2_LOCK This pin goes high when DPLL2 is locked
55	DPLL1_LOCK	O	CMOS	DPLL1_LOCK This pin goes high when DPLL1 is locked
Microprocessor Interface				
57	INT_REQ	O Tri-state	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request.
46 45	MPU_MODE1/ I2CM_SCL MPU_MODE0/ I2CM_SDA	I/O pull-up	CMOS/ Open Drain	MPU_MODE[1:0]: Microprocessor Interface Mode Selection During reset, these pins determine the default value of the MPU_SEL_CNFG[1:0] bits as follows: 00: I2C mode 01: SPI mode 10: UART mode 11: I2C master (EEPROM) mode I2CM_SCL: Serial Clock Line In I2C master mode, the serial clock is output on this pin. I2CM_SDA: Serial Data Input for I2C Master Mode In I2C master mode, this pin is used as the for the serial data.

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
47	SDI/I2C_AD2/ UART_RX	I pull-down	CMOS	SDI: Serial Data Input In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK. I2C_AD2: Device Address Bit 2 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. UART_RX In UART mode, this pin is used as the receive data (UART Receive)
48	CLKE/I2C_AD1	I pull-down	CMOS	CLKE: SCLK Active Edge Selection In Serial mode, this pin is an input, it selects the active edge of SCLK to update the SDO: High - The falling edge; Low - The rising edge. I2C_AD1: Device Address Bit 1 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
49	CS/I2C_AD0	I pull-up	CMOS	CS: Chip Selection In Serial modes, this pin is an input.A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over. I2C_AD0: Device Address Bit 0 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
50	SCLK/I2C_SCL	I pull-down	CMOS	SCLK: Shift Clock In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE. I2C_SCL: Serial Clock Line In I2C mode, the serial clock is input on this pin.
51	SDO/I2C_SDA/ UART_TX I2C_SDA	I/O pull-up	CMOS/ Open Drain	SDO: Serial Data Output In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK. I2C_SDA: Serial Data Input/Output In I2C mode, this pin is used as the input/output for the serial data. UART_TX: In UART mode, this pin is used as the transmit data (UART Transmit)
JTAG (per IEEE 1149.1)				
14	TMS	I pull-up	CMOS	TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
15	TRSTB	I pull-up	CMOS	TRSTB: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
16	TCK	I pull-down	CMOS	TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
17	TDI	I pull-up	CMOS	TDI: JTAG Test Data Input The test data are input on this pin. They are clocked into the device on the rising edge of TCK.

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
18	TDO	O tri-state	CMOS	TDO: JTAG Test Data Output The test data are output on this pin. They are clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning.
Power & Ground				
2, 3, 4, 5, 10 11, 12	VDDA	Power	-	VDDA: Analog Core Power - +3.3V DC nominal
20, 24, 69, 72	VDDAO	Power		VDDAO: Analog Output Power - +3.3V DC nominal
27, 29, 64, 66	VDDDO	Power		VDDDO: Digital Output Power - +3.3V DC nominal
40, 62	VDDD	Power		VDDD: Digital Core Power - +3.3V DC nominal
42, 53	VDDD_1_8	Power		VDDD_1_8: Digital Core Power - +1.8V DC nominal
19,23	VSSAO	Ground		VSSAO: Ground
73 (e_PAD)	VSS	Ground	-	VSS: Ground
Other				
56	IC	-	-	IC: Internal Connection Internal Use. This pin must be left open for normal operation.

1.1 RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

1.1.1 INPUTS

Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Single-Ended Clock Inputs

For protection, unused single-ended clock inputs should be tied to ground.

Differential Clock Inputs

For applications not requiring the use of a differential input, both *_POS and *_NEG can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from _POS to ground.

1.1.2 OUTPUTS

Status Pins

For applications not requiring the use of a status pin, we recommend bringing out to a test point for debugging purposes.

Single-Ended Clock Outputs

All unused single-ended clock outputs can be left floating, or can be brought out to a test point for debugging purposes.

Differential Clock Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

PACKAGE DIMENSIONS

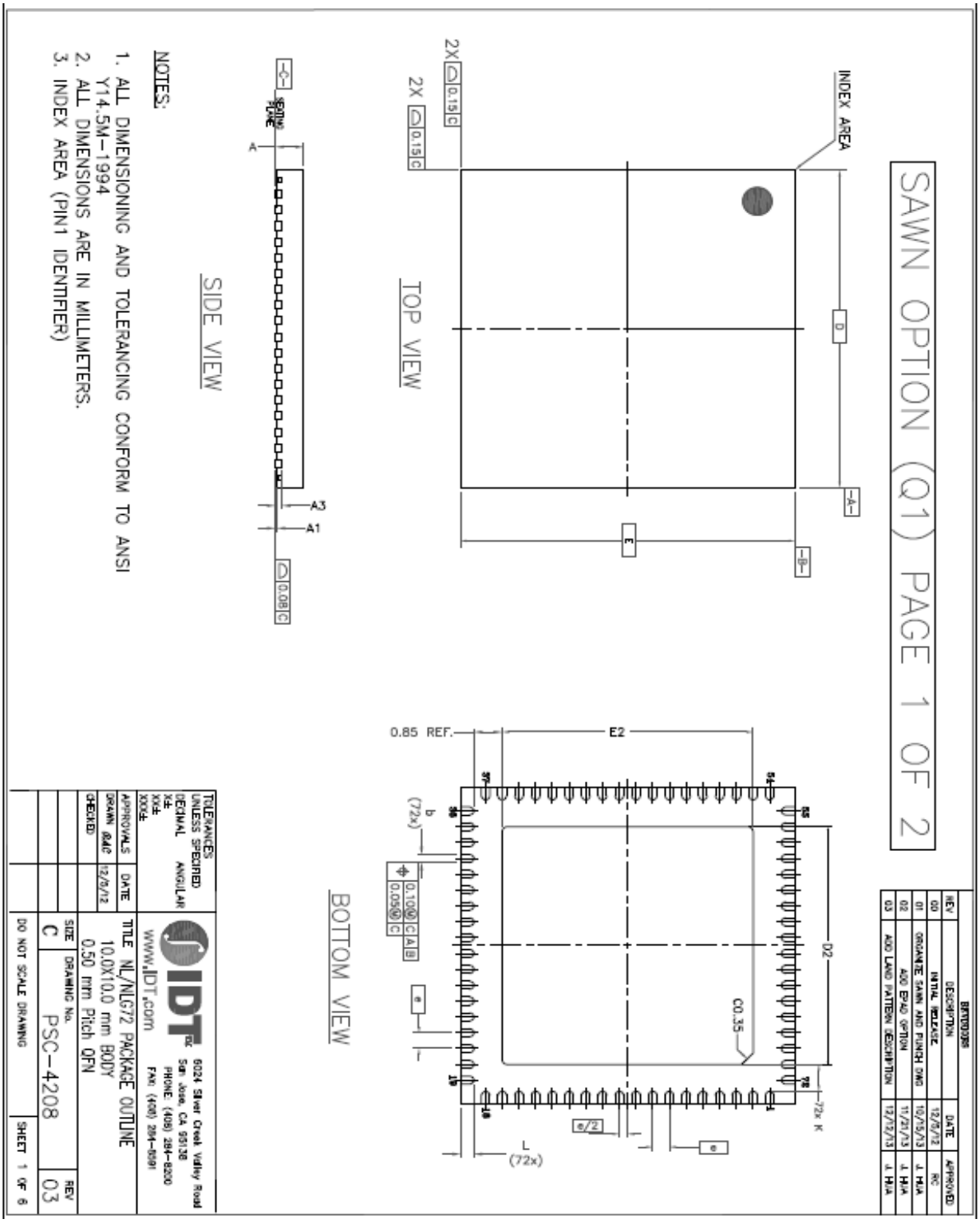

Figure 1. 72-Pin QFN Package Outline Page 1 (SAWN Option)

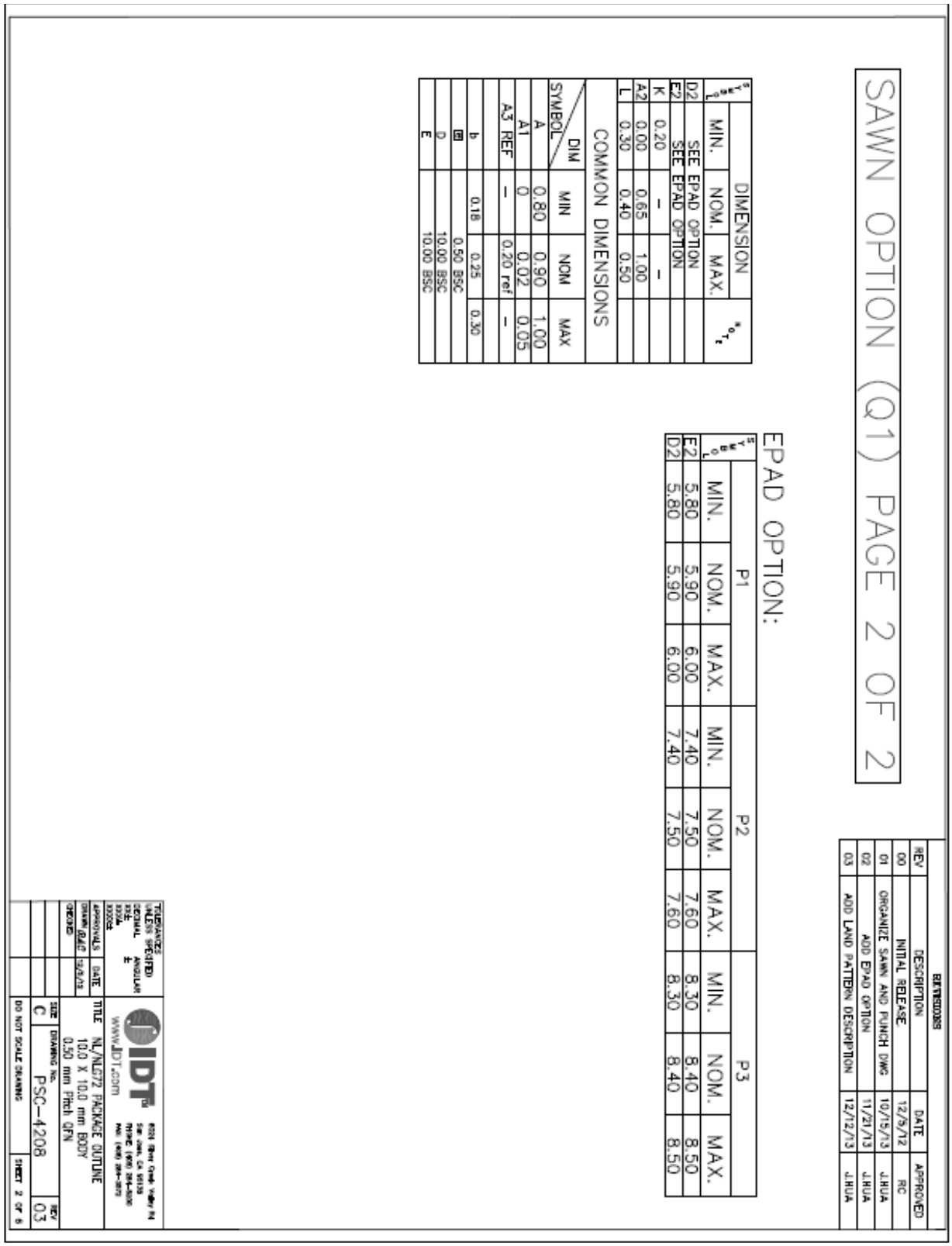

Figure 2. 72-Pin QFN Package Outline Page 2 (SAWN Option)

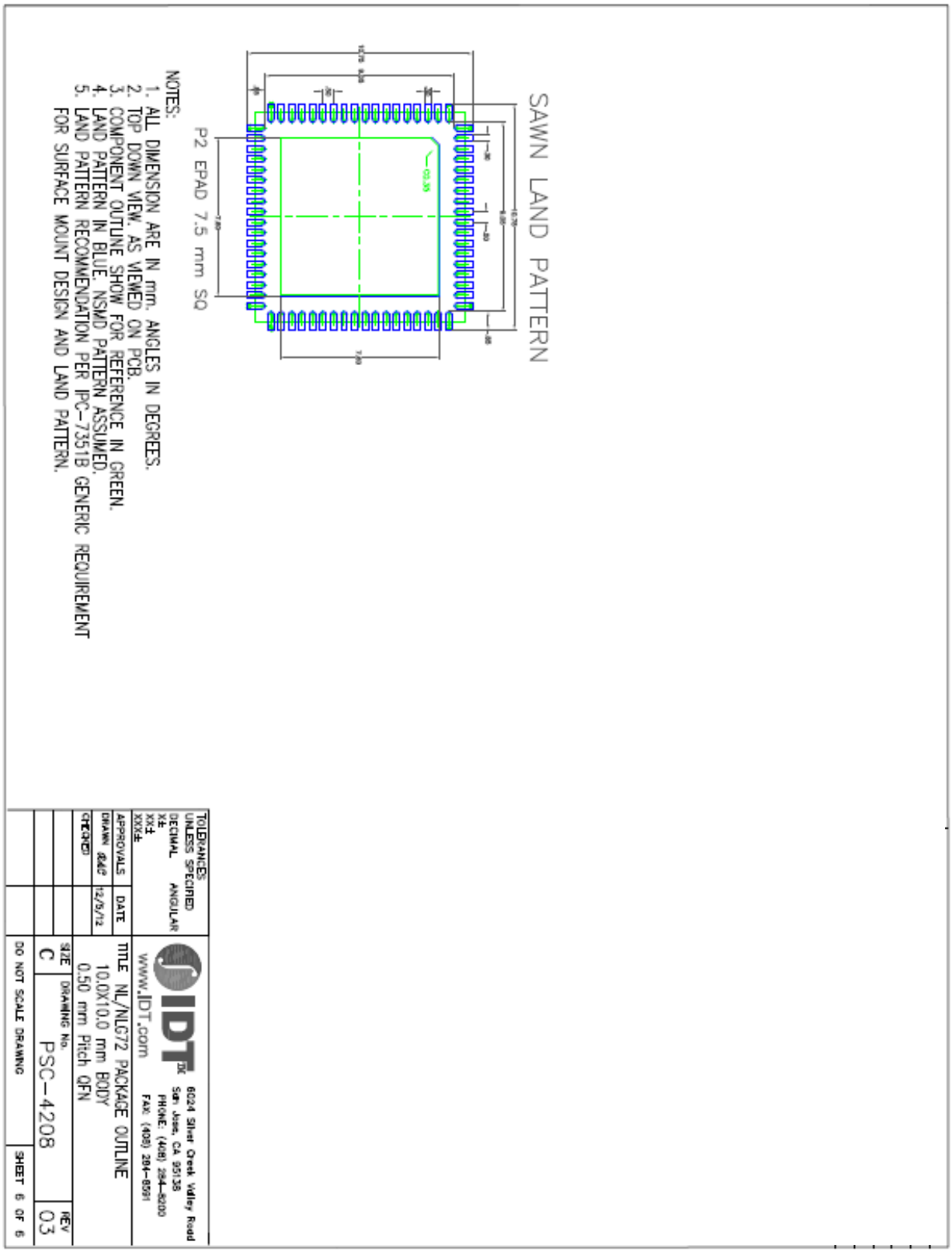

Figure 3. 72-Pin QFN Package Recommended Land Pattern

ORDERING INFORMATION

Table 2: Ordering Information

Part/Order Number	Package	Temperature
82P33714ANLG	72-Pin QFN	-40^0 to $+85^0$C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

REVISION HISTORY

Rev.	Date	Description of Change

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