



FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT805BT/CT

FEATURES:

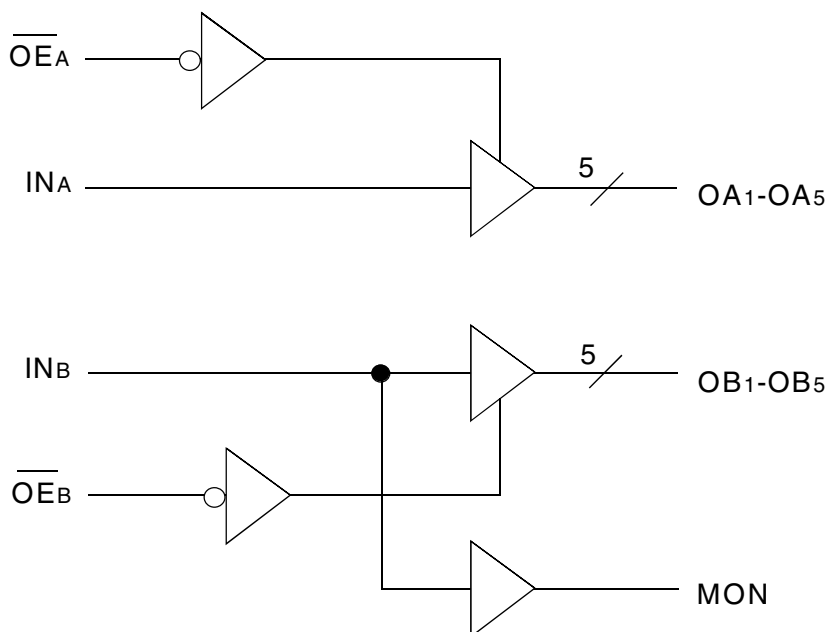
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 600ps (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- TTL level output voltage swings
- High drive: -32mA I_{OH} , +48mA I_{OL}
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in the following packages:
 - Commercial: QSOP, SOIC, SSOP
 - Military: CERDIP, LCC

DESCRIPTION:

This buffer/clock driver is built using advanced dual metal CMOS technology. The FCT805T is a non-inverting clock driver consisting of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible input. This part has extremely low output skew, pulse skew, and package skew. The device has a "heart-beat" monitor for diagnostics and PLL driving. The monitor output is identical to all other outputs and complies with the output specifications in this document.

The FCT805T is designed for fast, clean edge rates to provide accurate clock distribution in high speed systems.

FUNCTIONAL BLOCK DIAGRAM

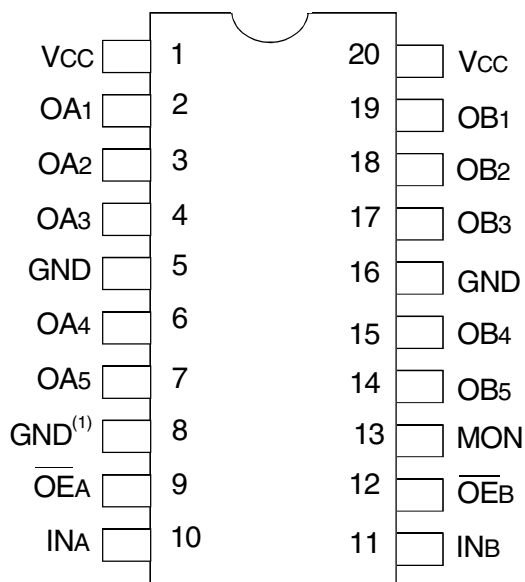


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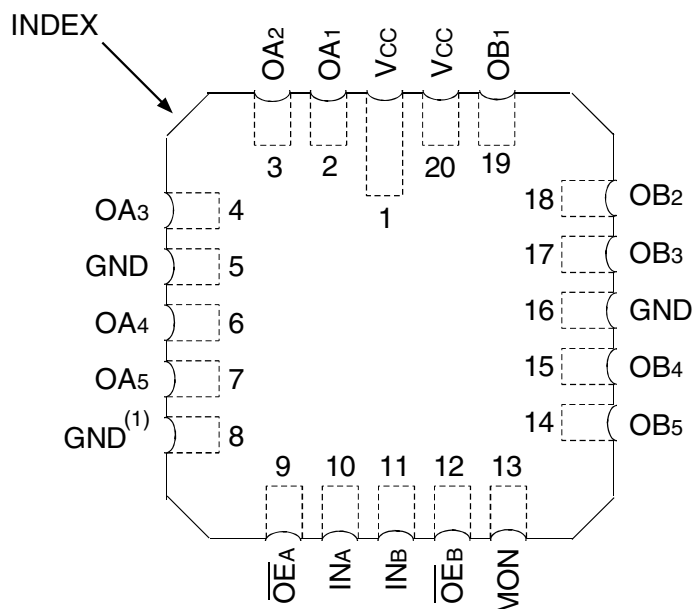
MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 2010

PIN CONFIGURATION



QSOP/ SOIC/ SSOP/ Cerdip
TOP VIEW



LCC
TOP VIEW

NOTE:

- Pin 8 is internally connected to GND. To insure compatibility with all products, pin 8 should be connected to GND at the board level.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	V _{IN} = 0V	4.5	6	pF
COUT	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
OEA, OEB	3-State Output Enable Inputs (Active LOW)
INA, INB	Clock Inputs
OAx, OBx	Clock Outputs
MON	Monitor Output

FUNCTION TABLE ⁽¹⁾

Inputs		Outputs	
OEA, OEB	INA, INB	OAx, OBx	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE:

- H = HIGH
L = LOW
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁵⁾	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	± 1	μA
I_{OZH}	High Impedance Output Current (3-State Output Pins)	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-255	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -12\text{mA MIL}$	2.4	3.3	—	V
			$I_{OH} = -15\text{mA COM'L}$				
			$I_{OH} = -24\text{mA MIL}$ $I_{OH} = -32\text{mA COM'L}^{(4)}$	2	3	—	V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 32\text{mA MIL}$ $I_{OL} = 48\text{mA COM'L}$	—	0.3	0.55	V
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	± 1	μA
V_H	Input Hysteresis for all inputs	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	5	500	μA

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition should not exceed one second.
5. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	1	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $OEA = OEB = GND$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	60	100	$\mu A/MHz$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_o = 25MHz$ 50% Duty Cycle $OEA = OEB = V_{CC}$ Mon. Output Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	1.5	3	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	1.8	4	
		$V_{CC} = \text{Max.}$ Outputs Open $f_o = 50MHz$ 50% Duty Cycle $OEA = OEB = GND$ Eleven Outputs Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	33	55.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	33.5	57.5 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5V$, $+25^\circ C$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V \text{)}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_o = \text{Output Frequency}$
 $N_o = \text{Number of Outputs at } f_o$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY^(1,2)

Symbol	Parameter	Conditions ⁽³⁾	FCT805BT		FCT805CT		Unit
			Min. ⁽⁴⁾	Max.	Min. ⁽⁴⁾	Max.	
t _{PLH}	Propagation Delay	C _L = 50pF R _L = 500Ω	1.5	5.7	1.5	5.2	ns
t _{PHL}	I _{NA} to O _{AX} , I _{NB} to O _{BX}		—	—	—	—	ns
t _R	Output Rise Time		—	2	—	2	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
t _{SK(O)}	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.9	—	0.7	ns
t _{SK(P)}	Pulse skew: skew between opposite transitions of same output (t _{PHL} – t _{PLH})		—	0.9	—	0.8	ns
t _{SK(PP)}	Part-to-part skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—	1.2	ns
t _{PZL}	Output Enable Time		1.5	6.5	1.5	6	ns
t _{PZH}	O _{EA} to O _{AX} , O _{EB} to O _{BX}						
t _{PLZ}	Output Disable Time		1.5	6.5	1.5	6	ns
t _{PHZ}	O _{EA} to O _{AX} , O _{EB} to O _{BX}						

NOTES:

- t_{PLH}, t_{PHL}, and t_{SK(pp)} are production tested. All other parameters are guaranteed but not production tested.
- Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature, and process parameters. These propagation delay limits do not imply skew.
- See Test Circuits and Waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

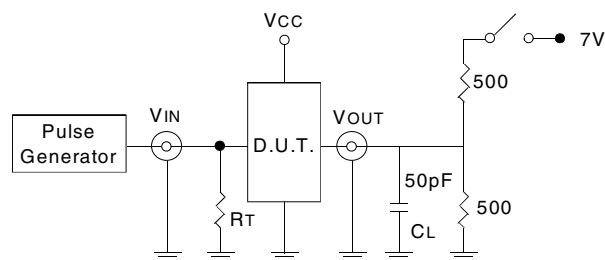
SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL^(1,2)

Symbol	Parameter	Conditions ⁽³⁾	FCT805BT		FCT805CT		Unit
			Min. ⁽⁴⁾	Max.	Min. ⁽⁴⁾	Max.	
t _{PLH}	Propagation Delay	C _L = 50pF R _L = 500Ω	1.5	5	1.5	4.5	ns
t _{PHL}	I _{NA} to O _{AX} , I _{NB} to O _{BX}		—	—	—	—	ns
t _R	Output Rise Time		—	1.5	—	1.5	ns
t _F	Output Fall Time		—	1.5	—	1.5	ns
t _{SK(O)}	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	0.5	ns
t _{SK(P)}	Pulse skew: skew between opposite transitions of same output (t _{PHL} – t _{PLH})		—	0.7	—	0.6	ns
t _{SK(PP)}	Part-to-part skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.2	—	1	ns
t _{PZL}	Output Enable Time		1.5	6	1.5	5	ns
t _{PZH}	O _{EA} to O _{AX} , O _{EB} to O _{BX}						
t _{PLZ}	Output Disable Time		1.5	6	1.5	5	ns
t _{PHZ}	O _{EA} to O _{AX} , O _{EB} to O _{BX}						

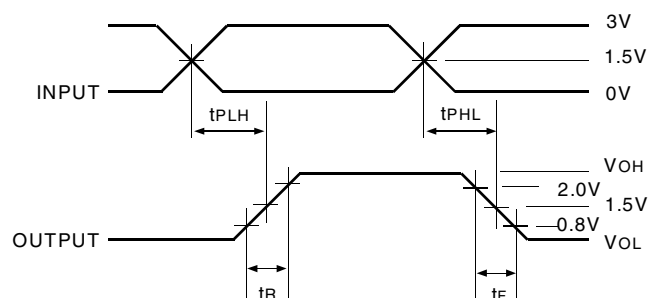
NOTES:

- t_{PLH}, t_{PHL}, and t_{SK(pp)} are production tested. All other parameters are guaranteed but not production tested.
- Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature, and process parameters. These propagation delay limits do not imply skew.
- See Test Circuits and Waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

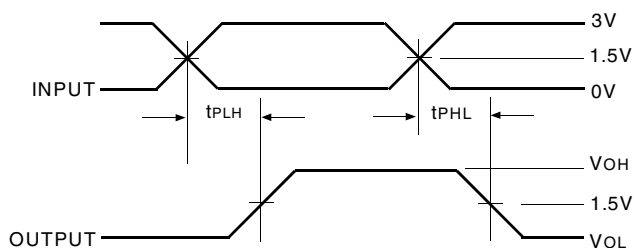
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs

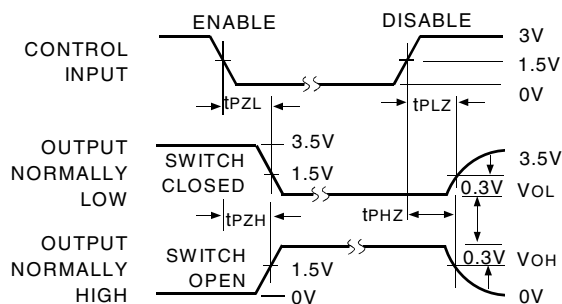


Package Delay



$$tSK(P) = |tPHL - tPLH|$$

Pulse Skew - $tSK(P)$



Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$

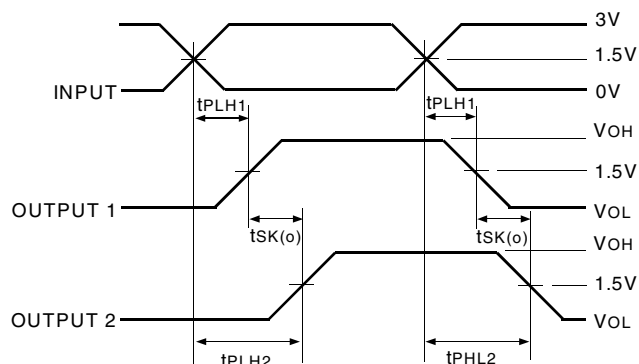
SWITCH POSITION

Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	GND

DEFINITIONS:

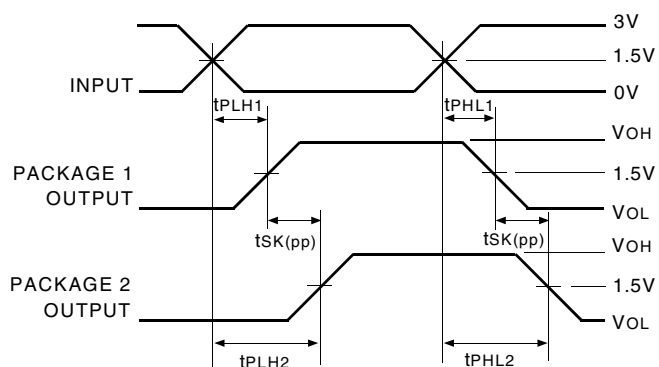
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{out} of the Pulse Generator.



$$tSK(O) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

Output Skew



$$tSK(PP) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

Part-to-Part Skew - $tSK(PP)$

NOTE:

1. Package 1 and Package 2 are same device type and speed grade.

ORDERING INFORMATION

49FCT	XXXX	XX	X		
	Device Type	Package	Process		
				Blank	Commercial (0°C to +70°C)
				B	MIL-STD-883, Class B (– 55°C to +125°C)
					<u>Commercial Options</u>
				SOG	SOIC - Green
				QG	QSOP - Green
				PYG	SSOP - Green
					<u>Military Options</u>
				D	CERDIP
				L	Leadless Chip Carrier
				805BT	Fast CMOS Buffer/Clock Driver
				805CT	



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