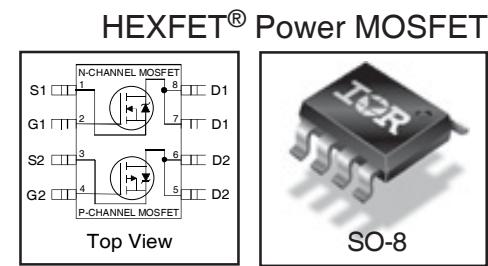


	N-CH	P-CH	
V_{DS}	30	-30	V
R_{DS(on)} max	27	64	mΩ
Q_g (typical)	6.8	8.1	nC
I_D (@ T _A = 25°C)	6.8	-4.6	A



Applications

- High and Low Side Switches for Inverter
- High and Low Side Switches for Generic Half-Bridge

Features

High and low-side MOSFETs in a single package
High-side P-Channel MOSFET
Industry-standard pinout
Compatible with existing surface mount techniques
RoHS compliant containing no Lead, no Bromide and no Halogen
MSL1, Consumer qualification

Benefits

Increased power density
Easier drive circuitry
Multi-vendor compatibility
Easier manufacturing
Environmentally friendlier
Increased reliability

Base Part Number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRF9389PbF	SO-8	Tube/Bulk	95	IRF9389PbF
		Tape and Reel	4000	IRF9389TRPbF

Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
V _{GS}	Gate-to-Source Voltage	±20	±20	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	6.8	-4.6	
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	5.4	-3.7	A
I _{DM}	Pulsed Drain Current ①	34	-23	
P _D @ T _A = 25°C	Power Dissipation	2.0		
P _D @ T _A = 70°C	Power Dissipation	1.3		W
	Linear Derating Factor	0.016		W/°C
T _J	Operating Junction and	-55 to + 150		
T _{STG}	Storage Temperature Range			°C

Thermal Resistance

	Parameter	Typ.	Max	Units
R _{θJL}	Junction-to-Drain Lead ④	—	20	°C/W
R _{θJA}	Junction-to-Ambient ③	—	62.5	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$
		P-Ch	-30	—	—		$V_{\text{GS}} = 0\text{V}, I_D = -250\mu\text{A}$
$\Delta \text{BV}_{\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.03	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch	—	0.02	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{\text{DS(on)}}$	Static Drain-to-Source On-Resistance	N-Ch	—	22	27	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}, I_D = 6.8\text{A}$ ②
			—	33	40		$V_{\text{GS}} = 4.5\text{V}, I_D = 5.4\text{A}$ ②
		P-Ch	—	51	64	$\text{m}\Omega$	$V_{\text{GS}} = -10\text{V}, I_D = -4.6\text{A}$ ②
			—	82	103		$V_{\text{GS}} = -4.5\text{V}, I_D = -3.7\text{A}$ ②
$V_{\text{GS(th)}}$	Gate Threshold Voltage	N-Ch	1.3	1.8	2.3	V	$V_{\text{DS}} = V_{\text{GS}}, I_D = 10\mu\text{A}$
		P-Ch	-1.3	-1.8	-2.3		$V_{\text{DS}} = V_{\text{GS}}, I_D = -10\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	$V_{\text{DS}} = 24\text{V}, V_{\text{GS}} = 0\text{V}$
		P-Ch	—	—	-1.0		$V_{\text{DS}} = -24\text{V}, V_{\text{GS}} = 0\text{V}$
		N-Ch	—	—	150		$V_{\text{DS}} = 24\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$
		P-Ch	—	—	-150		$V_{\text{DS}} = -24\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-Ch	—	—	100	nA	$V_{\text{GS}} = 20\text{V}$
		P-Ch	—	—	-100		$V_{\text{GS}} = -20\text{V}$
	Gate-to-Source Reverse Leakage	N-Ch	—	—	-100		$V_{\text{GS}} = -20\text{V}$
		P-Ch	—	—	100		$V_{\text{GS}} = 20\text{V}$
g_{fs}	Forward Transconductance	N-Ch	8.2	—	—	S	$V_{\text{DS}} = 15\text{V}, I_D = 5.4\text{A}$
		P-Ch	4.1	—	—		$V_{\text{DS}} = -15\text{V}, I_D = -3.7\text{A}$
Q_g	Total Gate Charge	N-Ch	—	6.8	14	nC	N-Channel $V_{\text{GS}} = 10\text{V}, V_{\text{DS}} = 15\text{V}, I_D = 6.8\text{A}$
		P-Ch	—	8.1	16		P-Channel
Q_{gs}	Gate-to-Source Charge	N-Ch	—	1.4	—		$V_{\text{GS}} = -10\text{V}, V_{\text{DS}} = -15\text{V}, I_D = -4.6\text{A}$
		P-Ch	—	1.3	—		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	0.98	—	Ω	
		P-Ch	—	2.1	—		
R_g	Gate Resistance	N-Ch	—	2.2	4.4		
		P-Ch	—	9.4	19		
$t_{\text{d(on)}}$	Turn-On Delay Time	N-Ch	—	5.1	—	ns	N-Channel $V_{\text{DD}} = 15\text{V}, V_{\text{GS}} = 4.5\text{V}$ ②
		P-Ch	—	8.0	—		$I_D = 1.0\text{A}, R_g = 6.2\Omega$
t_r	Rise Time	N-Ch	—	4.8	—		
		P-Ch	—	14	—		
$t_{\text{d(off)}}$	Turn-Off Delay Time	N-Ch	—	4.9	—	pF	P-Channel $V_{\text{DD}} = -15\text{V}, V_{\text{GS}} = -4.5\text{V}$ ②
		P-Ch	—	17	—		$I_D = -1.0\text{A}, R_g = 6.8\Omega$
t_f	Fall Time	N-Ch	—	3.9	—		
		P-Ch	—	15	—		
C_{iss}	Input Capacitance	N-Ch	—	398	—		N-Channel $V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 15\text{V}, f = 1.0\text{MHz}$
		P-Ch	—	383	—		P-Channel
C_{oss}	Output Capacitance	N-Ch	—	82	—		$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = -15\text{V}, f = 1.0\text{KHz}$
		P-Ch	—	104	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	36	—		
		P-Ch	—	64	—		

Diode Characteristics

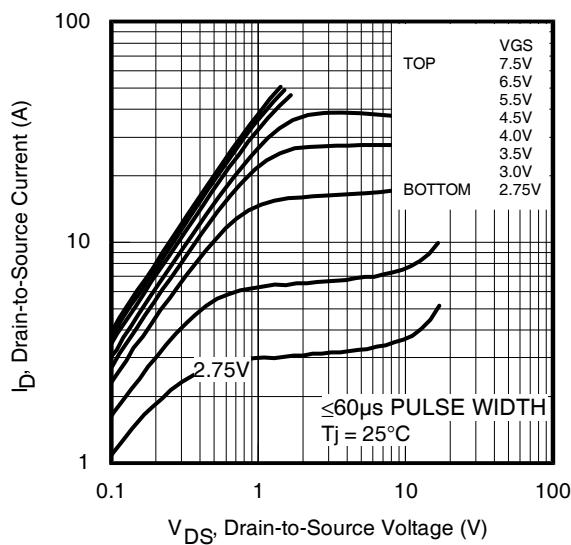
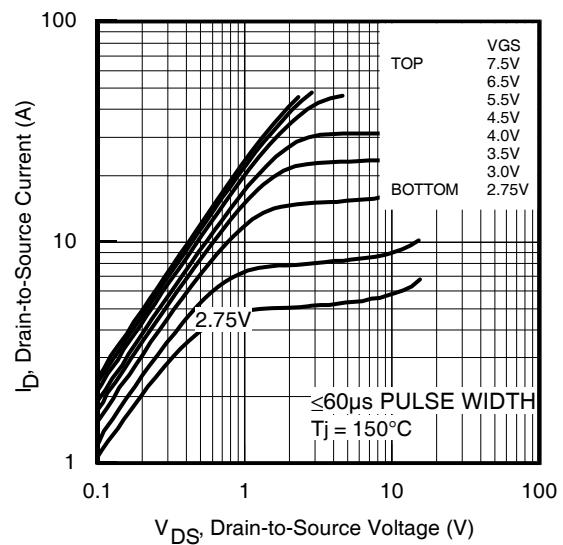
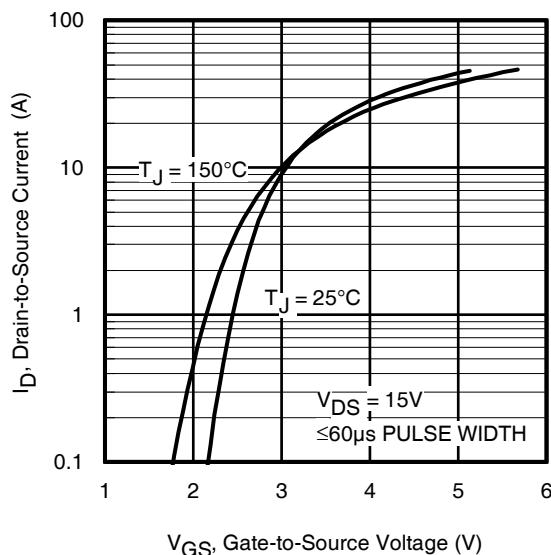
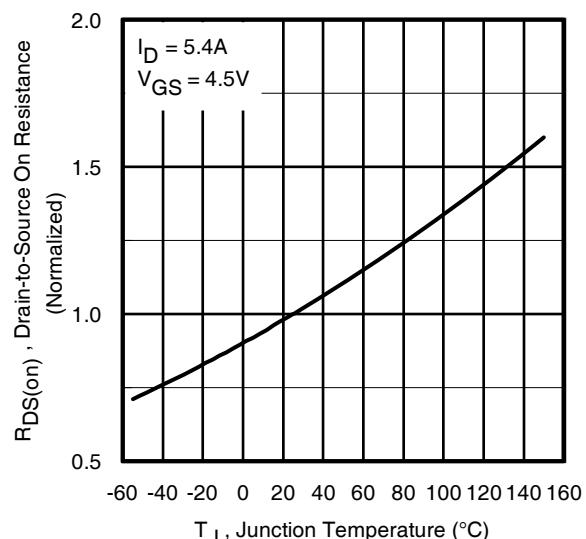
	Parameter		Min.	Typ.	Max.	Units	Conditions
I_s	Continuous Source Current (Body Diode)	N-Ch	—	—	2.0	A	
		P-Ch	—	—	-2.0		
I_{SM}	Pulsed Source Current (Body Diode)	N-Ch	—	—	34		
		P-Ch	—	—	-23		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 2.0\text{A}, V_{\text{GS}} = 0\text{V}$ ②
		P-Ch	—	—	-1.2		$T_J = 25^\circ\text{C}, I_S = -2.0\text{A}, V_{\text{GS}} = 0\text{V}$ ②
t_{rr}	Reverse Recovery Time	N-Ch	—	8.4	13	ns	N-Channel: $T_J = 25^\circ\text{C}, I_F = 2.0\text{A}, V_{\text{DD}} = 15\text{V}, di/dt = 102/\mu\text{s}$ ②
		P-Ch	—	11	17		P-Channel: $T_J = 25^\circ\text{C}, I_F = -2.0\text{A}, V_{\text{DD}} = -15\text{V}, di/dt = 102/\mu\text{s}$ ②
Q_{rr}	Reverse Recovery Charge	N-Ch	—	2.3	3.5	nC	
		P-Ch	—	4.8	7.2		

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 16)
 ② Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.

- ③ Surface mounted on 1 in square Cu board
 ④ R_θ is measured at T_J approximately 90°C

N-Channel

**Fig 1.** Typical Output Characteristics**Fig 2.** Typical Output Characteristics**Fig 3.** Typical Transfer Characteristics**Fig 4.** Normalized On-Resistance vs. Temperature

N-Channel

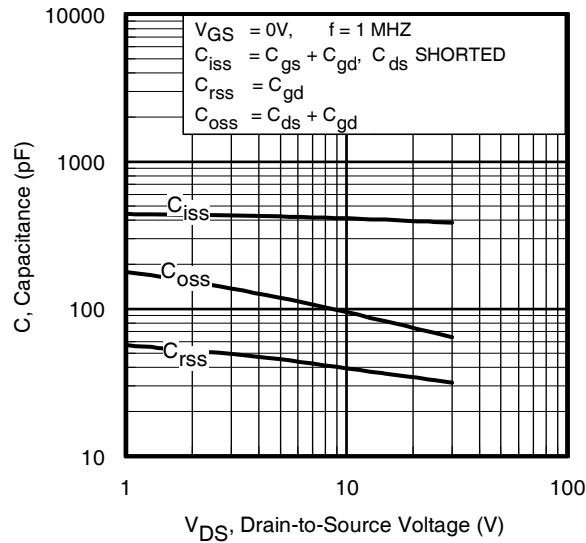


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

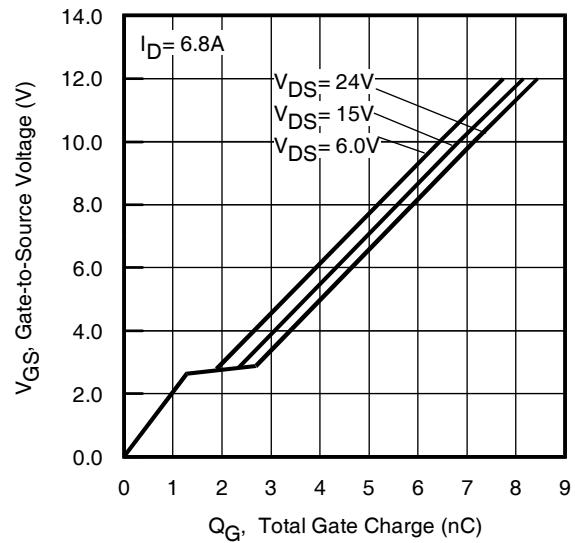


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

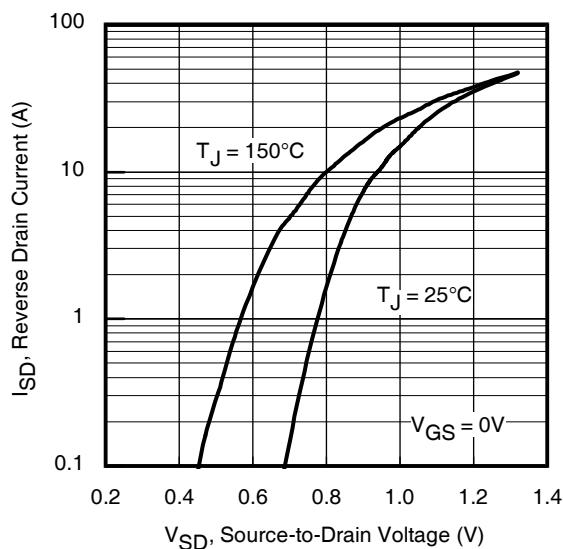


Fig 7. Typical Source-Drain Diode
Forward Voltage

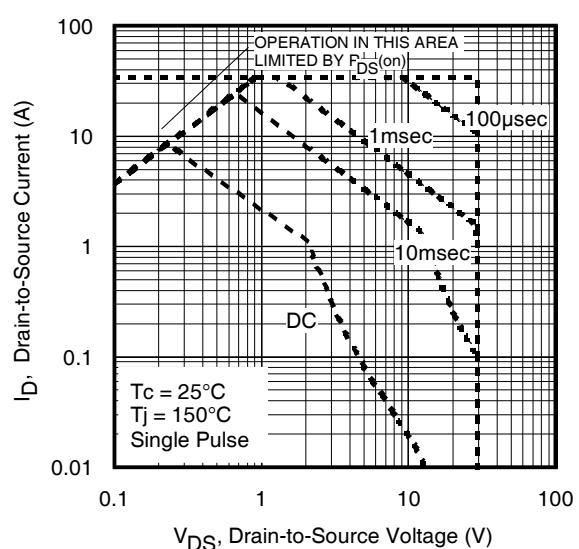


Fig 8. Maximum Safe Operating Area

N-Channel

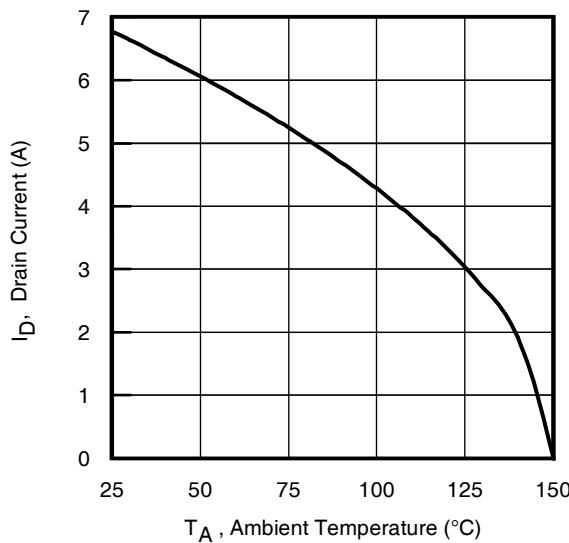


Fig 9. Maximum Drain Current vs. Ambient Temperature

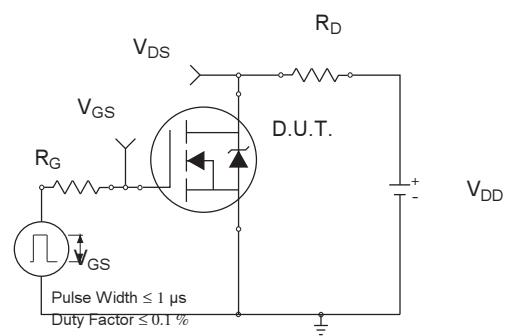


Fig 10a. Switching Time Test Circuit

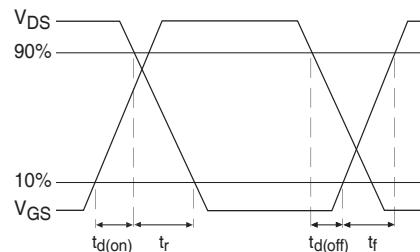


Fig 10b. Switching Time Waveforms

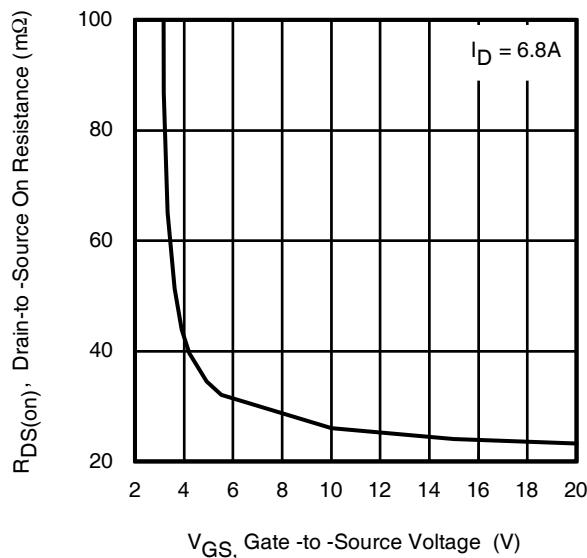


Fig 11. Typical On-Resistance vs. Gate Voltage

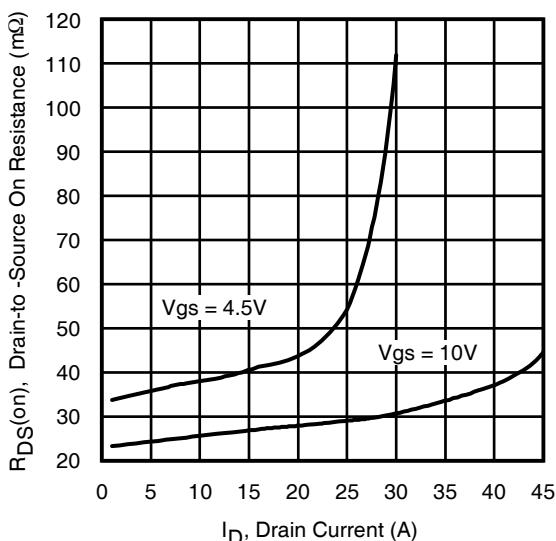
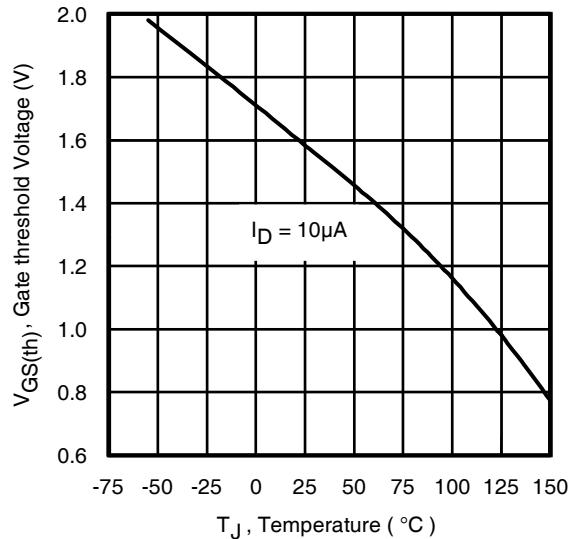
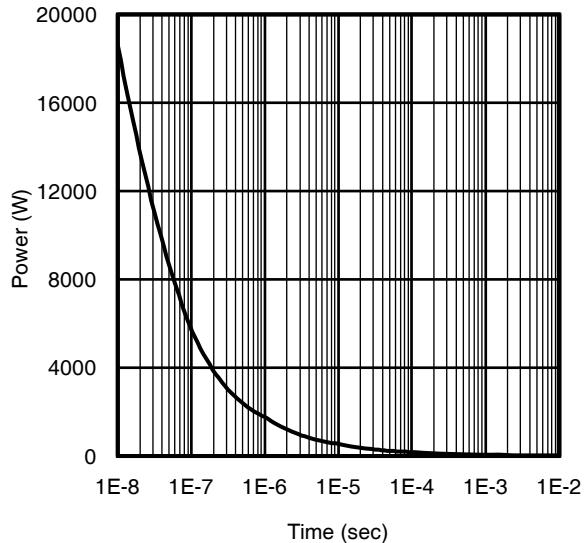
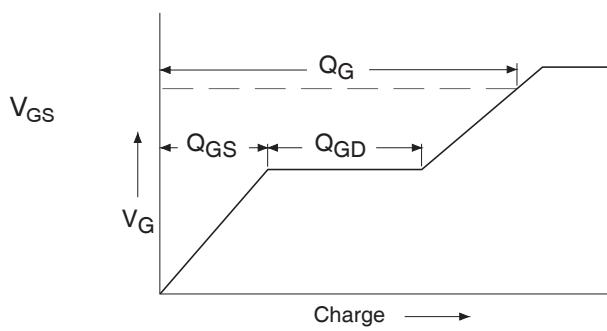
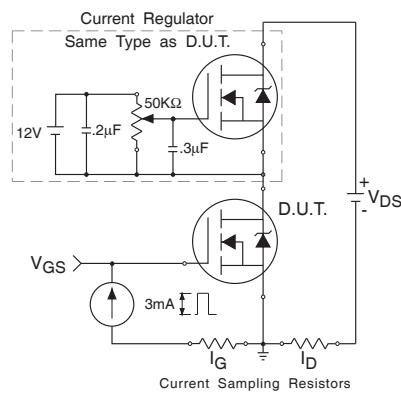


Fig 12. Typical On-Resistance vs. Drain Current

N-Channel

**Fig 13.** Threshold Voltage vs. Temperature**Fig 14.** Typical Power vs. Time**Fig 15a.** Basic Gate Charge Waveform**Fig 15b.** Gate Charge Test Circuit

N and P-Channel

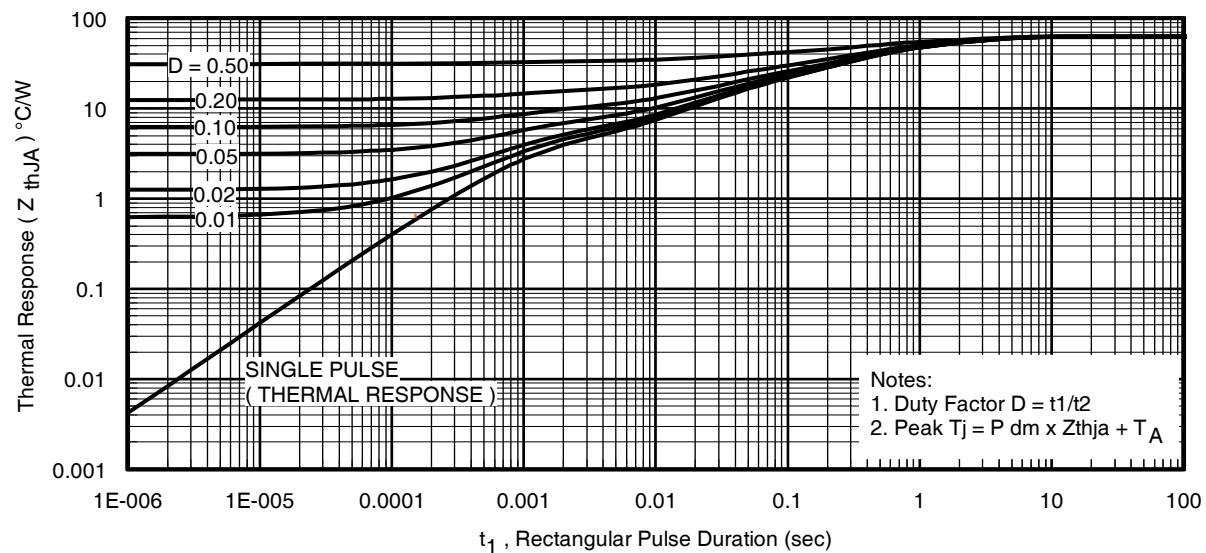
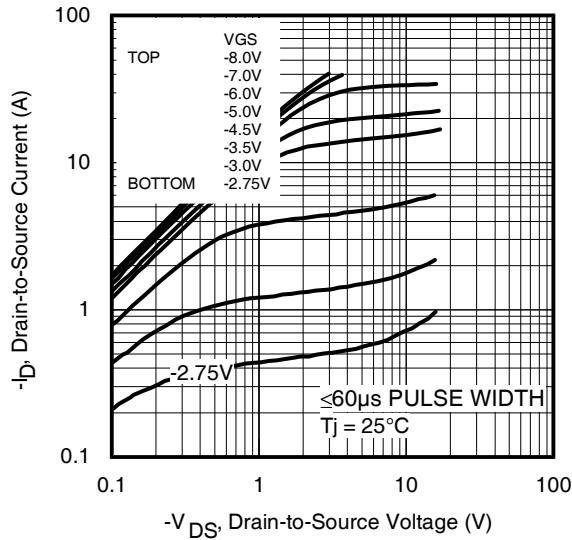
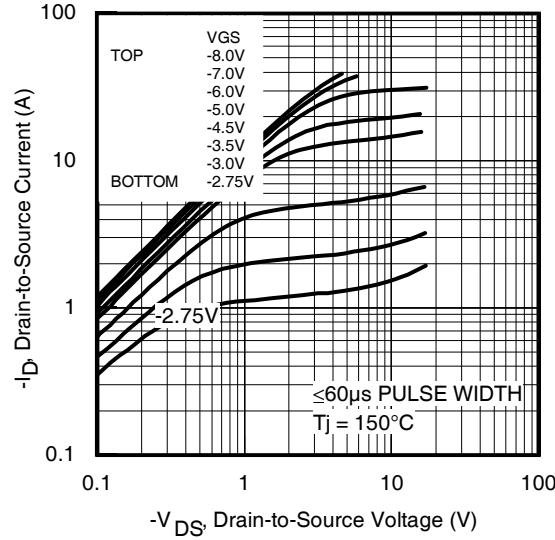
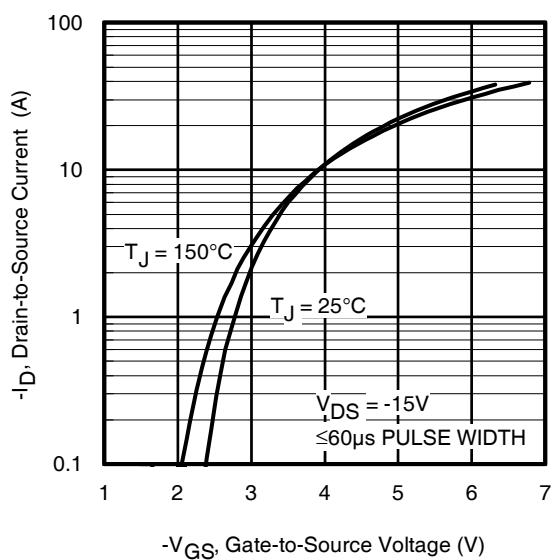
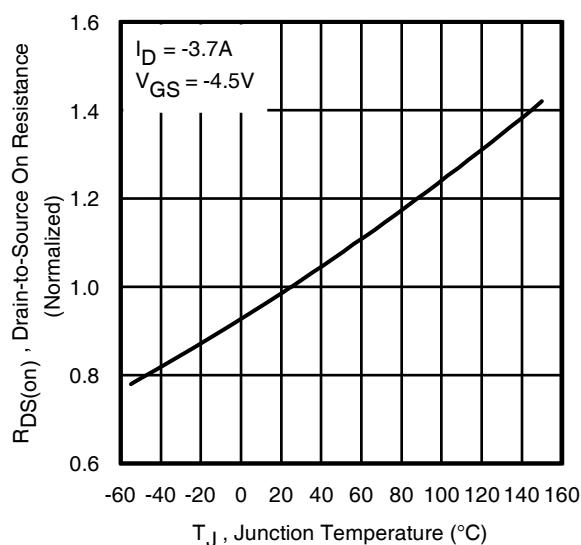


Fig 16. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

P-Channel

**Fig 17.** Typical Output Characteristics**Fig 18.** Typical Output Characteristics**Fig 19.** Typical Transfer Characteristics**Fig 20.** Normalized On-Resistance vs. Temperature

P-Channel

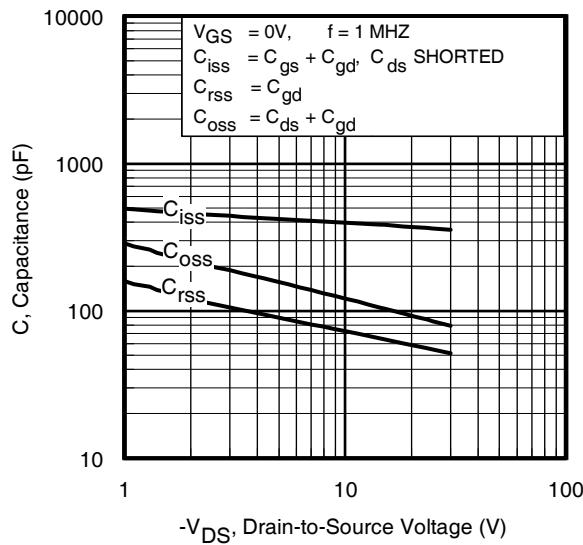


Fig 21. Typical Capacitance vs.
Drain-to-Source Voltage

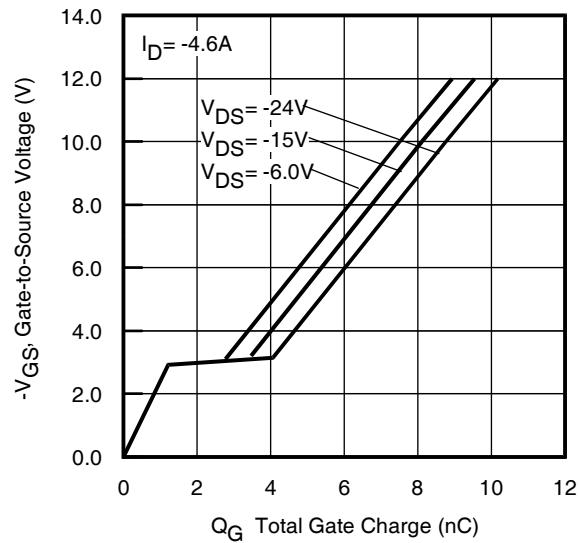


Fig 22. Typical Gate Charge vs.
Gate-to-Source Voltage

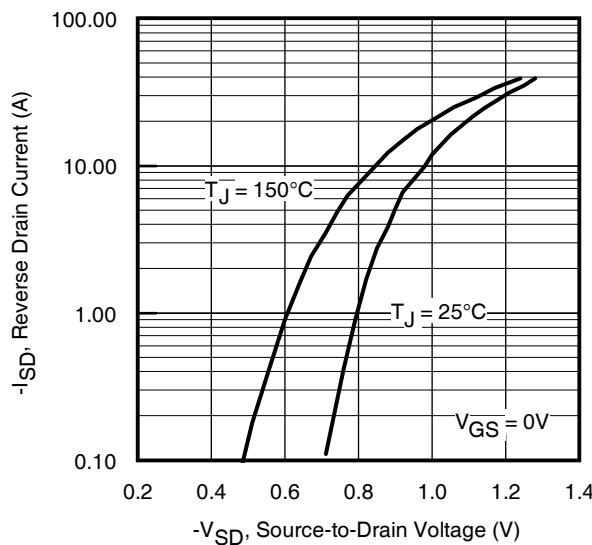


Fig 23. Typical Source-Drain Diode
Forward Voltage

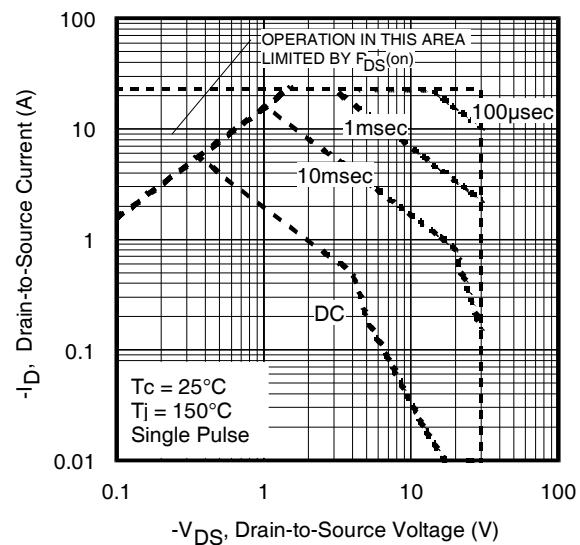


Fig 24. Maximum Safe Operating Area

P-Channel

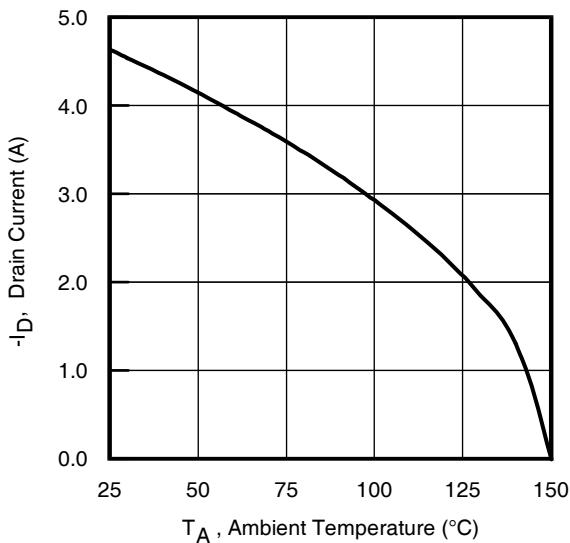


Fig 25. Maximum Drain Current vs. Ambient Temperature

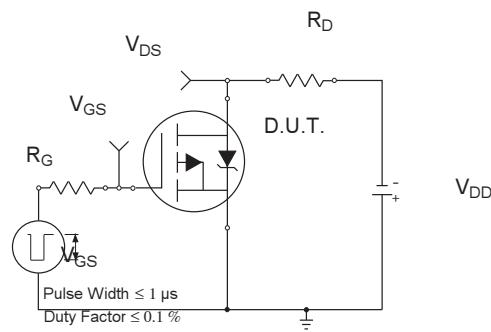


Fig 26a. Switching Time Test Circuit

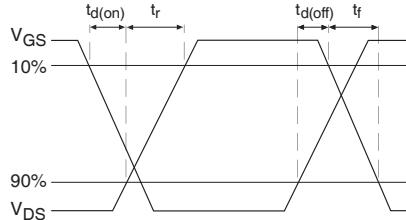


Fig 26b. Switching Time Waveforms

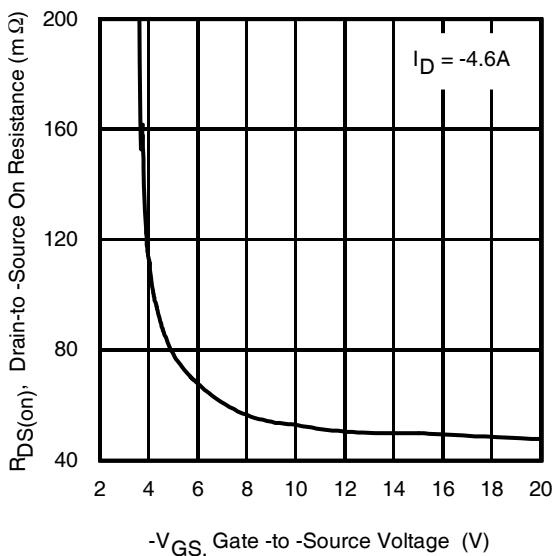


Fig 27. Typical On-Resistance vs. Gate Voltage

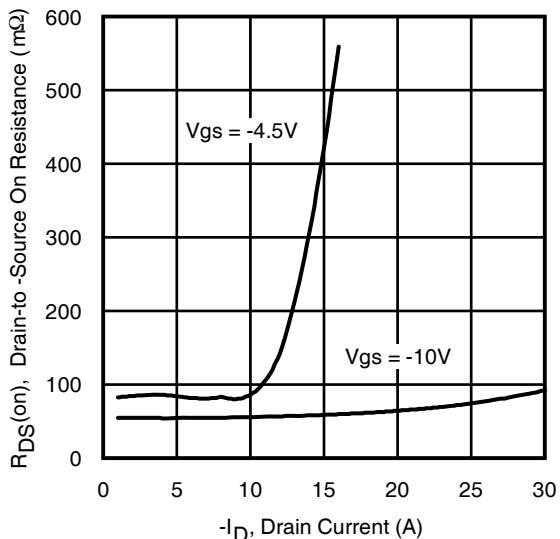
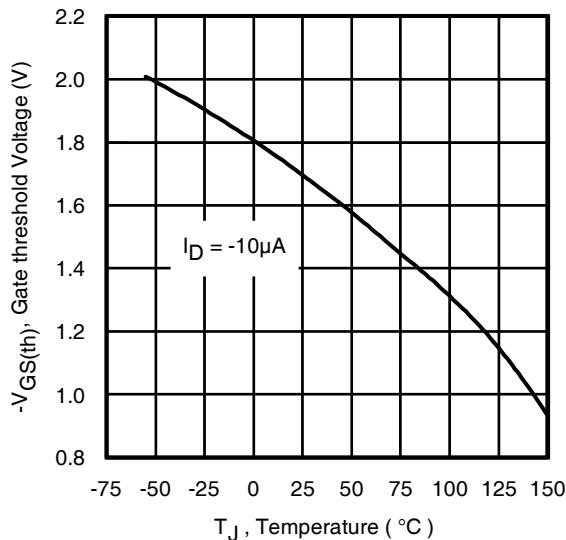
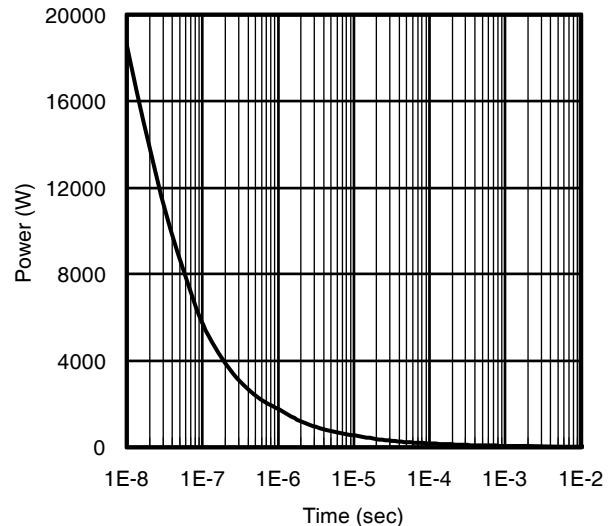
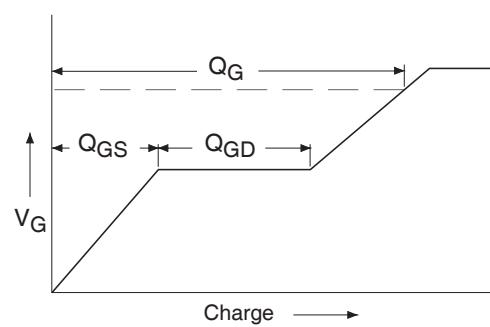
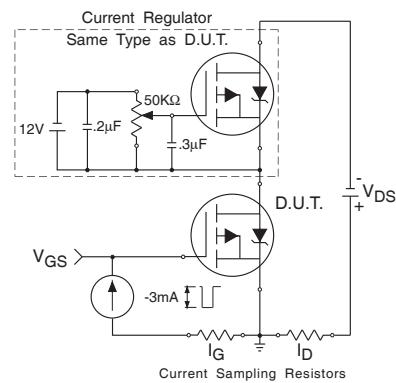
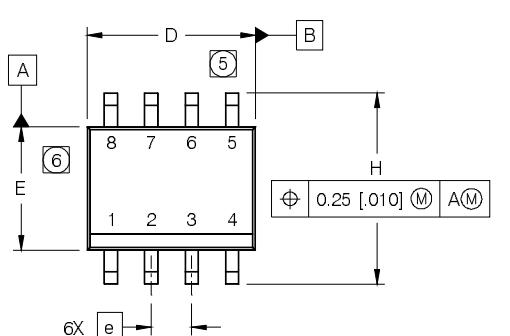


Fig 28. Typical On-Resistance vs. Drain Current

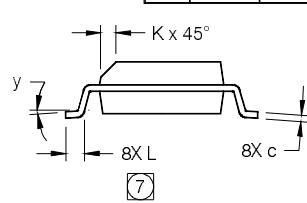
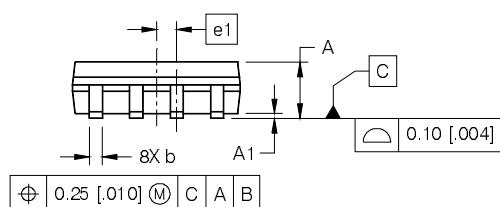
P-Channel

**Fig 29.** Threshold Voltage vs. Temperature**Fig 30.** Typical Power vs. Time**Fig 31a.** Basic Gate Charge Waveform**Fig 31b.** Gate Charge Test Circuit

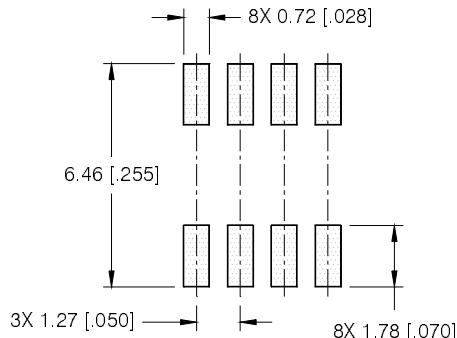
SO-8 Package Details



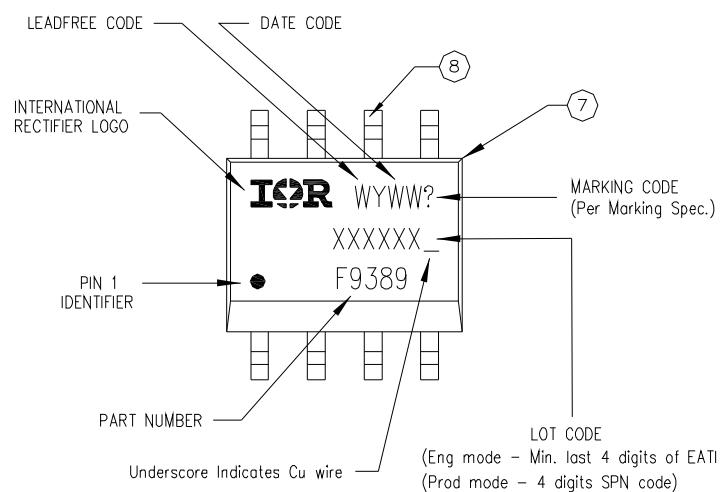
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A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050	BASIC	1.27	BASIC
e1	.025	BASIC	0.635	BASIC
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



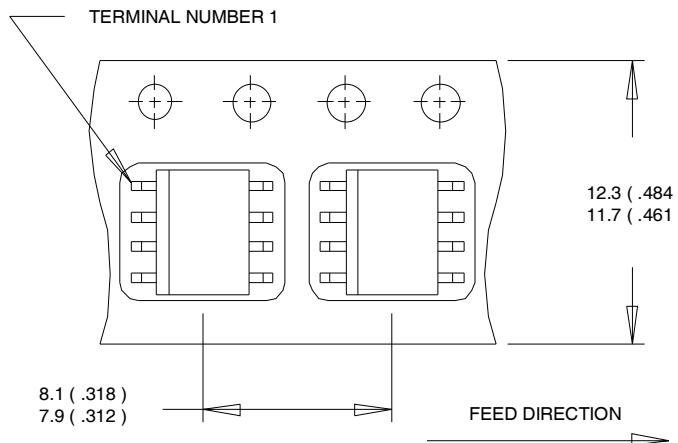
FOOTPRINT



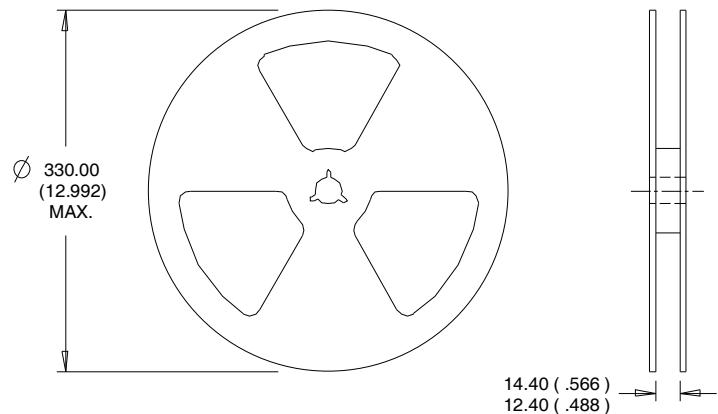
SO-8 Part Marking



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package>

Tape and Reel**NOTES:**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Qualification information[†]

Qualification level	Consumer (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	SO-8	MSL1 (per JEDEC J-STD-020D ^{††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site:

<http://www.irf.com/product-info/reliability/>

^{††} Applicable version of JEDEC standard at the time of product release.

International
IR Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245
To contact International Rectifier, please visit <http://www.irf.com/photo-call/>