CIPOS™ Mini IM564

IM564-X6D/IM564-X6DS

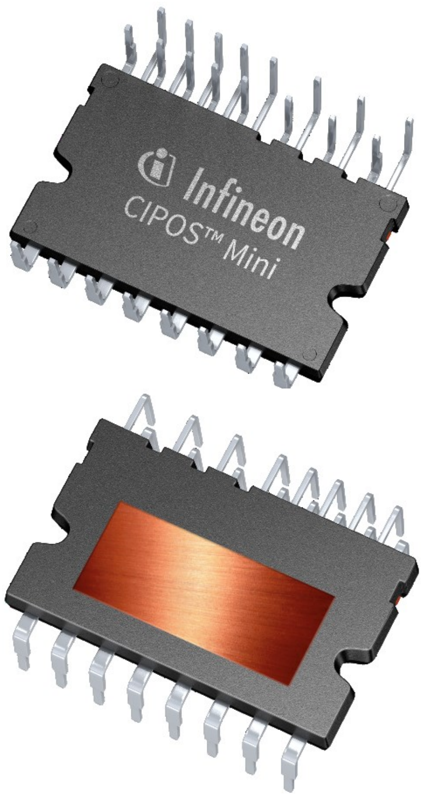
Description

The CIPOS™ IM564 product family (PFC-integrated IPM) offers the chance for integrating various power and control components of inverter and single boost PFC stages to increase reliability and optimize PCB size and system cost. It is designed to control three-phase motors in variable speed drives for applications such as air-conditioners and pumps. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also less EMI and overload protection. To deliver excellent electrical performance, the IM564 product family incorporated Infineon's leading-edge TRENCHSTOP™ IGBTs, anti-parallel diodes, and an optimized SOI gate driver for three-phase inverter stage, and a CoolMOS™ Power MOSFET and a rapid switching emitter controlled diode for single boost PFC stage.

Features

Package

- Fully isolated Dual In-Line molded module
- Very low thermal resistance due to DCB substrate
- Lead-free terminal plating; RoHS compliant



Inverter

- TRENCHSTOP™ IGBTs for Inverter
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative VS potential up to -11 V for signal transmission at VBS = 15 V
- Integrated bootstrap functionality
- Over current shutdown
- Built-in NTC thermistor for temperature monitor
- Under-voltage lockout at all channels
- Low-side common emitter
- Sleep function
- Fast track shutdown
- Cross-conduction prevention
- All of 6 switches turn off during protection

PFC

- CoolMOS™ Power MOSFET for PFC
- Rapid switching emitter controlled diode

Potential applications

- Air-conditioners, Fans, Pumps, Low power motor drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table 1 Product Information

Base Part Number	Package Type	Standard Pack		Remarks
		Form	MOQ	
IM564-X6D	DIP 36x21D	14 pcs / Tube	280 pcs	
IM564-X6DS	DIP 36x21D	14 pcs / Tube	280 pcs	Extended stand-off

Table of Contents

1 Internal Electrical Schematic

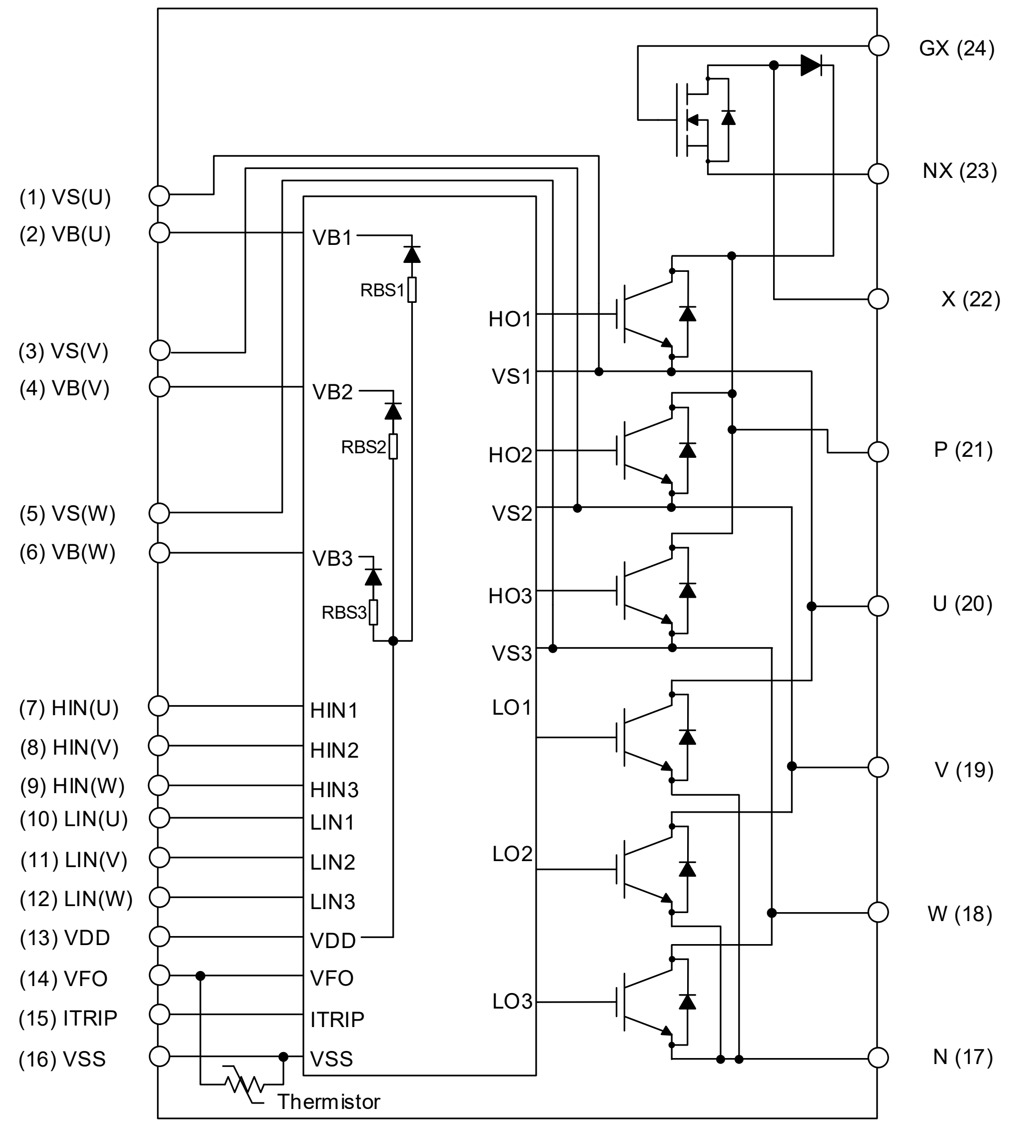


Figure 1 Internal electrical schematic

2 Pin Description

2.1 Pin Assignment

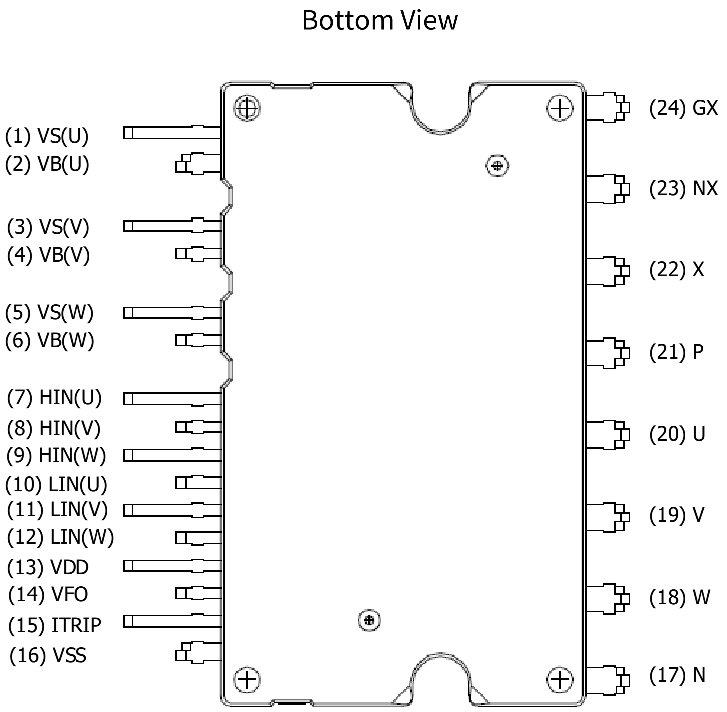


Figure 2 Pin configuration

Table 2 Pin assignment

Pin Number	Pin name	Pin Description
1	VS(U)	U-phase high-side floating IC supply offset voltage
2	VB(U)	U-phase high-side floating IC supply voltage
3	VS(V)	V-phase high-side floating IC supply offset voltage
4	VB(V)	V-phase high-side floating IC supply voltage
5	VS(W)	W-phase high-side floating IC supply offset voltage
6	VB(W)	W-phase high-side floating IC supply voltage
7	HIN(U)	U-phase high-side gate driver input
8	HIN(V)	V-phase high-side gate driver input
9	HIN(W)	W-phase high-side gate driver input
10	LIN(U)	U-phase low-side gate driver input
11	LIN(V)	V-phase low-side gate driver input
12	LIN(W)	W-phase low-side gate driver input
13	VDD	Low-side control supply
14	VFO	Fault output / Temperature monitor
15	ITRIP	Over-current shutdown input
16	VSS	Low-side control negative supply
17	N	Low-side emitter

Pin Number	Pin name	Pin Description
18	W	Motor W-phase output
19	V	Motor V-phase output
20	U	Motor U-phase output
21	P	Positive output voltage / Positive bus input voltage
22	X	PFC MOSFET drain
23	NX	PFC MOSFET source
24	GX	PFC MOSFET gate

2.2 Pin Description

HIN(U, V, W) and LIN(U, V, W) (Low-side and high-side control pins, Pin 7 - 12)

These pins are positive logic and they are responsible for the control of the integrated IGBTs. The Schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. A pull-down resistor of about 5 kΩ is internally provided to pre-bias input during supply start-up, and a zener clamp is provided to protect the pin. Negative pulses down to an absolute minimum of -5.5 V are allowed that offers an outstanding robustness. Input Schmitt-trigger and noise filter provide noise rejection to short input pulses.

The noise filter suppresses control pulses shoter than the filter time $t_{FIL,IN}$. The Figure 4 describes how the filter works. An input pulse-width shorter than 1 µs is not recommended.

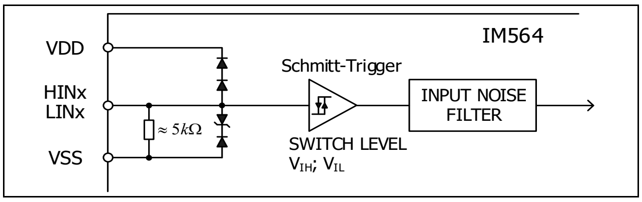


Figure 3 Input pin structure

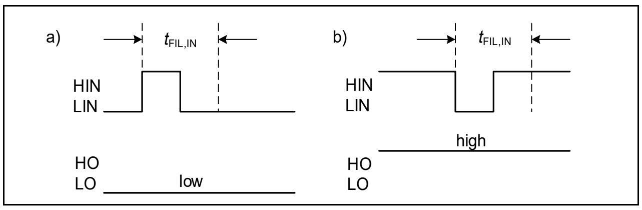


Figure 4 Input filter timing diagram

The integrated gate driver additionally provides a shoot-through prevention capability that avoids the simultaneous on-states of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When both inputs of the same leg are activated, only formerly activated one is remained activated so that the leg is kept steadily in a safe state.
A minimum deadtime insertion of typically 360 ns is also provided by driver, in order to reduce cross-conduction of the IGBTs.

VFO (Fault-output and NTC, Pin 14)

The VFO pin indicates a module failure in case of under voltage at pin VDD or in case of triggered over current detection at ITRIP. An external pull-up resistor is required.

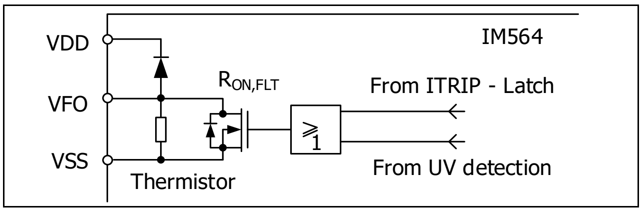


Figure 5 Internal circuit at pin VFO

The sleep function is activated after each trigger of ITRIP or under-voltage lockout. A new edge input signal is mandatory to activate gate drives after falut-clear time as shown in Figure 11.

ITRIP (Over current detection function, Pin 15)

The IM564 product family provides an over current detection function by connecting the ITRIP input with the IGBT current feedback. The ITRIP comparator threshold (typ. 0.525 V) is referenced to VSS. An input noise filter ($t_{ITRIPMIN}$ = typ. 300 ns) prevents the driver to detect false over-current events.
Over current detection generates a shutdown of outputs of the gate driver. Fast track shutdown

function allows low-side outputs to be turned off faster than high-side outputs about 200 ns.
The fault-clear time is set to minimum 100 µs.

VDD, VSS (Low-side control supply and reference, Pin 13, 16)

VDD is the control supply and it provides power both to input logic and to output stage. Input logic is referenced to VSS ground.
The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 12.4 V is present.
The gate driver shuts down all the outputs, when the VDD supply voltage is below V_{DDUV-} = 11.5 V. This prevents the IGBTs from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

VB(U, V, W) and VS(U, V, W) (High-side supplies, Pin 1 - 6)

VB to VS is the high-side supply voltage. The high-side circuit can float with respect to VSS following the high-side IGBT emitter voltage.
Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.
The under-voltage detection operates with a rising supply threshold of typical V_{BSUV+} = 11.5 V and a falling threshold of V_{BSUV-} = 10.7 V.
VS(U, V, W) provide a high robustness against negative voltage in respect of VSS of -50 V transiently. This ensures very stable designs even under harsh conditions.

N (Low-side emitter, Pin 17)

The low-side common emitter is available for current measurement. It is recommended to keep the connection to pin VSS as short as possible to avoid unnecessary inductive voltage drops.

W, V, U (High-side emitter and low-side collector, Pin 18 - 20)

These pins are connected to motor U, V, W input pins

P (Positive bus input voltage, Pin 21)

The high-side IGBTs and PFC diode cathode are connected to the bus voltage. It is noted that the bus voltage does not exceed 450 V.

X, NX, GX (Single boost PFC, Pins 22-24)

These pins are drain, source, and gate of MOSFET for single boost PFC stage.

3 Absolute Maximum Ratings

(V_{DD} = 15 V, V_{GE} = 15 V and T_J = 25°C, if not stated otherwise)

3.1 Module Section

Description	Symbol	Condition	Value	Unit
Storage temperature range	T_{STG}		-40 ~ 125	°C
Operating case temperature	T_C	Refer to Figure 7	-40 ~ 125	°C
Operating junction temperature	T_J		-40 ~ 150	°C
Isolation test voltage	V_{ISO}	1 min, RMS, f = 60 Hz	2000	V

3.2 Inverter Section

Description	Symbol	Condition	Value	Unit
Max. blocking voltage	V_{CES}	I_C = 250 µA	600	V
DC link supply voltage of P-N	V_{PN}	Applied between P-N	450	V
DC link supply voltage (surge) of P-N	$V_{PN(surge)}$	Applied between P-N	500	V
Continuous collector current	I_C	T_C = 25°C, T_J < 150°C	±20	A
		T_C = 80°C, T_J < 150°C	±15	
Maximum peak collector current	$I_{C(peak)}$	T_C = 25°C, T_J < 150°C less than 1 ms	±40	A
Power dissipation per IGBT	P_{tot}		63.1	W
Short circuit withstand time[1]	t_{SC}	$V_{DC} \leq$ 400V, T_J = 150°C	5	µs

3.3 Control Section

Description	Symbol	Condition	Value	Unit
High-side offset voltage	V_S		600	V
Repetitive peak reverse voltage of bootstrap diode	V_{RRM}		600	V
Module supply voltage	V_{DD}		-1 ~ 20	V
High-side floating supply voltage (V_B reference to V_S)	V_{BS}		-1 ~ 20	V
Input voltage(LIN, HIN, ITRIP)	V_{IN}		-5.5 ~ V_{DD}+0.5	V

[1] Allowed number of short circuits: < 1000; time between short circuits: > 1 s.

3.4 PFC Section

Description	Symbol	Condition	Value	Unit
Max. blocking voltage	V_{DSS}	V_{GS} = 0 V, I_D = 1 mA	600	V
Gate-source voltage	V_{GS}	DC	±20	V
		AC (f > 1 Hz)	±30	
Continuous drain current	I_D	T_C = 25°C, T_J ≤ 150°C	±20	A
		T_C = 80°C, T_J ≤ 150°C	±15	
Maximum peak drain current	$I_{D(peak)}$	T_J ≤ 150°C, T_C = 25°C	±40	A
Power dissipation	P_{tot}		88.6	W

4 Thermal Characteristics

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Single IGBT thermal resistance, junction-case(Inverter)	R_{thJC}	High-side W-phase IGBT (See Figure 7 for T_C measurement point)			1.98	K/W
Single Diode thermal resistance, junction-case(Inverter)	$R_{thJC,D}$	High-side W-phase Diode			3.24	K/W
Single MOSFET thermal resistance, junction-case(PFC)	R_{thJC}	(See Figure 7 for T_C measurement point)			1.41	K/W
Single Diode thermal resistance, junction-case(PFC)	$R_{thJC,D}$				2.34	K/W

5 Recommended Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

Description	Symbol	Value			Unit
		Min.	Typ.	Max.	
DC link supply voltage of P-N	V_{PN}	0	-	450	V
Low-side supply voltage	V_{DD}	13	15	17.5	V
High-side floating supply voltage (V_B vs. V_S)	V_{BS}	13	-	17.5	V
Logic input voltages LIN, HIN, ITRIP	V_{IN} V_{ITRIP}	0	-	5	V
Inverter PWM carrier frequency	f_{PWM}	-	-	20	kHz
PFC switching frequency	$f_{PWM(PFC)}$			150	kHz
External deadtime between HIN and LIN	DT	1.5	-	-	µs
Voltage between VSS – N and NX (including surge)	V_{COMP}	-5	-	5	V
Minimum input pulse width	$PW_{IN(ON)}$ $PW_{IN(OFF)}$	1	-	-	µs
Control supply variation	ΔV_{BS}, ΔV_{DD}	-1 -1	- -	1 1	V/µs
PFC MOSFET gate-source voltage	V_{GE}	10	15	18	V
PFC MOSFET external gate parameters	R_G	-	5.1	-	Ω
	C_{GS}	-	4.7	-	nF
	R_{GS}	-	10	-	kΩ

6 Static Parameters

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

6.1 Inverter Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter voltage	$V_{CE(Sat)}$	I_C = 20 A, T_J = 25°C I_C = 20 A, T_J = 150°C	- -	1.75 2.0	2.05 -	V
Collector-emitter leakage current	I_{CES}	V_{CE} = 600 V	-	-	1	mA
Diode forward voltage	V_F	I_F = 20 A, T_J = 25°C I_F = 20 A, T_J = 150°C	- -	2.2 2.15	2.8 -	V

6.2 Control Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Logic "1" input voltage (LIN, HIN)	V_{IH}		1.7	2.0	2.3	V
Logic "0" input voltage (LIN, HIN)	V_{IL}		0.7	0.9	1.1	V
ITRIP positive going threshold	$V_{IT,TH+}$		475	525	570	mV
ITRIP input hysteresis	$V_{IT,HYS}$		45	70	-	mV
VDD and VBS supply under voltage positive going threshold	V_{DDUV+}		11.5	12.4	13.1	V
	V_{BSUV+}		10.6	11.5	12.2	
VDD and VBS supply under voltage negative going threshold	V_{DDUV-}		10.6	11.5	12.3	V
	V_{BSUV-}		9.7	10.7	11.7	
VDD and VBS supply under voltage lockout hysteresis	V_{DDUVH} V_{BSUVH}		0.5	0.9	-	V
Quiescent VB_x supply current (V_{Bx} only)	I_{QBS}	H_{IN} = 0 V	-	-	300	µA
Quiescent VDD supply current (V_{DD} only)	I_{QDD}	L_{IN} = 0 V, H_{INX} = 5 V	-	-	1.1	mA
Input bias current for LIN, HIN	I_{IN+}	V_{IN} = 5 V	-	1.1	1.7	mA
Input bias current for ITRIP	I_{ITRIP+}	V_{ITRIP} = 5 V	-	68	185	µA
Input bias current for VFO	I_{FO}	V_{FO} = 5 V, V_{ITRIP} = 0 V	-	60	-	µA
VFO output voltage	V_{FO}	I_{FO} = 10 mA, V_{ITRIP} = 1 V	-	0.35	-	V
Bootstrap diode forward voltage	V_{F_BSD}	I_F = 0.3 mA	-	1.0	-	V
Bootstrap diode resistance	R_{BSD}	V_{F1} = 4 V, V_{F2} = 5 V	-	37	-	Ω

6.3 PFC Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
PFC MOSFET drain-source on-state resistance	$R_{DS(on)}$	I_D = 20 A, V_{GS}= 15 V, T_J = 25°C I_D = 20 A, V_{GS}= 15 V, T_J = 150°C	- -	0.086 0.156	0.115 -	Ω
PFC MOSFET drain-source leakage current	I_{DSS}	V_{DS} = 600 V, V_{GS}= 0 V	-	-	1	mA
PFC diode forward voltage	V_F	I_F = 20 A, T_J = 25°C I_F = 20 A, T_J = 150°C	- -	1.4 1.3	- -	V

7 Dynamic Parameters

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

7.1 Inverter Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Turn-on propagation delay time	t_{on}	$V_{LIN, HIN}$ = 5 V, I_C = 20 A, V_{DC} = 300 V	-	740	-	ns
Turn-on rise time	t_r		-	60	-	ns
Turn-on switching time	$t_{c(on)}$		-	200	-	ns
Reverse recovery time	t_{rr}		-	215	-	ns
Turn-off propagation delay time	t_{off}	$V_{LIN, HIN}$ = 0 V, I_C = 20 A, V_{DC} = 300 V	-	860	-	ns
Turn-off fall time	t_f		-	20	-	ns
Turn-off switching time	$t_{c(off)}$		-	65	-	ns
Short circuit propagation delay time	t_{SCP}	From $V_{IT,TH+}$ to 10% I_{SC}	-	1600	-	ns
IGBT turn-on energy (includes reverse recovery of diode)	E_{on}	V_{DC} = 300 V, V_{DD} = 15 V, I_C = 20 A T_J = 25°C T_J = 150°C	- -	710 780	- -	µJ
IGBT turn-off energy	E_{off}	V_{DC} = 300 V, V_{DD} = 15 V, I_C = 20 A T_J = 25°C T_J = 150°C	- -	250 350	- -	µJ
Diode recovery energy	E_{rec}	V_{DC} = 300 V, V_{DD} = 15 V, I_C = 20 A T_J = 25°C T_J = 150°C	- -	60 115	- -	µJ

7.2 Control Section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input filter time ITRIP	t_{ITRIP}	V_{ITRIP} = 1 V	-	530	-	ns
Input filter time at LIN, HIN for turn on and off	$t_{FIL,IN}$	$V_{LIN, HIN}$ = 0 V or 5 V	-	290	-	ns
Fault clear time after ITRIP-fault	t_{FLTCLR}		100	280	-	µs
ITRIP to Fault propagation delay	t_{FLT}	$V_{LIN, HIN}$ = 0 or $V_{LIN, HIN}$ = 5 V, V_{ITRIP} = 1 V	-	680	1000	ns
Internal deadtime	DT_{IC}		-	360	-	ns
Matching propagation delay time (On and Off) all channels	M_T	External dead time > 500 ns	-	20	-	ns

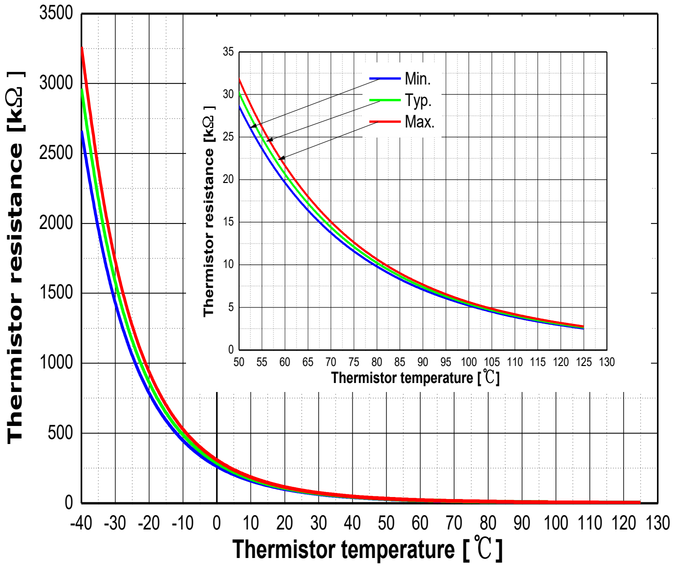
7.3 PFC Section

Description	Symbol	Condition	Value			Unit
			min	typ	max	
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DC} = 400 V, f = 250 kHz	-	1952	-	pF
Output capacitance	C_{oss}		-	33	-	
Effective output capacitance, energy related[1]	$C_{o(er)}$	V_{GS} = 0 V, V_{DC} = 0..400 V	-	62	-	
Gate charge total	Q_G	V_{DC} = 400 V, I_D = 10.5 A, V_{GS} = 0 to 10 V	-	45	-	nC
Turn-on delay time	$t_{d(on)}$	V_{DC} = 400 V, I_D = 20 A, R_G = 5.1 Ω, C_{GS} = 4.7 nF, R_{GS} = 10 kΩ, T_J = 25°C	-	30	-	ns
Turn-on rise time	t_r		-	25	-	ns
Turn-off delay time	$t_{d(off)}$		-	110	-	ns
Turn-off fall time	t_f		-	20	-	ns
Reverse recovery time	t_{rr}		-	45	-	ns
Turn-on energy	E_{on}	V_{DC} = 400 V, I_D = 20 A, R_G = 5.1 Ω, C_{GS} = 4.7 nF, R_{GS} = 10 kΩ T_J = 25°C T_J = 150°C	- -	310 390	- -	µJ
Turn-off energy	E_{off}	V_{DC} = 400 V, I_D = 20 A, R_G = 5.1 Ω, C_{GS} = 4.7 nF, R_{GS} = 10 kΩ T_J = 25°C T_J = 150°C	- -	110 130	- -	µJ
Diode recovery energy	E_{rec}	V_{DC} = 400 V, I_D = 20 A, R_G = 5.1 Ω, C_{GS} = 4.7 nF, R_{GS} = 10 kΩ T_J = 25°C T_J = 150°C	- -	90 140	- -	µJ

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.

8 Thermistor

Description	Condition	Symbol	Value			Unit
			Min.	Typ.	Max.	
Resistance	T_{NTC} = 25°C	R_{NTC}	-	85	-	kΩ
B-constant of NTC (Negative Temperature Coefficient)		B(25/100)	-	4092	-	K



T [°C]	Rmin. [kΩ]	Rtyp. [kΩ]	Rmax. [kΩ]
50	28.400	29.972	31.545
60	19.517	20.515	21.514
70	13.670	14.315	14.960
80	9.745	10.169	10.593
90	7.062	7.345	7.628
100	5.199	5.388	5.576
110	3.856	4.009	4.163
120	2.900	3.024	3.149
125	2.527	2.639	2.751

Figure 6 Thermistor resistance – temperature curve and table

(For more information, please refer to the application note 'AN2016-10 CIPOS Mini Technical description')

9 Mechanical Characteristics and Ratings

Description	Condition	Value			Unit
		Min.	Typ.	Max.	
Comparative Tracking Index (CTI)		600	-	-	V
Mounting torque	M3 screw and washer	0.49	-	0.78	Nm
Backside Curvature	Refer to Figure 8	-50	-	100	µm
Weight		-	6.83	-	g

10 Qualification Information

UL Certification	File number: E314539	
RoHS Compliant	Yes (Lead-free terminal plating)	
ESD	HBM(Human Body Model) Class as per JESD22-A114	2 (> 2000 V to < 4000 V)
	CDM(Charged Device Model) Class as per JESD22-C101	C3 (>= 1000 V)

11 Diagrams and Tables

11.1 T_C Measurement Point

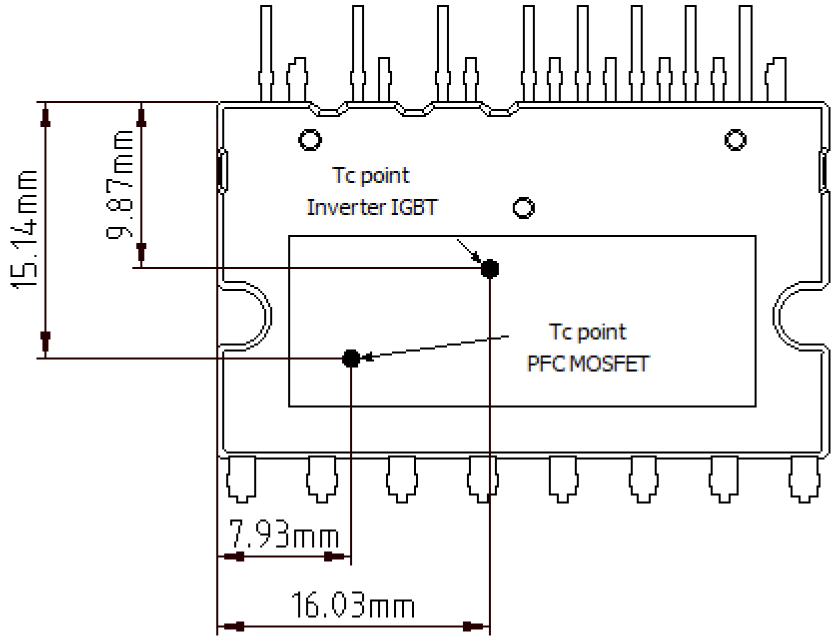


Figure 7 T_C measurement point[1]

11.2 Backside Curvature Measurment Point

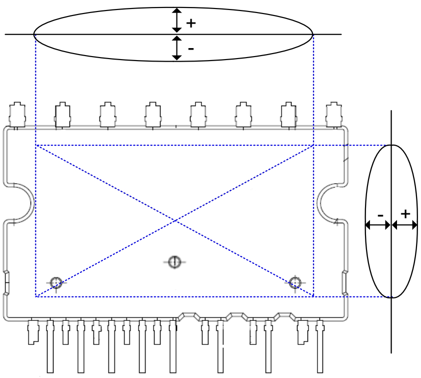


Figure 8 Backside curvature measurement position

[1]Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.

11.3 Switching Time Definition

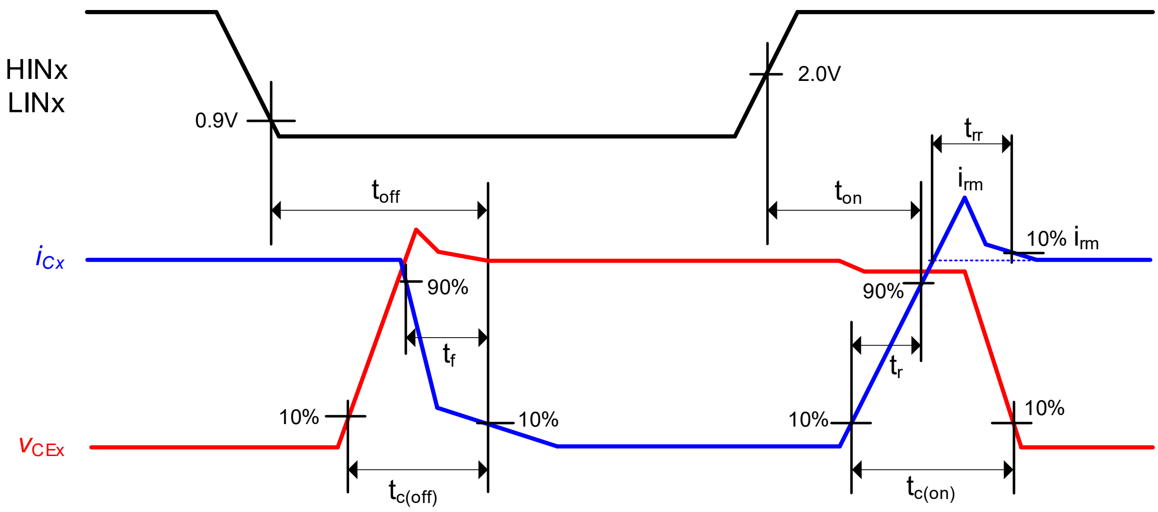


Figure 9 Switching times definition of inverter part

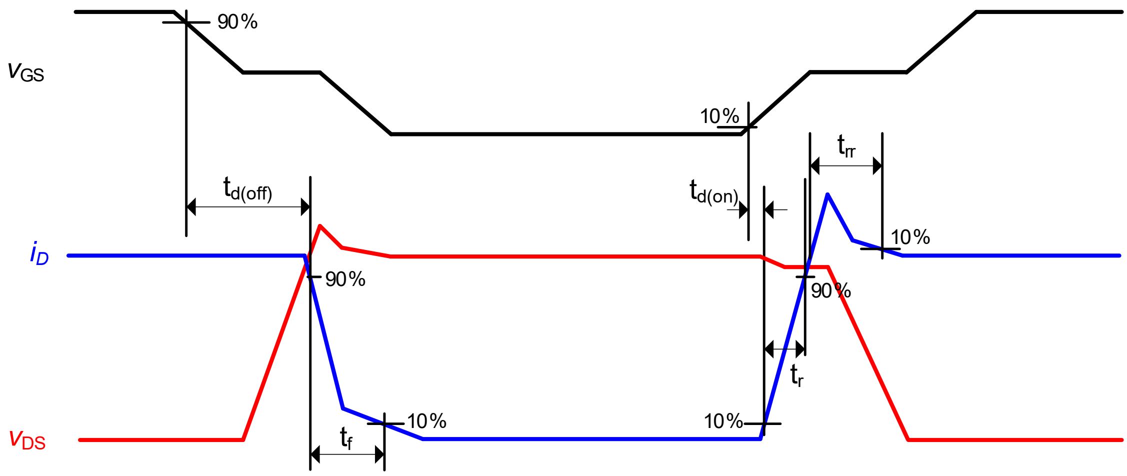


Figure 10 Switching times definition of PFC part

11.4 Sleep function timing diagram

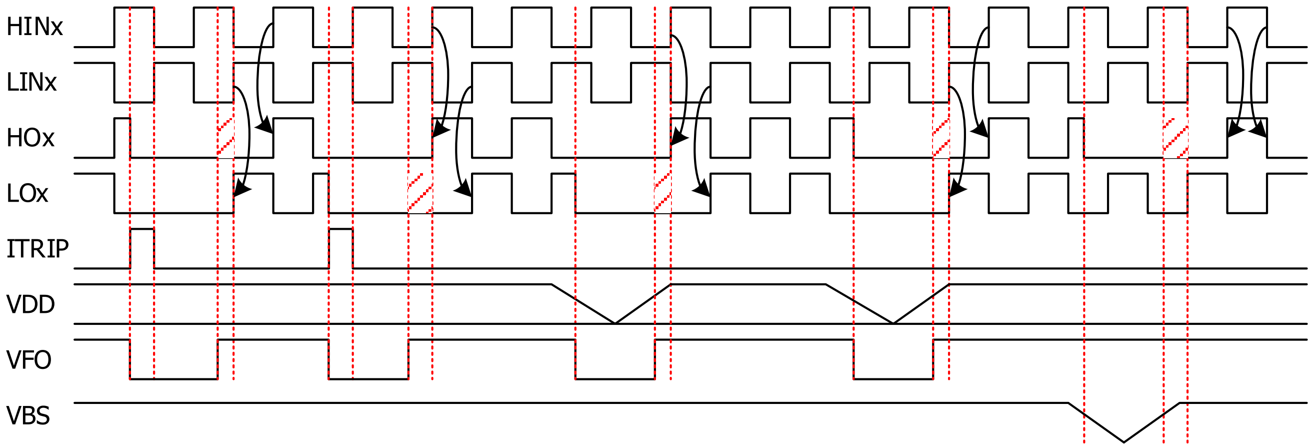


Figure 11 Sleep function timing diagram

12 Application Guide

12.1 Typical Application Schematic

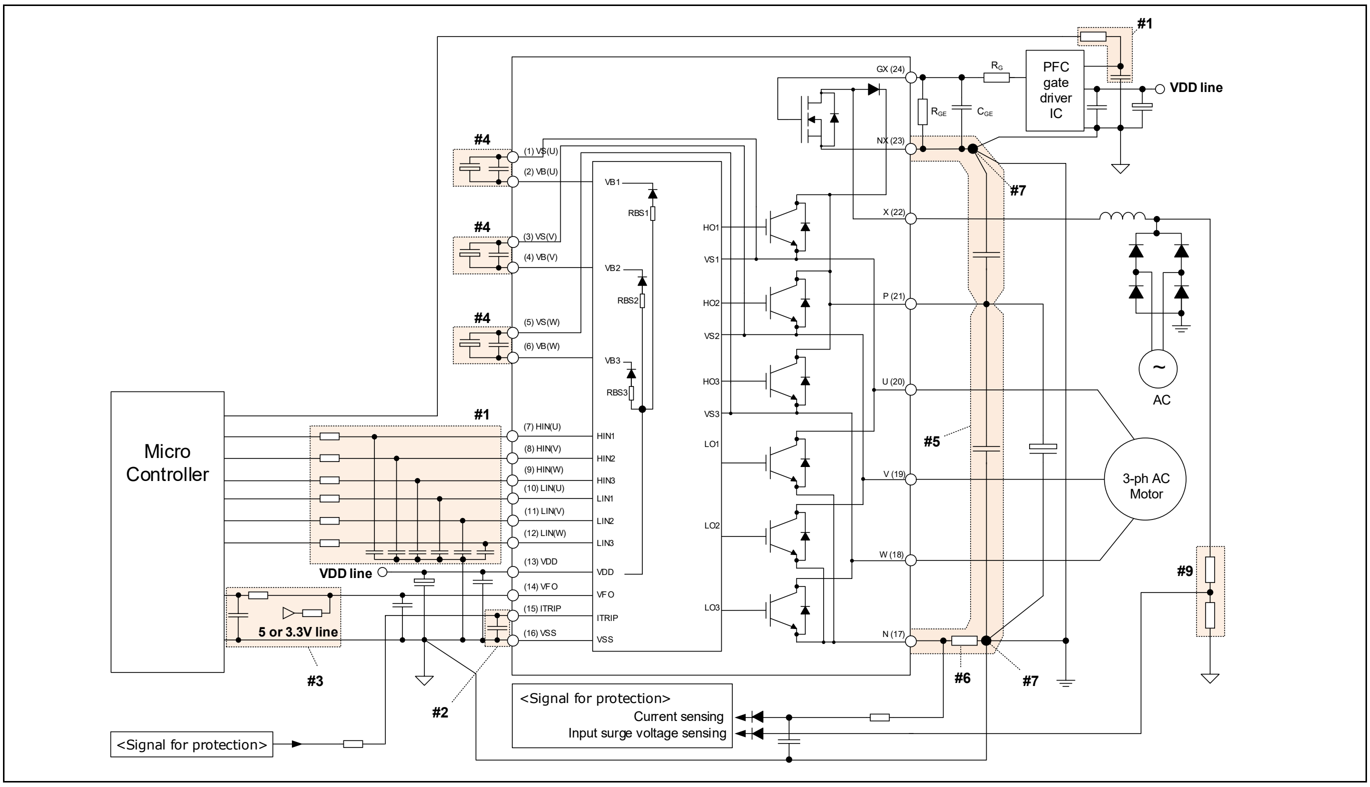


Figure 12 Typical application circuit

- #1 Input circuit
  - RC filter can be used to reduce input signal noise. (100 Ω, 1 nF)
  - The capacitors should be located close to the IPM (to V_{SS} terminal especially).
- #2 Itrip circuit
  - To prevent a mis operation of protection function, RC filter is recommended.
  - The capacitor should be located close to Itrip and VSS terminals.
- #3 VFO circuit
  - VFO pin is open drain configuration. This terminal should be pulled up to the bias voltage of the 5 V/3.3 V through a proper resistor.
  - It is recommended that RC filter is placed close to the controller.
- #4 VB-VS circuit
  - Capacitors for high-side floating supply voltage should be placed close to VB and VS terminals.
- #5 Snubber capacitor
  - The wiring among the IPM, snubber capacitor and shunt resistors should be short as possible.
- #6 Shunt resistor
  - SMD type shunt resistors are strongly recommended to minimize its internal stray inductance.
- #7 Ground pattern
  - Pattern overlap of power ground and signal ground should be minimized. The patterns should be connected at one end of shunt resistor only for the same potential.

12.2 Performance Chart

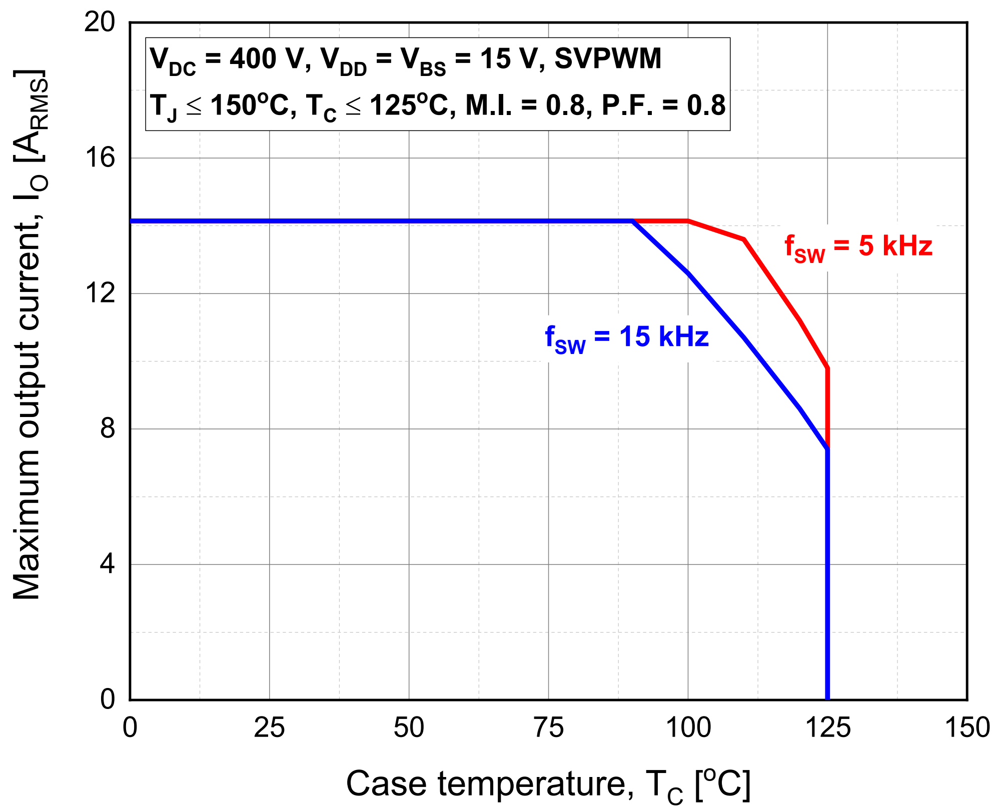


Figure 13 Maximum operating current SOA of inverter part[1]

[1]This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be changed by each user's actual operating conditions.

13 Package Outline

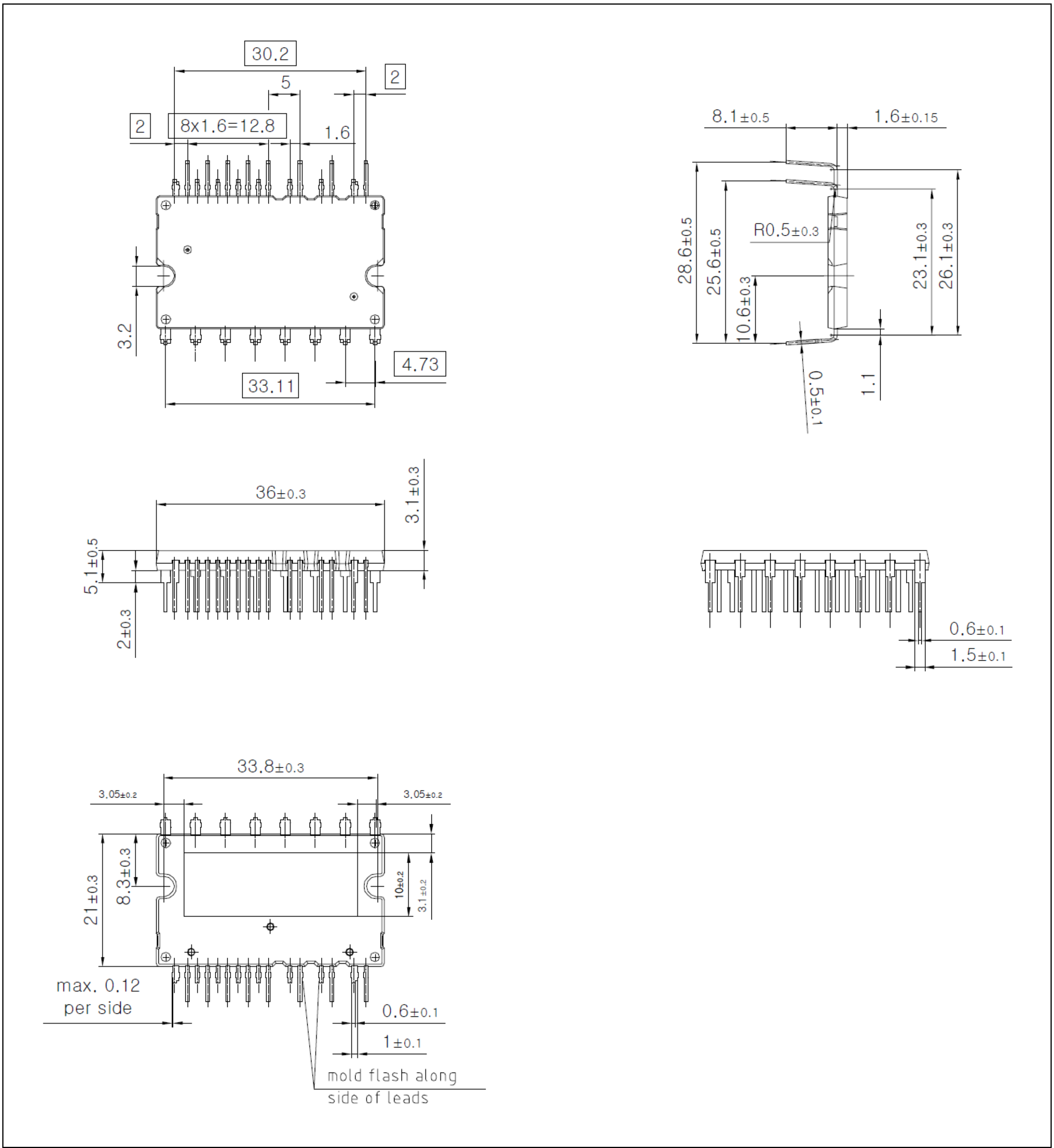


Figure 14 IM564-X6D

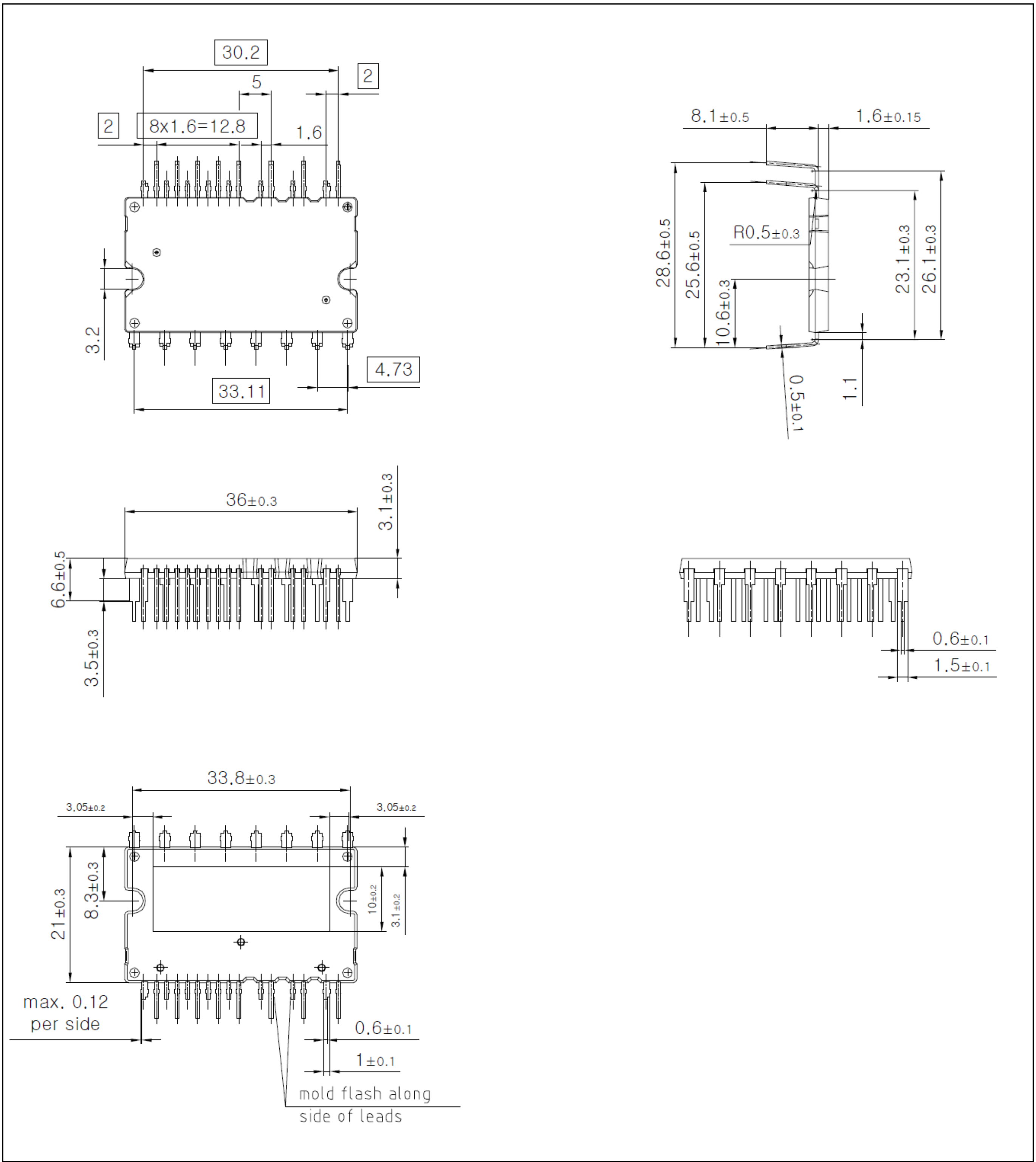


Figure 15 IM564-X6DS

Revision history

Document version	Date of release	Description of changes
Version 2.0	2019-08-09	Initial Release
Version 2.1	2019-11-05	Added remark in Table 1 Corrected error in Figure 9
Version 2.2	2020-04-24	Corrected error in Figure 13 Updated Figure 14 and Figure 15

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