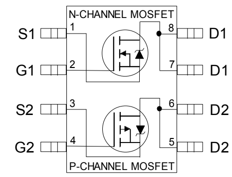
Features

- Advanced Planar Technology
- Low On-Resistance
- Logic Level Gate Drive
- Dual N and P Channel MOSFET
- Dynamic dv/dt Rating
- 150°C Operating Temperature
- Fast Switching
- Full Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



Top View

	N-CH	P-CH
V_{DSS}	30V	-30V
$R_{DS(on)}$ max.	0.10Ω	0.25Ω
I_D	3.5A	-2.3A

SO-8
AUIRF9952Q

G	D	S
Gate	Drain	Source

Description

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF952Q	SO-8	Tape and Reel	4000	AUIRF9952QTR

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.		Units
		N-Channel	P-Channel	
I_D @ T_A = 25°C	10 Sec. Pulsed Drain Current, V_{GS} @ 10V	3.5	-2.3	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	2.8	-1.8	
I_{DM}	Pulsed Drain Current ①	16	-10	
P_D @T_A = 25°C	Maximum Power Dissipation	2.0		W
P_D @T_A = 70°C	Maximum Power Dissipation	1.3		
	Linear Derating Factor	0.016		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ③	44	57	mJ
I_{AR}	Avalanche Current ①	2.0	-1.3	A
E_{AR}	Repetitive Avalanche Energy ①	0.25		mJ
dv/dt	Peak Diode Recovery dv/dt ②	5.0	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑤	——	62.5	°C/W

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*Qualification standards can be found at www.infineon.com

Static @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	30	——	——	V	V_{GS} = 0V, I_D = 250μA
		P-Ch	-30	——	——		V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	——	0.015	——	V/°C	Reference to 25°C, I_D = 1mA
		P-Ch	——	-0.015	——		Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	N-Ch	——	0.08	0.10	Ω	V_{GS} = 10V, I_D = 2.2A ④
			——	0.12	0.15		V_{GS} = 4.5V, I_D = 1.0A ④
		P-Ch	——	0.165	0.250		V_{GS} = -10V, I_D = -1.0A ④
			——	0.290	0.400		V_{GS} = -4.5V, I_D = -0.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	——	3.0	V	V_{DS} = V_{GS}, I_D = 250μA
		P-Ch	-1.0	——	-3.0		V_{DS} = V_{GS}, I_D = -250μA
gfs	Forward Trans conductance	N-Ch	——	12	——	S	V_{DS} = 15V, I_D = 3.5A
		P-Ch	——	2.4	——		V_{DS} = -15V, I_D = -2.3A
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	——	——	2.0	μA	V_{DS} =24V, V_{GS} = 0V
		P-Ch	——	——	-2.0		V_{DS} = -24V,V_{GS} = 0V
		N-Ch	——	——	25		V_{DS} =24V, V_{GS} = 0V ,T_J = 125°C
		P-Ch	——	——	-25		V_{DS} = -24V,V_{GS} = 0V,T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	N-P	——	——	± 100	nA	V_{GS} = ± 20V
	Gate-to-Source Reverse Leakage	N-P	——	——	± 100		V_{GS} = ± 20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q_g	Total Gate Charge	N-Ch	——	6.9	14	nC	N-Channel I_D = 1.8A, V_{DS} = 10V,V_{GS} = 10V ④ P-Channel I_D = -2.3A,V_{DS} = -10V,V_{GS} = -10V
		P-Ch	——	6.1	12		
Q_{gs}	Gate-to-Source Charge	N-Ch	——	1.0	2.0		
		P-Ch	——	1.7	3.4		
Q_{gd}	Gate-to-Drain Charge	N-Ch	——	1.8	3.5		
		P-Ch	——	1.1	2.2		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	——	6.2	12	ns	N-Channel V_{DD} = 10V,I_D = 1.0A,R_G = 6.0Ω, R_D = 10Ω ④ P-Channel V_{DD} = -10V,I_D = -1.0A,R_G = 6.0Ω, R_D = 10Ω
		P-Ch	——	9.7	19		
t_r	Rise Time	N-Ch	——	8.8	18		
		P-Ch	——	14	28		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	——	13	26		
		P-Ch	——	20	40		
t_f	Fall Time	N-Ch	——	3.0	6.0		
		P-Ch	——	6.9	14		
C_{iss}	Input Capacitance	N-Ch	——	190	——	pF	N-Channel V_{GS} = 0V,V_{DS} = 15V,f = 1.0MHz P-Channel V_{GS} = 0V,V_{DS} = -15V,f = 1.0MHz
		P-Ch	——	190	——		
C_{oss}	Output Capacitance	N-Ch	——	120	——		
		P-Ch	——	110	——		
C_{rss}	Reverse Transfer Capacitance	N-Ch	——	61	——		
		P-Ch	——	54	——		

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	——	——	1.7	A	
		P-Ch	——	——	-1.3		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	——	——	16		
		P-Ch	——	——	-16		
V_{SD}	Diode Forward Voltage	N-Ch	——	0.82	1.2	V	T_J = 25°C,I_S = 1.25A,V_{GS} = 0V ④
		P-Ch	——	-0.82	-1.2		T_J = 25°C,I_S = -1.25A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	N-Ch	——	27	53	ns	N-Channel T_J = 25°C ,I_F = 1.25A, di/dt = 100A/μs P-Channel ④ T_J = 25°C,I_F = -1.25A, di/dt = 100A/μs
		P-Ch	——	27	54		
Q_{rr}	Reverse Recovery Charge	N-Ch	——	28	57	nC	
		P-Ch	——	31	62		
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)					

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig.23)
② N-Channel $I_{SD} \leq$ 2.0A, di/dt ≤ 100A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C.
P-Channel $I_{SD} \leq$ -1.3A, di/dt ≤ 84A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C.
③ N-Channel Starting T_J = 25°C, L = 22mH R_G = 25Ω, I_{AS} = 2.0A.(See Figure 12)
P-Channel Starting T_J = 25°C, L = 67mH R_G = 25Ω, I_{AS} = -1.3A.
④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
⑤ Surface mounted on FR-4 board , t ≤ 10sec.

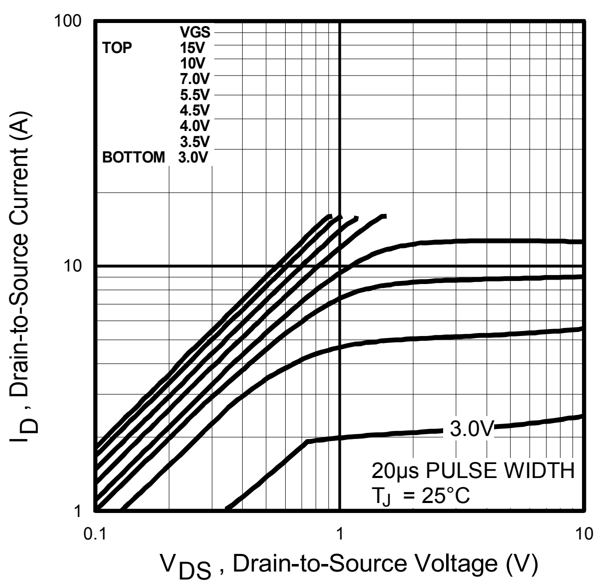


Fig. 1 Typical Output Characteristics

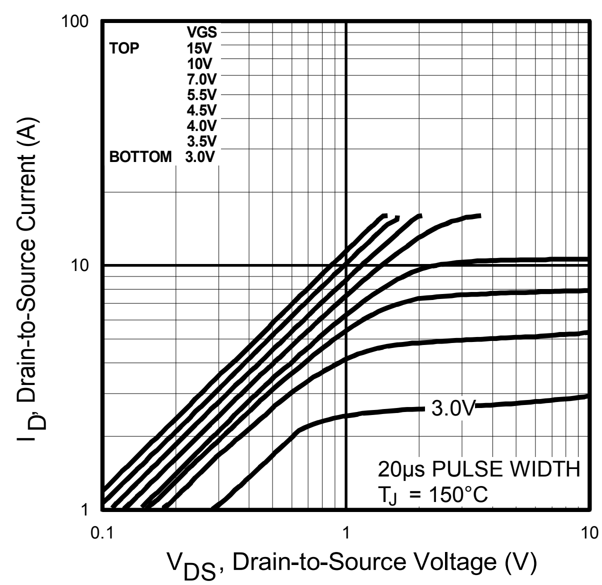


Fig. 2 Typical Output Characteristics

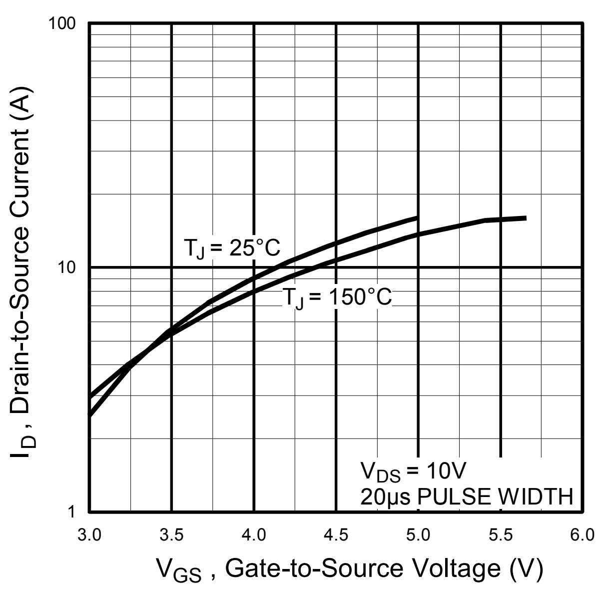


Fig. 3 Typical Transfer Characteristics

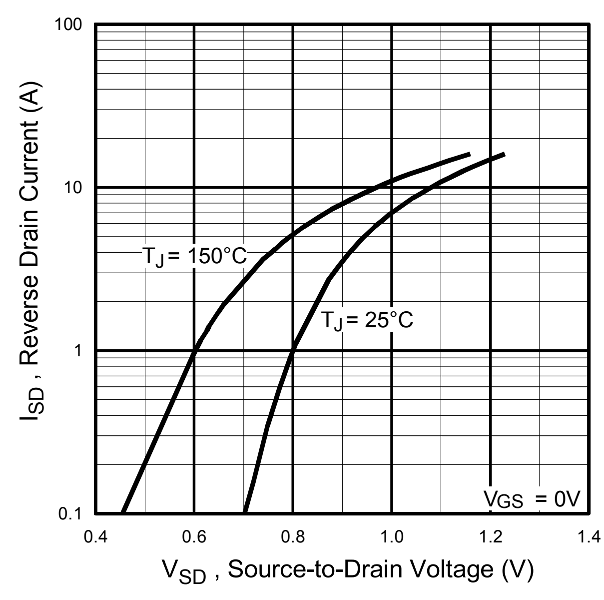


Fig. 4 Typical Source-Drain Diode Forward Voltage

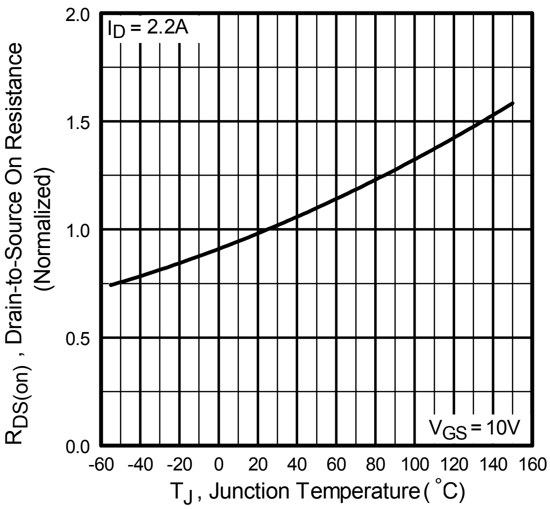


Fig 5. Normalized On-Resistance Vs. Temperature

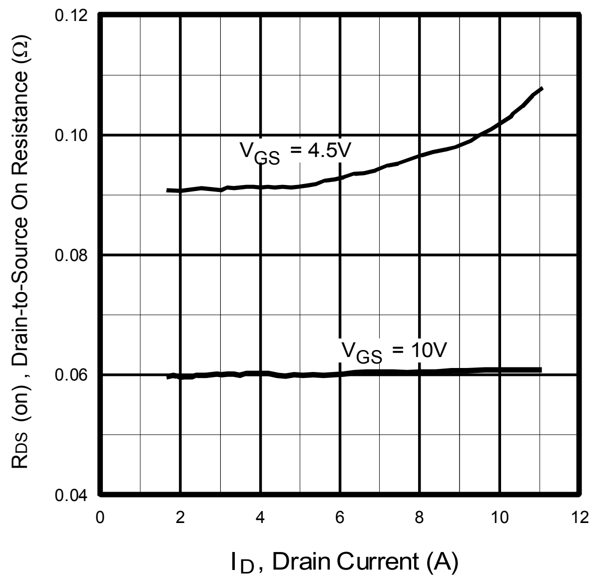


Fig 6. Typical On-Resistance Vs. Drain Current

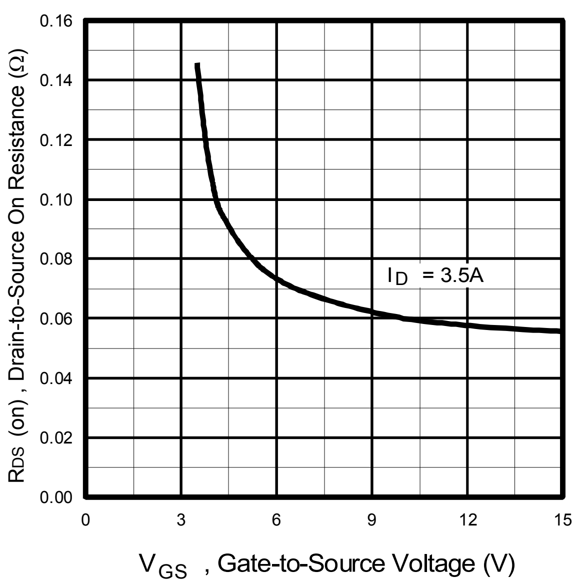


Fig. 7 Typical On-Resistance Vs. Gate Voltage

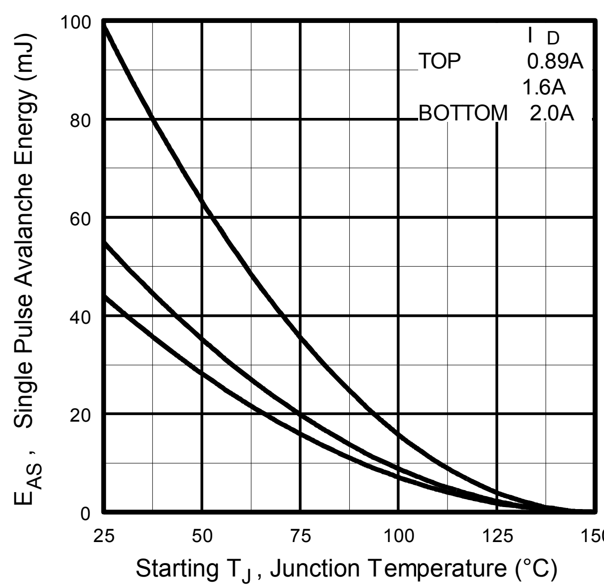


Fig 8. Maximum Avalanche Energy Vs. Drain Current

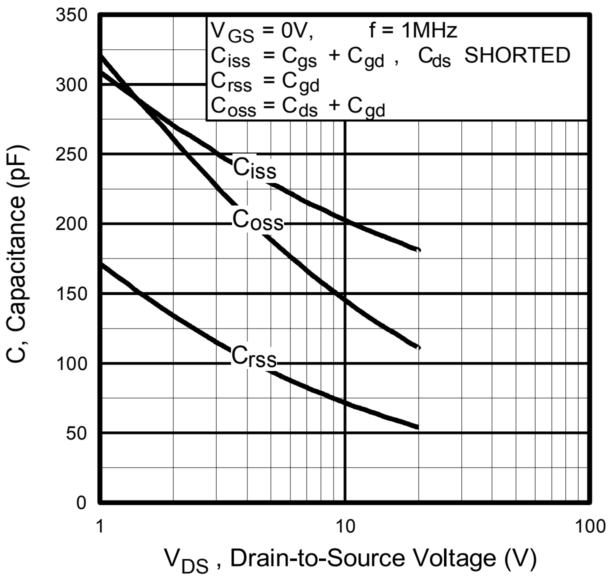


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

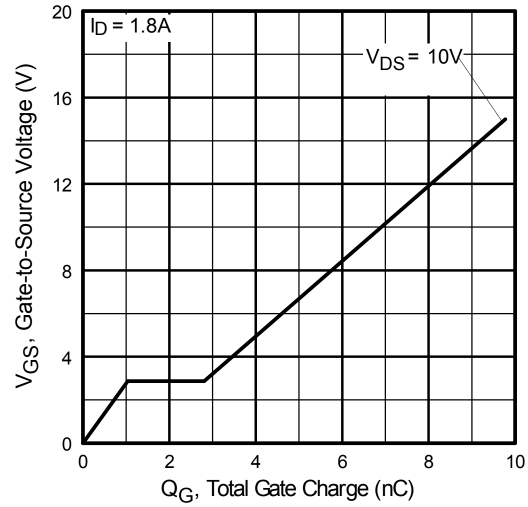


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

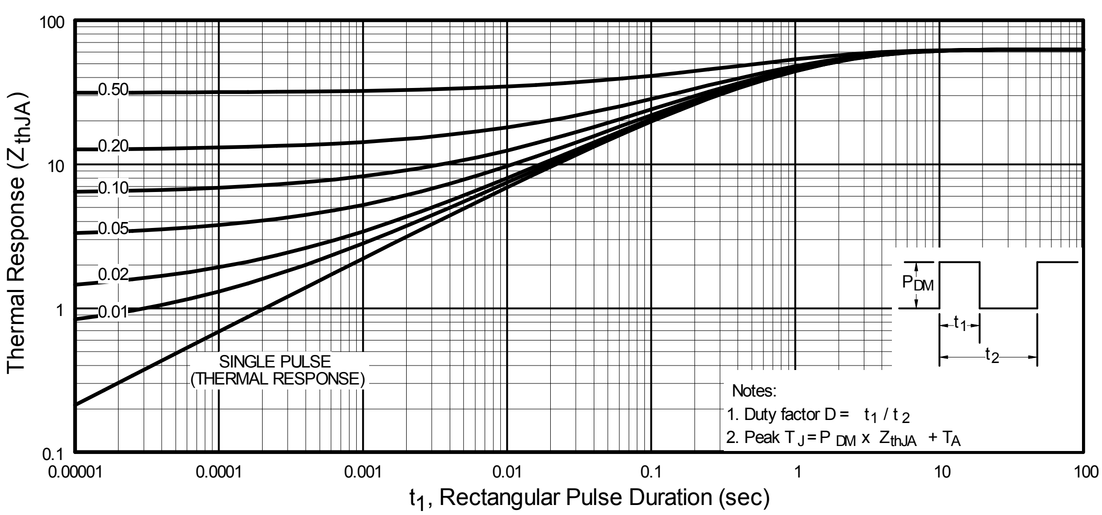


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

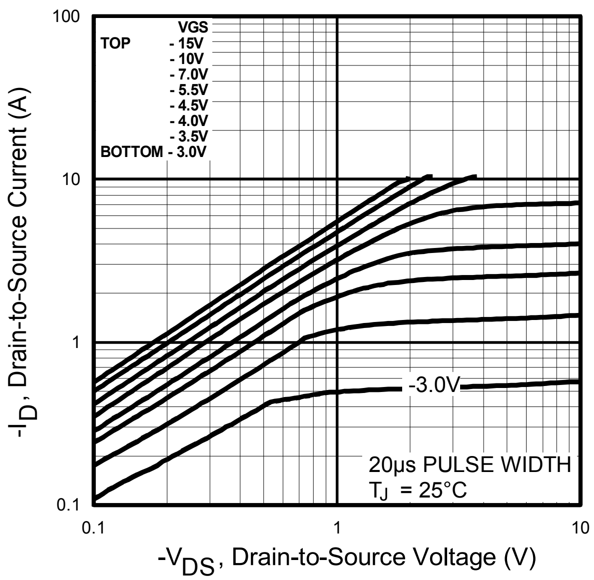


Fig. 12 Typical Output Characteristics

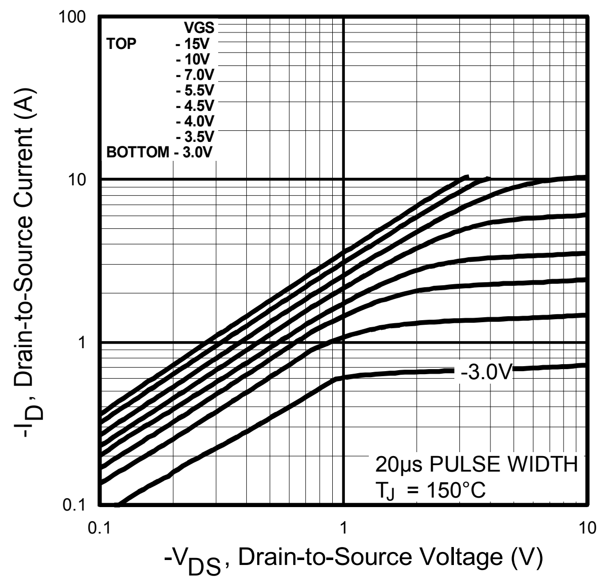


Fig. 13 Typical Output Characteristics

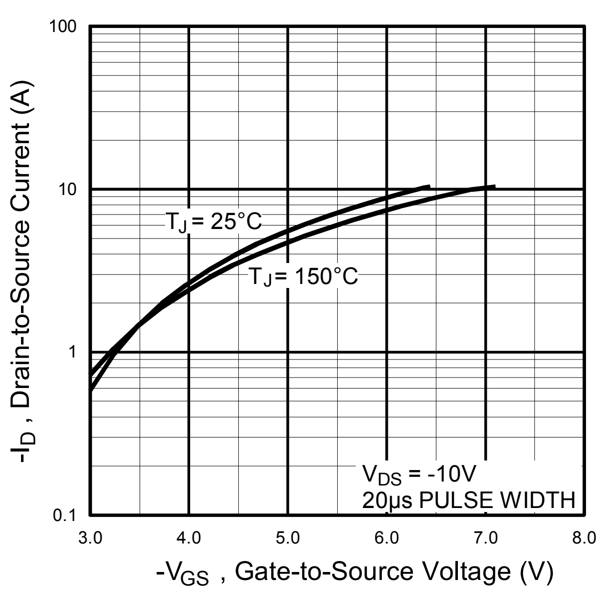


Fig. 14 Typical Transfer Characteristics

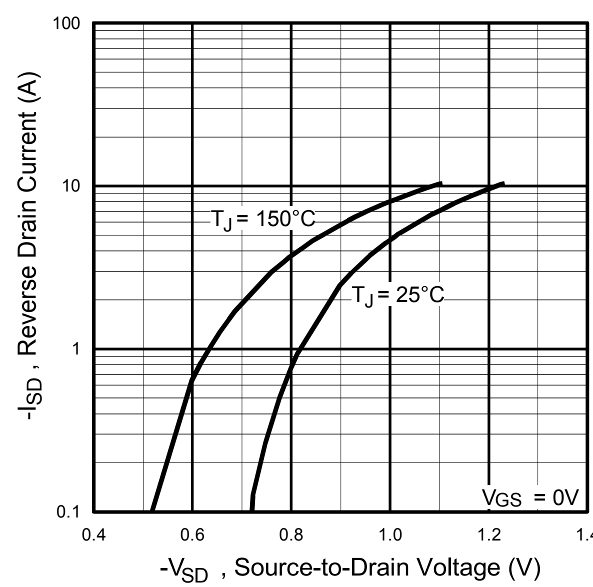


Fig. 15 Typical Source-Drain Diode Forward Voltage

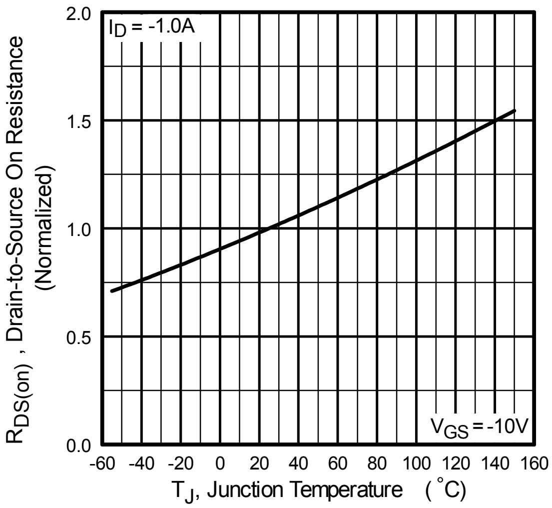


Fig 16. Normalized On-Resistance Vs. Temperature

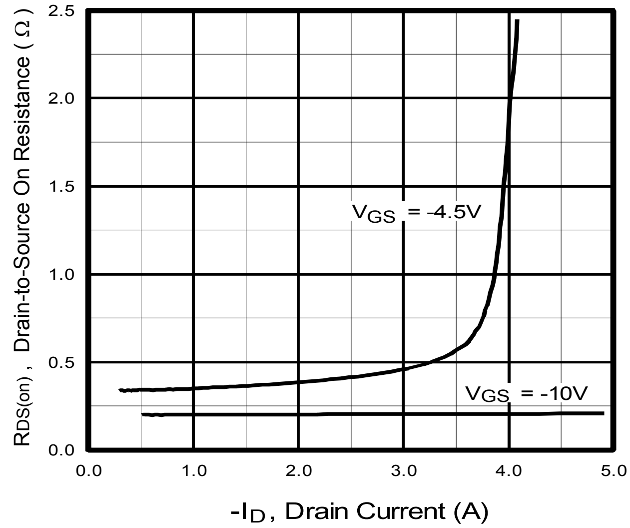


Fig 17. Typical On-Resistance Vs. Drain Current

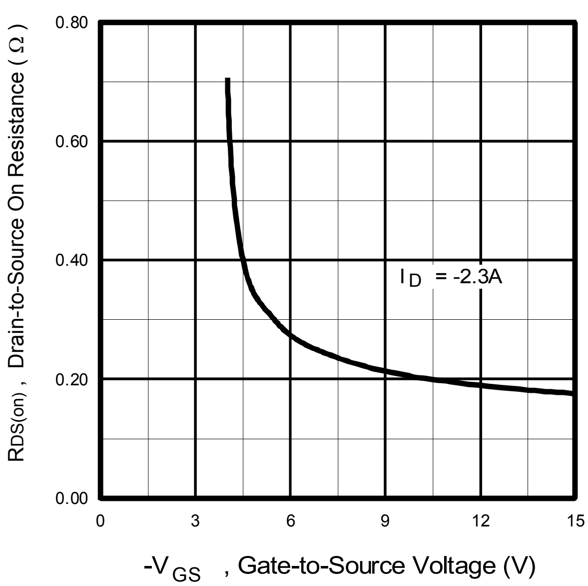


Fig. 18 Typical On-Resistance Vs. Gate Voltage

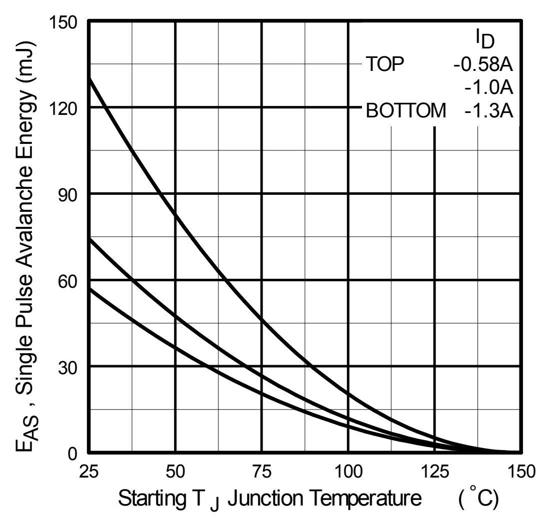


Fig 19. Maximum Avalanche Energy Vs. Drain Current

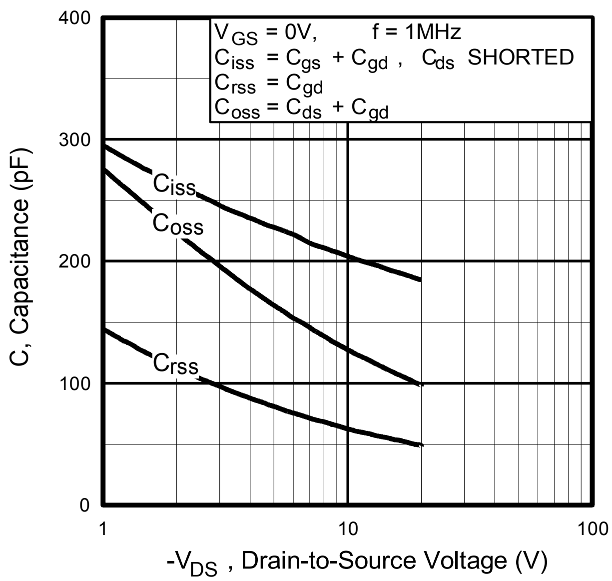


Fig 20. Typical Capacitance Vs. Drain-to-Source Voltage

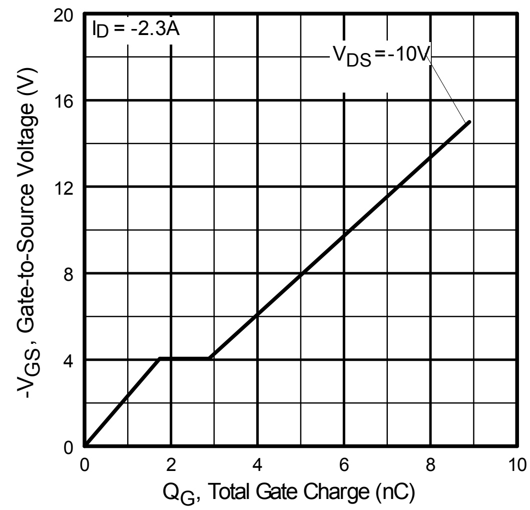


Fig 21. Typical Gate Charge Vs. Gate-to-Source Voltage

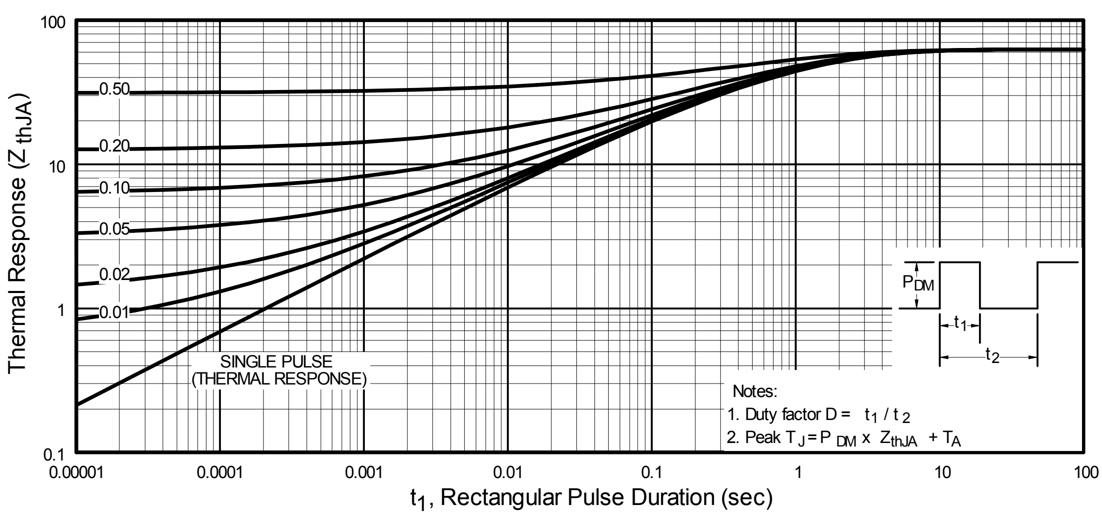
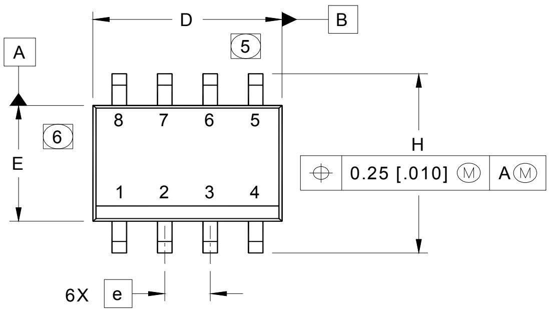
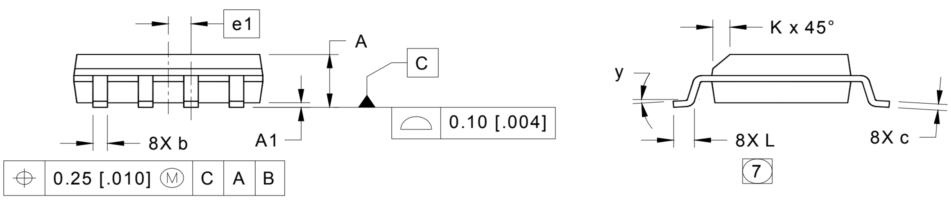


Fig 22. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

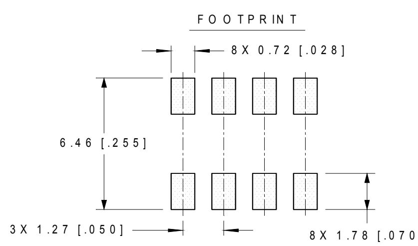
SO-8 Package Outline (Dimensions are shown in millimeters (inches))



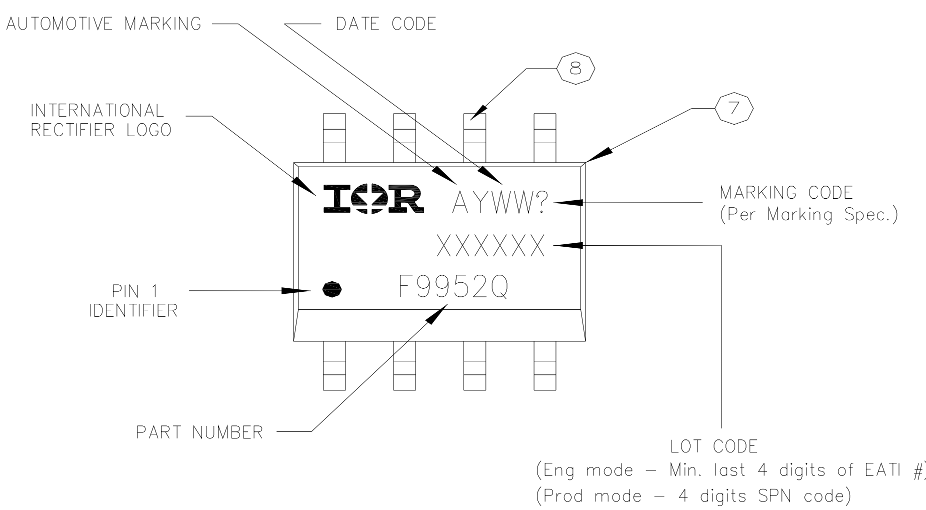
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

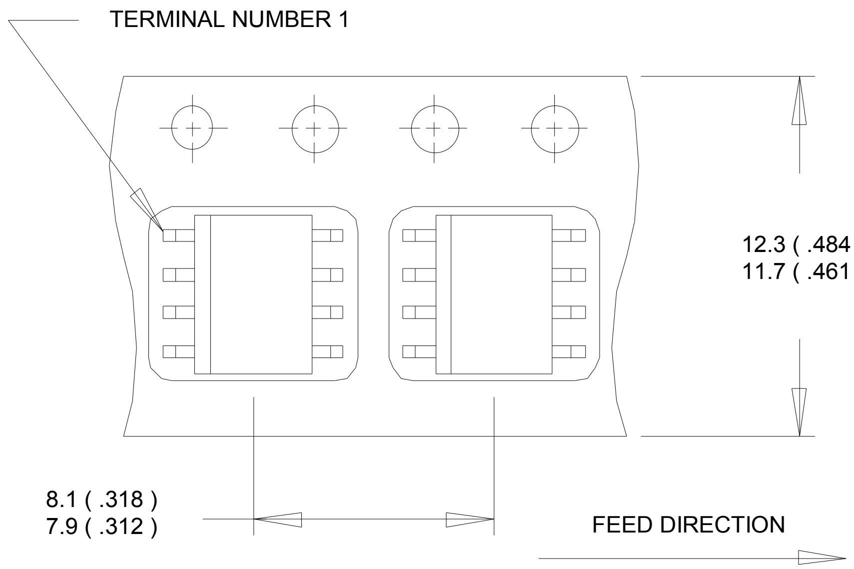


SO-8 Part Marking Information

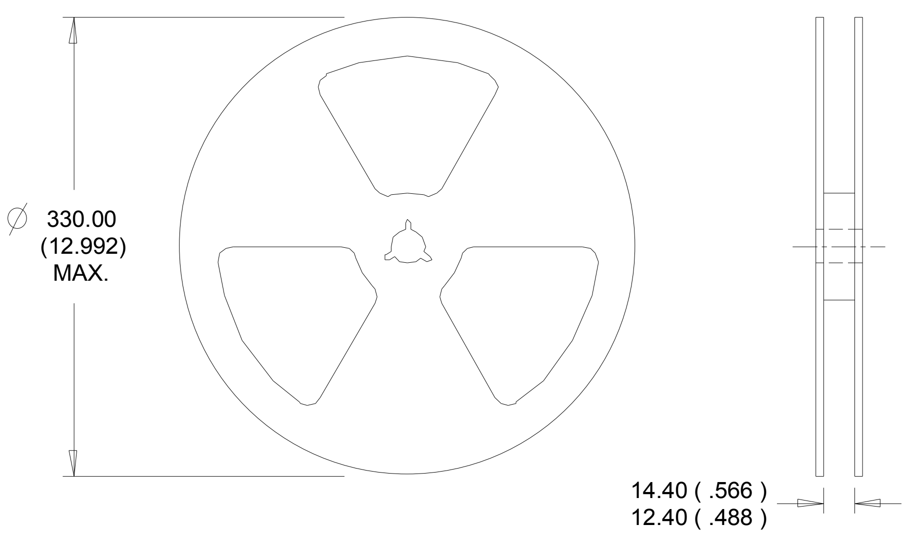


Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

SO-8 Tape and Reel (Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SO-8	MSL1
ESD	Machine Model	N Ch: Class M1A (+/- 50V)† P Ch: Class M1A (+/- 50V)† AEC-Q101-002	
	Human Body Model	N Ch: Class H0 (+/- 150V)† P Ch: Class H0 (+/- 150V)† AEC-Q101-001	
	Charged Device Model	N Ch: Class C4 (+/- 1000V)† P Ch: Class C4 (+/- 1000V)† AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
3/5/2014	• Added "Logic Level Gate Drive" bullet in the features section on page 1 • Updated data sheet with new IR corporate template
10/5/2015	• Updated datasheet with corporate template • Corrected ordering table on page 1.

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