

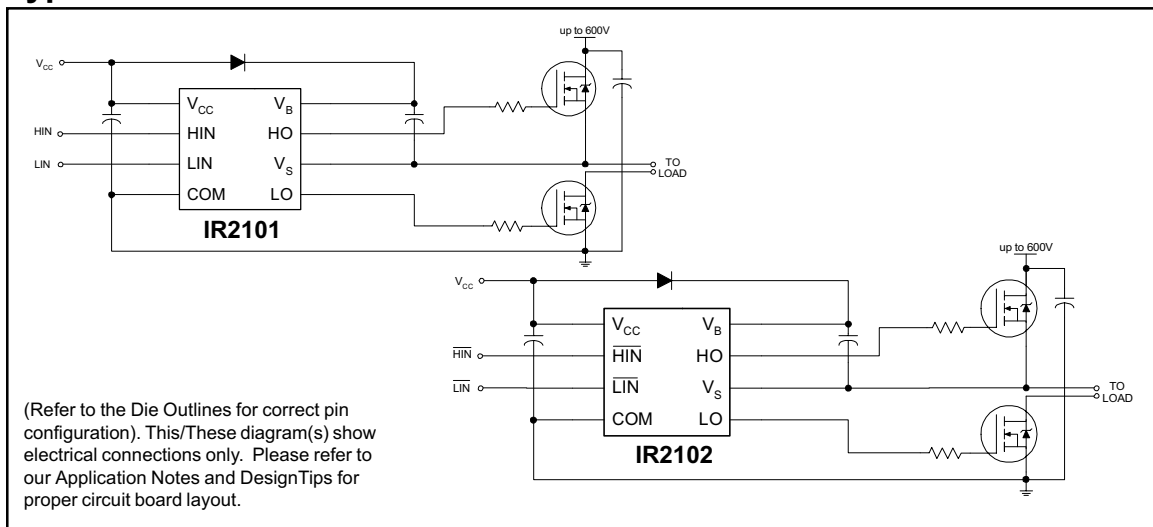
IR2101C/IR2102C

HIGH AND LOW SIDE DRIVER DIE IN WAFER FORM

Features

- 100 % Tested at Probe^①
- Available in Chip Pack, Unsawn Wafer, Sawn on Film^②
- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V, and 15V logic input compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs (IR2101) or out of phase with inputs (IR2102)

Typical Connection



Note:

① This IR product is 100% tested at wafer level and is manufactured using established, mature and well characterized processes. Due to restrictions in die level processing, die may not be equivalent to standard package products and are therefore offered with a conditional performance guarantee. The above data sheet is based on IR sample testing under certain predetermined and assumed conditions, and are provided for illustration purposes only. Customers are encouraged to perform testing in actual proposed packaged and use conditions. IR die products are tested using IR-based quality assurance procedures and are manufactured using IR's established processes. Programs for customer-specified testing are available upon request. IR has experienced assembly yields of generally 95% or greater for individual die; however, customer's results will vary. Estimates such as those described and set forth in this data sheet for semiconductor die will vary depending on a number of packaging, handling, use and other factors. Sold die may not perform on an equivalent basis to standard package products and are therefore offered with a limited warranty as described in IR's applicable standard terms and conditions of sale. All IR die sales are subject to IR's applicable standard terms and conditions of sale, which are available upon request. For customers requiring a particular parameter to be guaranteed, special testing can be carried out or product can be purchased as known good die.

② Part number shown is for die in wafer. Contact factory for these other options.

IR2101C/IR2102C

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Description

The IR2101C/IR2102C are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	-0.3	625	V
V_S	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage (HIN & LIN)	-0.3	$V_{CC} + 0.3$	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN) (IR2101) & ($\overline{HIN}$ & $\overline{LIN}$) (IR2102)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Static Electrical Characteristics

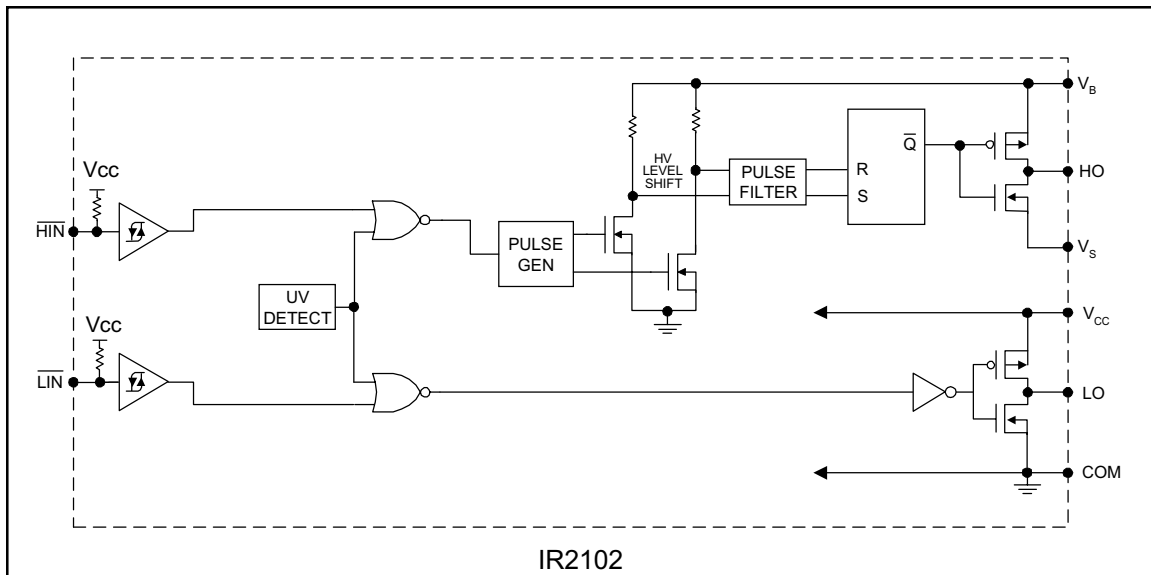
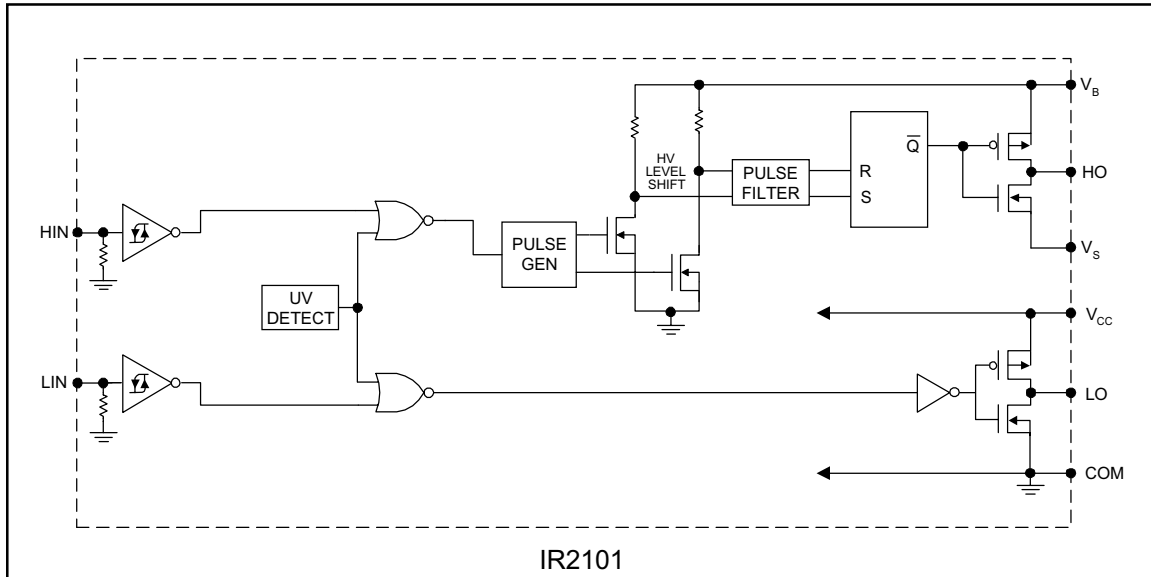
V_{BIAS} (V_{CC} , V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage (IR2101) Logic "0" input voltage (IR2102)	3	—	—	V	$V_{CC} = 10V$ to 20V
V_{IL}	Logic "0" input voltage (IR2101) Logic "1" input voltage (IR2102)	—	—	0.8		$V_{CC} = 10V$ to 20V
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
V_{OL}	Low level output voltage, V_O	—	—	100		$I_O = 0A$
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		$V_{IN} = 0V$ or 5V
I_{IN+}	Logic "1" input bias current	—	3	10		$V_{IN} = 5V$ (IR2101) $V_{IN} = 0V$ (IR2102)
I_{IN-}	Logic "0" input bias current	—	—	1		$V_{IN} = 0V$ (IR2101) $V_{IN} = 5V$ (IR2102)
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8	8.9	9.8	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.4	8.2	9		
I_{O+}	Output high short circuit pulsed current	130	210	—	mA	$V_O = 0V$ $V_{IN} = \text{Logic "1"}$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	270	360	—		$V_O = 15V$ $V_{IN} = \text{Logic "0"}$ $PW \leq 10 \mu s$

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Functional Block Diagram



Bonding Pad Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (IR2101)
$\overline{\text{HIN}}$	Logic input for high side gate driver output (HO), out of phase (IR2102)
LIN	Logic input for low side gate driver output (LO), in phase (IR2101)
$\overline{\text{LIN}}$	Logic input for low side gate driver output (LO), out of phase (IR2102)
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

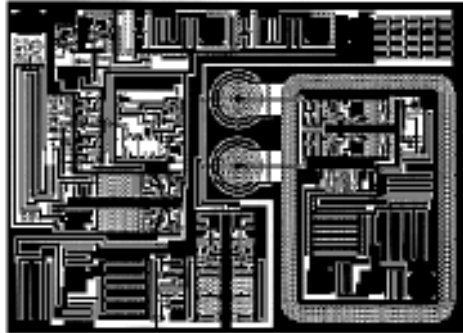
Mechanical Data

Nominal Front Metal Composition, Thickness	Al-Si (Si: 1.0% $\pm$ 0.1%), 2 μ m
Wafer Diameter	125mm with std. <100> flat
Wafer Thickness	625 $\pm$ 25 μ m
Minimum Street Width	0.006"
Reject Ink Dot Size	0.02" – 0.03"
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination.

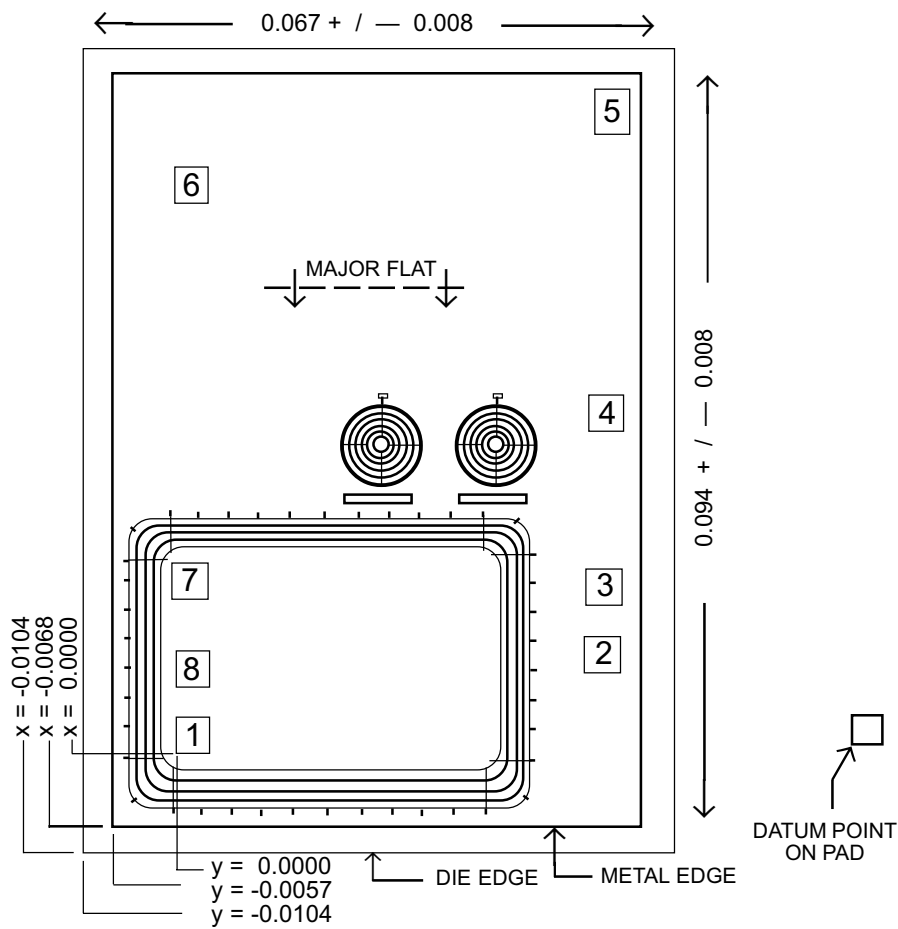
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Device Information IR2101C & IR2102C

Process & Design Rule			HVDCMOS 600V	
Transistor Count			168	
Die Size			94 x 67 mils	
Die Outline				
Thickness of Gate Oxide			800Å	
Connections	First Layer	Material	Poly Silicon	
		Width	4.0 µm	
		Spacing	6.0 µm	
		Thickness	5000Å	
	Second Layer	Material	Al - Si (Si: 1.0% ±0.1%)	
		Width	6 µm	
		Spacing	9 µm	
		Thickness	20,000Å	
Contact Hole Dimension			5.0 µm X 5.0 µm	
Insulation Layer	Material	PSG (SiO ₂)		
	Thickness	1.6 µm		
Passivation	Material	PSG (SiO ₂)		
	Thickness	1.6 µm		
Method of Saw			Full Cut	
Method of Die Bond			Ablebond 84 - 1	
Wire Bond	Method	Thermosonic		
	Material	Au (1.3 mil)		
Leadframe	Material	Cu		
	Die Area	Ag		
	Lead Plating	70-90% Sn (Balance Pb)		
Package	Types	8-Lead PDIP / 8-Lead SOIC		
	Materials	EME6300H EME6600RA		
Remarks:				

Die Outline: IR2101C/IR2102C
(in inches)



Pad #	Function	Datum		PAD SIZE
		X	Y	
1	VB	0.0000	0.0000	0.0039 X 0.0039
2	VCC	0.0474	0.0112	0.0039 X 0.0039
3	HIN	0.0476	-0.0193	0.0039 X 0.0039
4	LIN	0.0476	0.0388	0.0039 X 0.0039
5	PGND	0.0485	0.0728	0.0039 X 0.0039
6	LO	-0.0008	0.0644	0.0039 X 0.0039
7	VS	-0.0008	0.0191	0.0039 X 0.0039
8	HO	0.0008	0.0093	0.0039 X 0.0039
X and Y Tolerances ± 0.0002				

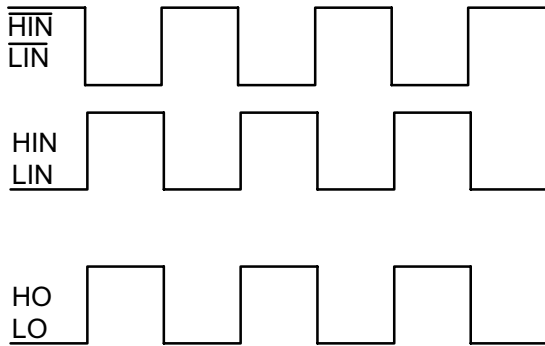


Figure 1. Input/Output Timing Diagram

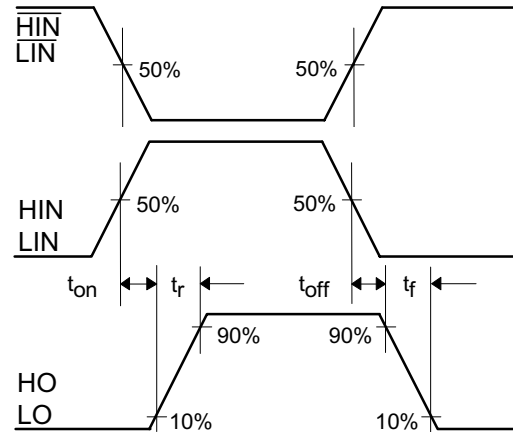


Figure 2. Switching Time Waveform Definitions

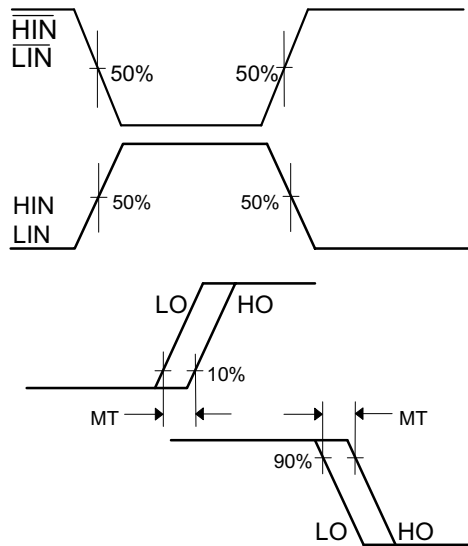


Figure 3. Delay Matching Waveform Definitions

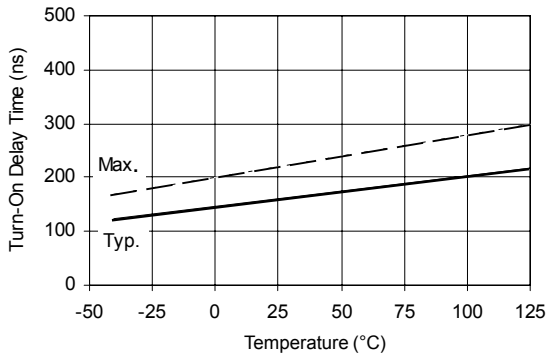


Figure 6A. Turn-On Time vs Temperature

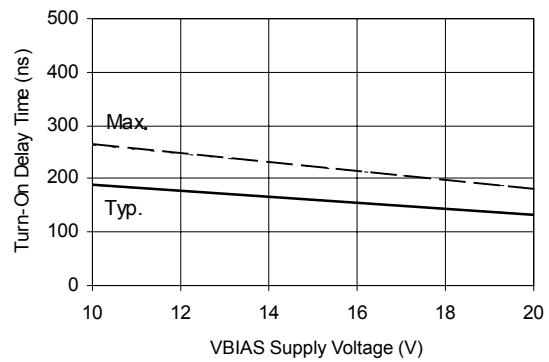


Figure 6B. Turn-On Time vs Supply Voltage

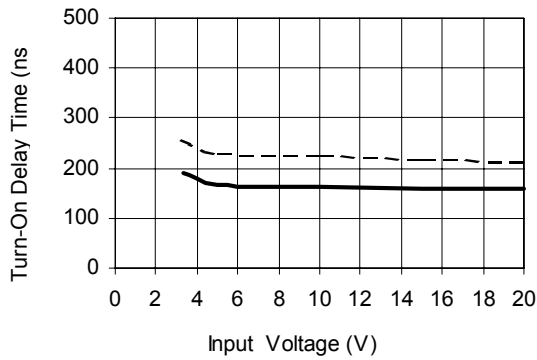


Figure 6C. Turn-On Time vs Input Voltage

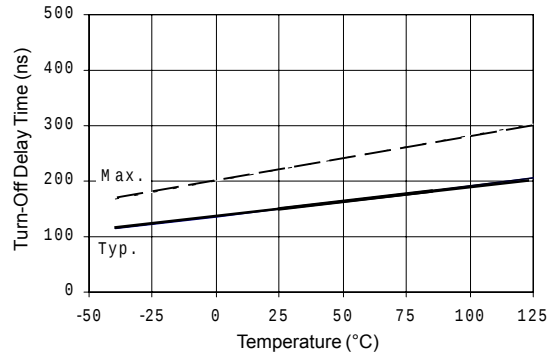


Figure 7A. Turn-Off Time vs Temperature

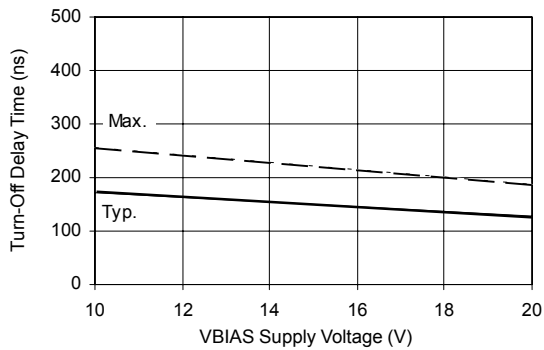


Figure 7B. Turn-Off Time vs Supply Voltage

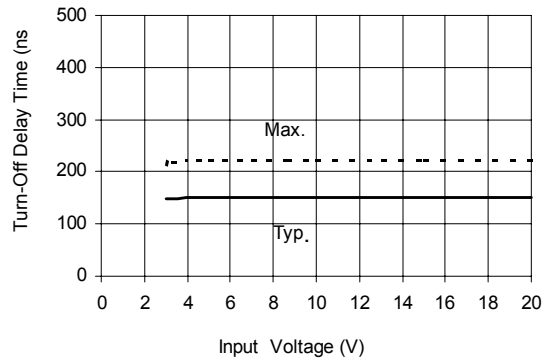


Figure 7C. Turn-Off Time vs Input Voltage

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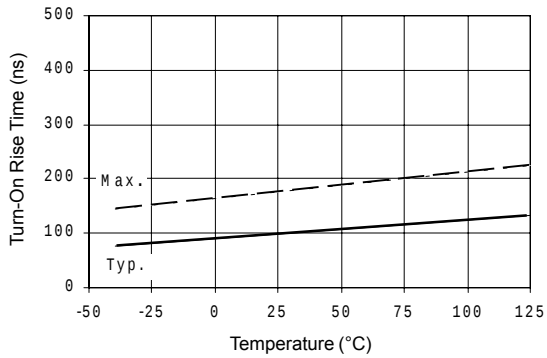


Figure 9A. Turn-On Rise Time vs Temperature

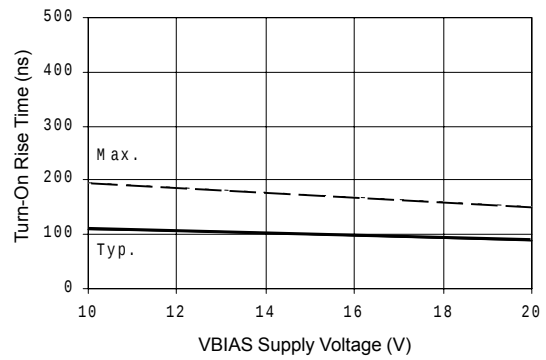


Figure 9B. Turn-On Rise Time vs Voltage

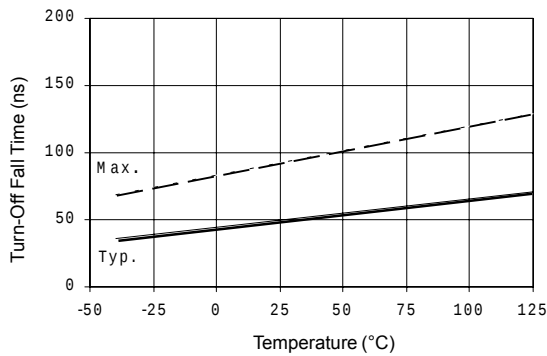


Figure 10A. Turn-Off Fall Time vs Temperature

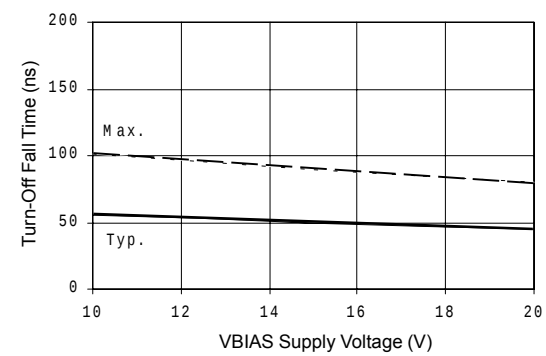
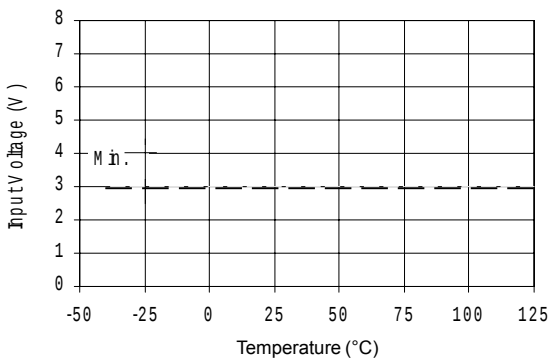
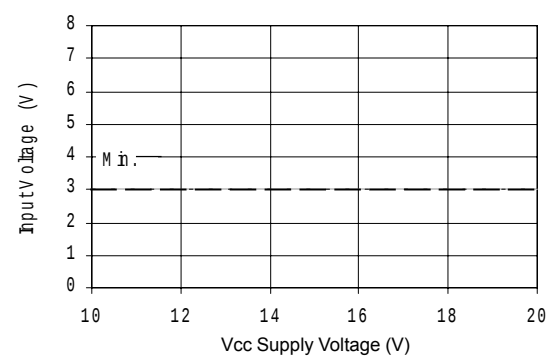


Figure 10B. Turn-Off Fall Time vs Voltage

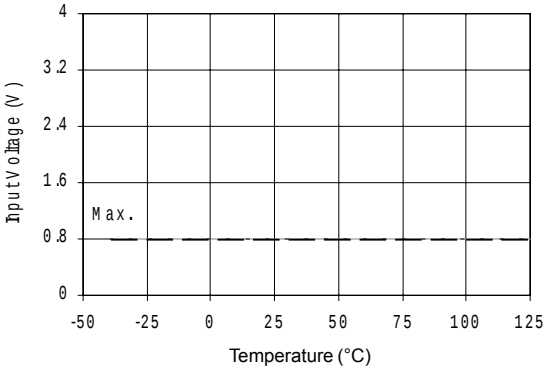


**Figure 12A. Logic "1" Input Voltage (IR2101)
Logic "0" Input Voltage (IR2102)
vs Temperature**

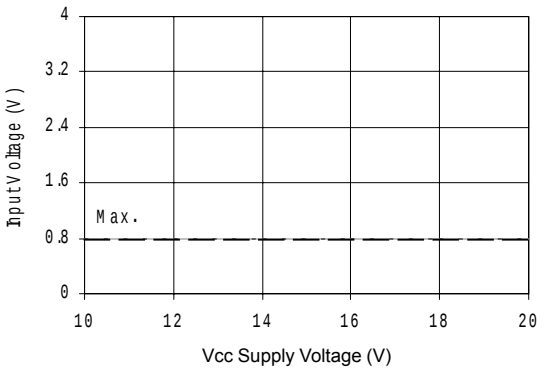


**Figure 12B. Logic "1" Input Voltage (IR2101)
Logic "0" Input Voltage (IR2102)
vs Voltage**

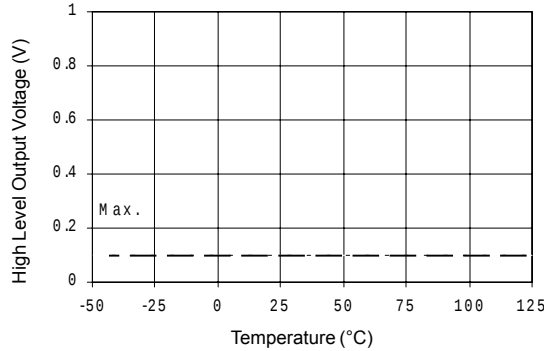
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**Figure 13A. Logic "0" Input Voltage (IR2101)
Logic "1" Input Voltage (IR2102)
vs Temperature**



**Figure 13B. Logic "0" Input Voltage (IR2101)
Logic "1" Input Voltage (IR2102)
vs Voltage**



**Figure 14A. High Level Output
vs Temperature**

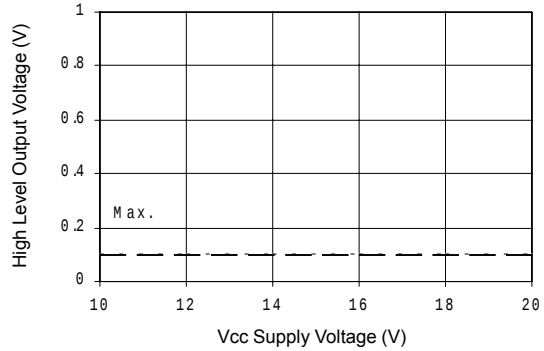
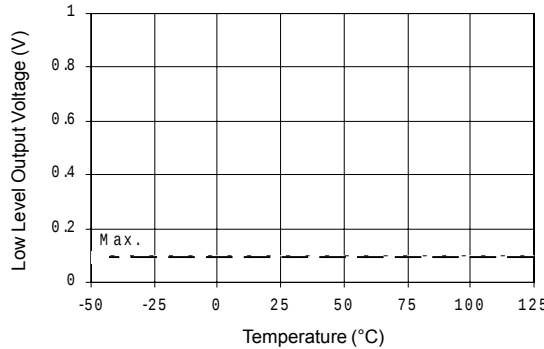


Figure 14B. High Level Output vs Voltage



**Figure 15A. Low Level Output
vs Temperature**

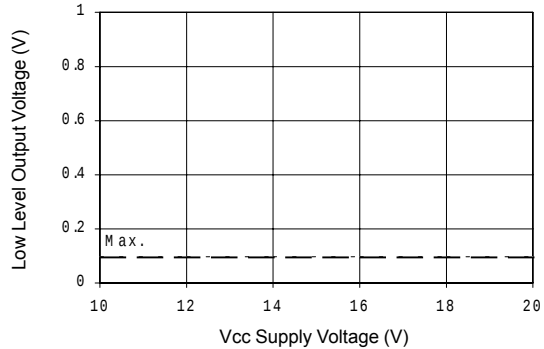


Figure 15B. Low level Output vs Voltage

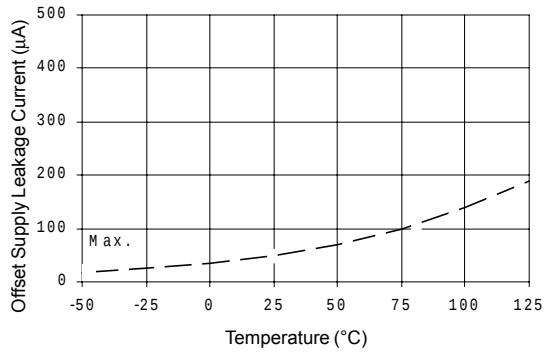


Figure 16A. Offset Supply Current vs Temperature

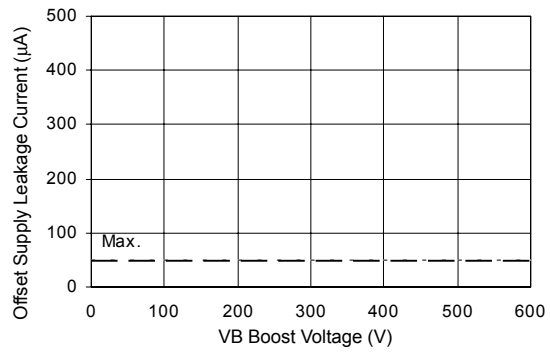


Figure 16B. Offset Supply Current vs Voltage

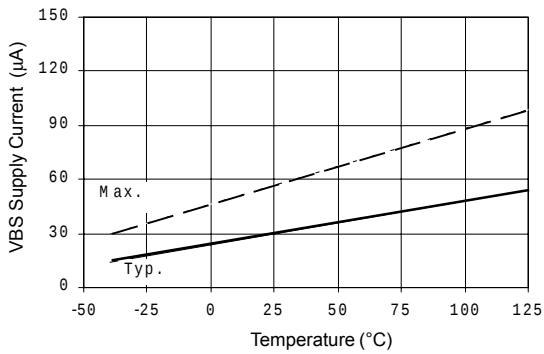


Figure 17A. V_{BS} Supply Current vs Temperature

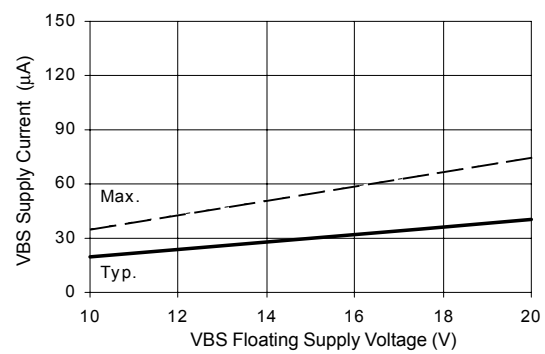


Figure 17B. V_{BS} Supply Current vs Voltage

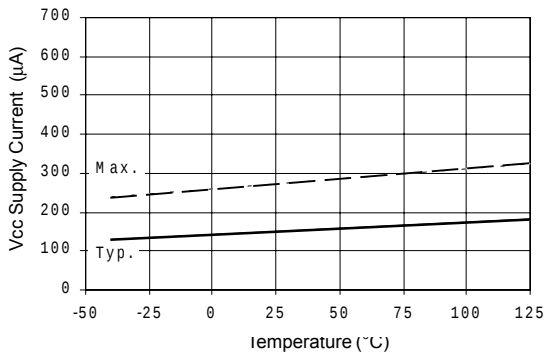


Figure 18A. V_{CC} Supply Current vs Temperature

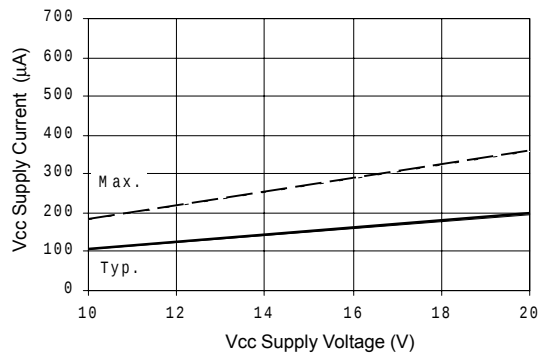


Figure 18B. V_{CC} Supply Current vs Voltage

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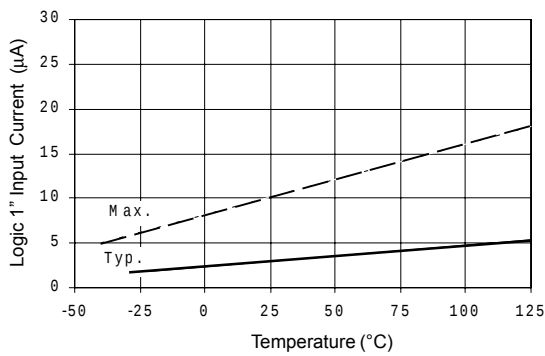


Figure 19A. Logic "1" Input Current vs Temperature

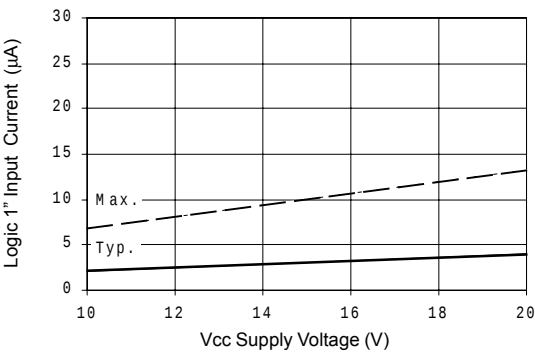


Figure 19B. Logic "1" Input Current vs Voltage

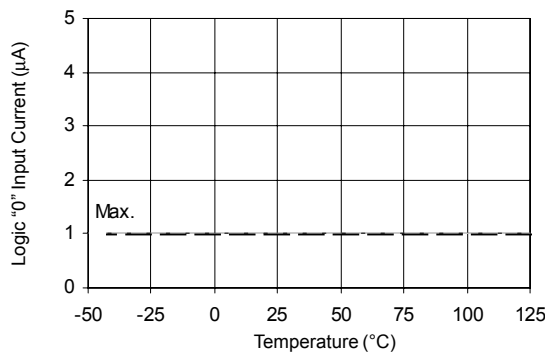


Figure 20A. Logic "0" Input Current vs Temperature

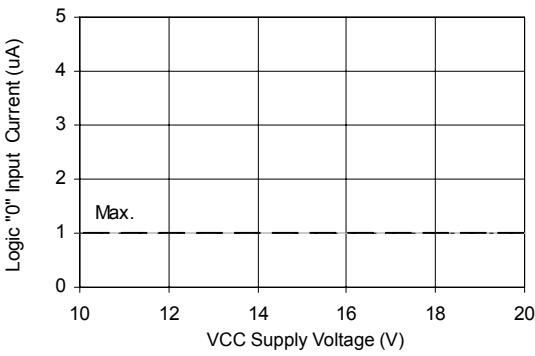


Figure 20B. Logic "0" Input Current vs Voltage

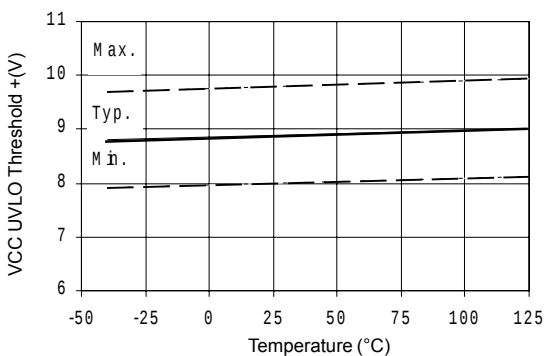


Figure 21A. Vcc Undervoltage Threshold(+) vs Temperature

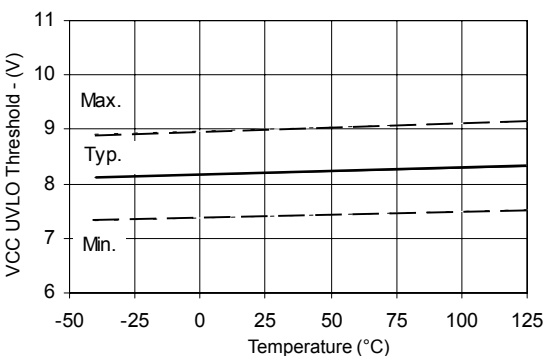


Figure 21B. Vcc Undervoltage Threshold(-) vs Temperature

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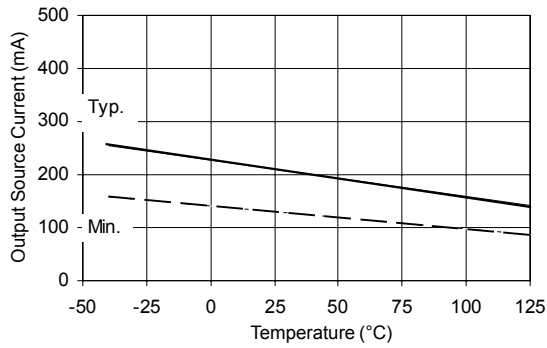


Figure 22A. Output Source Current vs Temperature

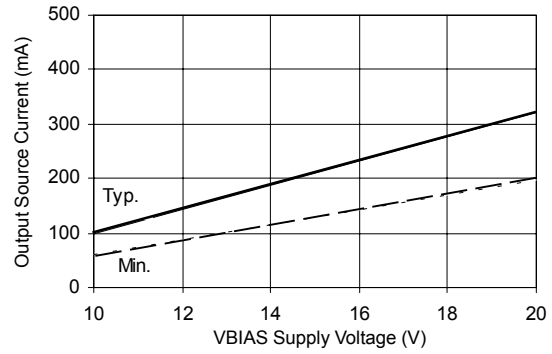


Figure 22B. Output Source Current vs Voltage

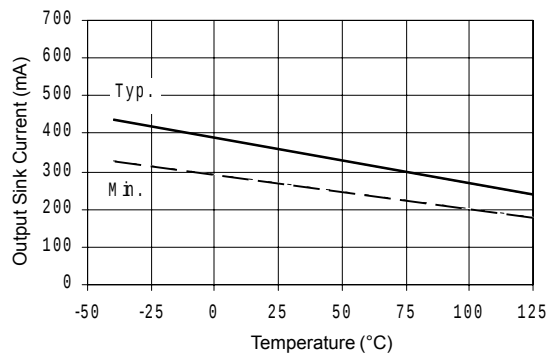


Figure 23A. Output Sink Current vs Temperature

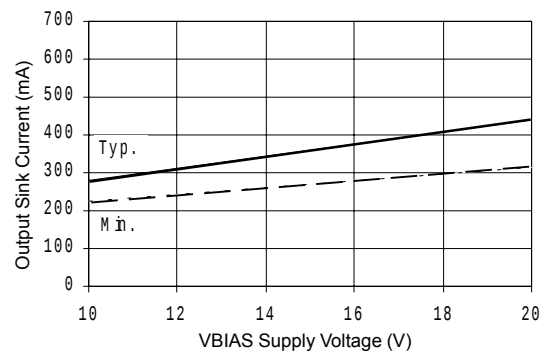


Figure 23B. Output Sink Current vs Voltage

Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales.

Shipping

Three shipping options are offered as standard.

- Un-sawn wafer
- Die in waffle pack
- Die on film

Tape and Reel is also available for some products.

Please specify your required shipping option when requesting prices and ordering Die product. If not specified, Un-sawn wafer will be assumed.

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Un-sawn wafers and singulated die can be stored for up to 12 months when in the original sealed packaging at room temperature (45% +/- 15% RH controlled environment).
- Un-sawn wafers and singulated die that have been opened can be stored when returned to their containers and placed in a Nitrogen purged cabinet, at room temperature (45% +/- 15% RH controlled environment).
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.
- Die in Surf Tape type carrier tape are intended for immediate use and have a limited shelf life. This is primarily due to the nature of the adhesive tape used to hold the product in the carrier tape cavity. This product can be stored for up to 30 days. This applies whether or not the material has remained in its original sealed container.

For further information: Please contact your local IR Sales office or email your enquiry to <http://die.irf.com>

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
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