



# **SN74AVC16T245 16-Bit Dual-Supply Bus Transceiver** **with Configurable Level-Shifting / Voltage Translation and Tri-State Outputs**

## 1 Features

- Control Inputs  $V_{IH}/V_{IL}$  Levels Are Referenced to  $V_{CCA}$  Voltage
- $V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs and Outputs Allow Mixed-Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2 V to 3.6 V Power-Supply Range
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- I/Os Are 4.6 V Tolerant
- Maximum Data Rates
  - 380 Mbps (1.8 V to 3.3 V Level-Shifting)
  - 200 Mbps (<1.8 V to 3.3 V Level-Shifting)
  - 200 Mbps (Level-Shifting to 2.5 V or 1.8 V)
  - 150 Mbps (Level-Shifting to 1.5 V)
  - 100 Mbps (Level-Shifting to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom

## 3 Description

This 16-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVC16T245 device is optimized to operate with  $V_{CCA}/V_{CCB}$  set at 1.4 V to 3.6 V. The device is operational with  $V_{CCA}/V_{CCB}$  as low as 1.2 V. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVC16T245 device is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the outputs so the buses effectively are isolated.

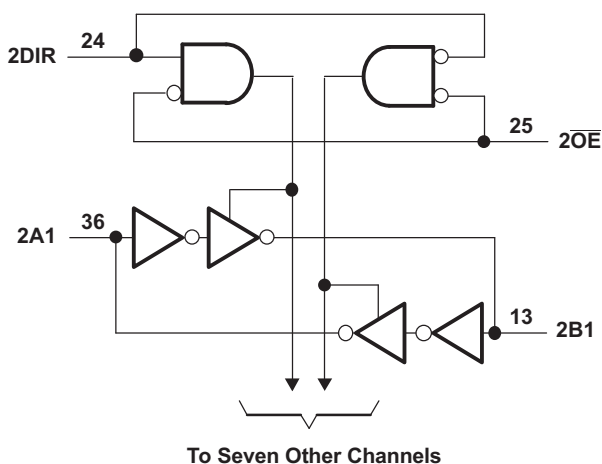
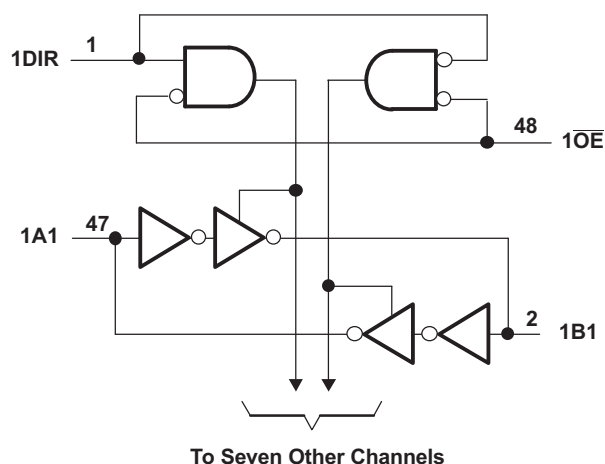
The SN74AVC16T245 control pins (1DIR, 2DIR,  $1\overline{OE}$ , and  $2\overline{OE}$ ) are supplied by  $V_{CCA}$ .

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC16T245	TSSOP (48)	12.50 mm × 6.10 mm
	TVSOP (48)	9.70 mm × 4.40 mm
	BGA MICROSTAR JUNIOR (56)	7.00 mm × 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Logic Diagram (Positive Logic)



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>9 Detailed Description</b> .....	<b>13</b>
<b>2 Applications</b> .....	<b>1</b>	9.1 Overview .....	13
<b>3 Description</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	13
<b>4 Revision History</b> .....	<b>2</b>	9.3 Feature Description .....	13
<b>5 Description (continued)</b> .....	<b>3</b>	9.4 Device Functional Modes .....	14
<b>6 Pin Configuration and Functions</b> .....	<b>4</b>	<b>10 Application and Implementation</b> .....	<b>15</b>
<b>7 Specifications</b> .....	<b>5</b>	10.1 Application Information .....	15
7.1 Absolute Maximum Ratings .....	5	10.2 Typical Application .....	16
7.2 ESD Ratings .....	5	<b>11 Power Supply Recommendations</b> .....	<b>18</b>
7.3 Recommended Operating Conditions .....	6	<b>12 Layout</b> .....	<b>18</b>
7.4 Thermal Information .....	6	12.1 Layout Guidelines .....	18
7.5 Electrical Characteristics .....	7	12.2 Layout Example .....	19
7.6 Switching Characteristics: $V_{CCA} = 1.2\text{ V}$ .....	8	<b>13 Device and Documentation Support</b> .....	<b>20</b>
7.7 Switching Characteristics: $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$ .....	8	13.1 Documentation Support .....	20
7.8 Switching Characteristics: $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$ .....	8	13.2 Community Resources .....	20
7.9 Switching Characteristics: $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ .....	9	13.3 Trademarks .....	20
7.10 Switching Characteristics: $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	9	13.4 Electrostatic Discharge Caution .....	20
7.11 Operating Characteristics .....	9	13.5 Glossary .....	20
7.12 Typical Characteristics .....	10	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>20</b>
<b>8 Parameter Measurement Information</b> .....	<b>12</b>		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (February 2015) to Revision E</b>	<b>Page</b>
• Updated Pin Functions Table. ....	<b>4</b>
<b>Changes from Revision C (August 2005) to Revision D</b>	<b>Page</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>

## 5 Description (continued)

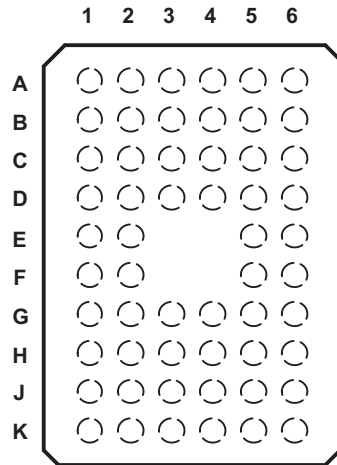
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, both ports are in the high-impedance state.

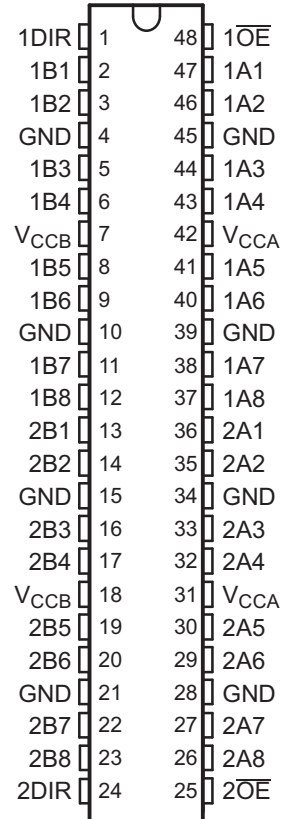
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CCA}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 6 Pin Configuration and Functions

**GQL or ZQL Package**  
**56-Pin BGA MICROSTAR JUNIOR**  
**Top View**



**DGG or DGV Package**  
**48-Pin TSSOP or TVSOP**  
**Top View**



### Pin Functions

PIN			I/O	DESCRIPTION
NAME	TSSOP, TVSOP	BGA MICROSTAR		
1DIR, 2DIR	1, 24	A1, K1	I	Direction-control signal
1B1 to 1B8	2, 3, 5, 6, 8, 9, 11, 12	B2, B1, C2, C1, D2, D1, E2, E1	I/O	Input/Output. Referenced to $V_{CCB}$
2B1 to 2B8	13, 14, 16, 17, 19, 20, 22, 23	F1, F2, G1, G2, H1, H2, J1, J2	I/O	Input/Output. Referenced to $V_{CCB}$
GND	4, 10, 15, 21, 45, 39, 34, 28	B3, D3, G3, J3, J4, G4, D4, B4	—	Ground
$V_{CCB}$	7, 18	C3, H3	—	B-port supply voltage. $1.2\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$
$1\overline{OE}$ , $2\overline{OE}$	48, 25	A6, K6	—	Tri-State output-mode enables. Pull $\overline{OE}$ high to place all outputs in Tri-State mode. Referenced to $V_{CCA}$
1A1 to 1A8	47, 46, 44, 43, 41, 40, 38, 37	B5, B6, C5, C6, D5, D6, E5, E6	I/O	Input/Output. Referenced to $V_{CCA}$
2A1 to 2A8	36, 35, 33, 32, 30, 29, 27, 26	F6, F5, G6, G5, H6, H5, J6, J5	I/O	Input/Output. Referenced to $V_{CCA}$
$V_{CCA}$	42, 31	C4, H4	—	A-port supply voltage. $1.2\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$
N.C.	—	A2, A3, A4, A5, K2, K3, K4, K5	—	No internal connection

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CCA}$ $V_{CCB}$	Supply voltage	–0.5	4.6	V
$V_I$	Input voltage <sup>(2)</sup>	I/O ports (A port)	–0.5	4.6
		I/O ports (B port)	–0.5	4.6
		Control inputs	–0.5	4.6
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	–0.5	4.6
		B port	–0.5	4.6
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	A port	–0.5	$V_{CCA} + 0.5$
		B port	–0.5	$V_{CCB} + 0.5$
$I_{IK}$	Input clamp current	$V_I < 0$	–50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	–50	mA
$I_O$	Continuous output current		±50	mA
	Continuous current through each $V_{CCA}$ , $V_{CCB}$ , and GND		±100	mA
$R_{\theta JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	70	°C/W
		DGV package	58	
		GQL/ZQL package	42	
$T_J$	Junction temperature		–40	150
$T_{stg}$	Storage temperature		–65	150

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input voltage ( $V_I$ ) and output negative-voltage ( $V_O$ ) ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±8000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	
	Machine model (A115-A)	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

## SN74AVC16T245

SCES551E –FEBRUARY 2004–REVISED NOVEMBER 2015

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### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)(3)</sup>

			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.2	3.6	V
V <sub>CCB</sub>	Supply voltage				1.2	3.6	V
V <sub>IH</sub>	High-level input voltage	Data inputs <sup>(4)</sup>	1.2 V to 1.95 V		V <sub>CCI</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	Data inputs <sup>(4)</sup>	1.2 V to 1.95 V		V <sub>CCI</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>IH</sub>	High-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.2 V to 1.95 V		V <sub>CCA</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	DIR (referenced to V <sub>CCA</sub> ) <sup>(5)</sup>	1.2 V to 1.95 V		V <sub>CCA</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>I</sub>	Input voltage				0	3.6	V
V <sub>O</sub>	Output voltage	Active state			0	V <sub>CCO</sub>	V
		Tri-State			0	3.6	
I <sub>OH</sub>	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I <sub>OL</sub>	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T <sub>A</sub>	Operating free-air temperature				–40	85	°C

(1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the data input port.

(2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

(3) All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

(4) For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCI</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCI</sub> × 0.3 V.

(5) For V<sub>CCA</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCA</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCA</sub> × 0.3 V.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AVC16T245			UNIT
		DGV (TVSOP)	DGG (TSSOP)	ZQL (BGA MICROSTAR JUNIOR)	
		48 PINS	48 PINS	56 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	82.5	69.9	64.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	34.2	23.9	16.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	45.1	36.6	30.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.7	1.7	0.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	44.6	36.2	64.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

PARAMETER	TEST CONDITIONS	$V_{CCA}$	$V_{CCB}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH}$	$I_{OH} = -100\ \mu\text{A}$	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V			$V_{CCO} - 0.2$			V
	$I_{OH} = -3\ \text{mA}$		1.2 V	1.2 V	0.95					
	$I_{OH} = -6\ \text{mA}$		1.4 V	1.4 V			1.05			
	$I_{OH} = -8\ \text{mA}$		1.65 V	1.65 V			1.2			
	$I_{OH} = -9\ \text{mA}$		2.3 V	2.3 V			1.75			
	$I_{OH} = -12\ \text{mA}$		3 V	3 V			2.3			
$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
	$I_{OL} = 3\ \text{mA}$		1.2 V	1.2 V	0.15					
	$I_{OL} = 6\ \text{mA}$		1.4 V	1.4 V					0.35	
	$I_{OL} = 8\ \text{mA}$		1.65 V	1.65 V					0.45	
	$I_{OL} = 9\ \text{mA}$		2.3 V	2.3 V					0.55	
	$I_{OL} = 12\ \text{mA}$		3 V	3 V					0.7	
$I_I$	Control inputs	$V_I = V_{CCA}$ or GND	1.2 V to 3.6 V	1.2 V to 3.6 V	$\pm 0.025$	$\pm 0.25$			$\pm 1$	$\mu\text{A}$
$I_{off}$	A or B port	$V_I$ or $V_O = 0$ to 3.6 V	0 V	0 to 3.6 V	$\pm 0.1$	$\pm 2.5$			$\pm 5$	$\mu\text{A}$
	A or B port		0 to 3.6 V	0 V	$\pm 0.5$	$\pm 2.5$			$\pm 5$	
$I_{OZ}^{(3)}$	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $OE = V_{IH}$	3.6 V	3.6 V	$\pm 0.5$	$\pm 2.5$			$\pm 5$	$\mu\text{A}$
$I_{CCA}$	$V_I = V_{CCI}$ or GND, $I_O = 0$		1.2 V to 3.6 V	1.2 V to 3.6 V					25	$\mu\text{A}$
			0 V	3.6 V					-5	
			3.6 V	0 V					25	
$I_{CCB}$	$V_I = V_{CCI}$ or GND, $I_O = 0$		1.2 V to 3.6 V	1.2 V to 3.6 V					25	$\mu\text{A}$
			0 V	3.6 V					25	
			3.6 V	0 V					-5	
$I_{CCA} + I_{CCB}$	$V_I = V_{CCI}$ or GND, $I_O = 0$		1.2 V to 3.6 V	1.2 V to 3.6 V					45	$\mu\text{A}$
$C_i$	Control inputs	$V_I = 3.3\ \text{V}$ or GND	3.3 V	3.3 V		3.5				pF
$C_{io}$	A or B port	$V_O = 3.3\ \text{V}$ or GND	3.3 V	3.3 V		7				pF

(1)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

(2)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

(3) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

# SN74AVC16T245

SCES551E –FEBRUARY 2004–REVISED NOVEMBER 2015

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## 7.6 Switching Characteristics: $V_{CCA} = 1.2\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.2\text{ V}$  (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V			V <sub>CCB</sub> = 1.5 V			V <sub>CCB</sub> = 1.8 V			V <sub>CCB</sub> = 2.5 V			V <sub>CCB</sub> = 3.3 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PLH</sub>	A	B	4.1			3.3			3			2.8			3.2			ns
t <sub>PHL</sub>			4.1			3.3			3			2.8			3.2			
t <sub>PLH</sub>	B	A	4.4			4			3.8			3.6			3.5			ns
t <sub>PHL</sub>			4.4			4			3.8			3.6			3.5			
t <sub>PZH</sub>	OE	A	6.4			6.4			6.4			6.4			6.4			ns
t <sub>PZL</sub>			6.4			6.4			6.4			6.4			6.4			
t <sub>PZH</sub>	OE	B	6			4.6			4			3.4			3.2			ns
t <sub>PZL</sub>			6			4.6			4			3.4			3.2			
t <sub>PHZ</sub>	OE	A	6.6			6.6			6.6			6.6			6.8			ns
t <sub>PLZ</sub>			6.6			6.6			6.6			6.6			6.8			
t <sub>PHZ</sub>	OE	B	6			4.9			4.9			4.2			5.3			ns
t <sub>PLZ</sub>			6			4.9			4.9			4.2			5.3			

## 7.7 Switching Characteristics: $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$  (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V			V <sub>CCB</sub> = 1.5 V ± 0.1 V			V <sub>CCB</sub> = 1.8 V ± 0.15 V			V <sub>CCB</sub> = 2.5 V ± 0.2 V			V <sub>CCB</sub> = 3.3 V ± 0.3 V			UNIT												
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX													
t <sub>PLH</sub>	A	B	3.6			0.5			6.2			0.5			4.1			0.5			3.7			ns						
t <sub>PHL</sub>			3.6			0.5			6.2			0.5			5.2			0.5			4.1				0.5			3.7		
t <sub>PLH</sub>	B	A	3.3			0.5			6.2			0.5			5.9			0.5			5.6			0.5			5.5			ns
t <sub>PHL</sub>			3.3			0.5			6.2			0.5			5.9			0.5			5.6			0.5			5.5			
t <sub>PZH</sub>	OE	A	4.3			1			10.1			1			10.1			1			10.1			1			10.1			ns
t <sub>PZL</sub>			4.3			1			10.1			1			10.1			1			10.1			1			10.1			
t <sub>PZH</sub>	OE	B	5.6			1			10.1			0.5			8.1			0.5			5.9			0.5			5.2			ns
t <sub>PZL</sub>			5.6			1			10.1			0.5			8.1			0.5			5.9			0.5			5.2			
t <sub>PHZ</sub>	OE	A	4.5			1.5			9.1			1.5			9.1			1.5			9.1			1.5			9.1			ns
t <sub>PLZ</sub>			4.5			1.5			9.1			1.5			9.1			1.5			9.1			1.5			9.1			
t <sub>PHZ</sub>	OE	B	5.5			1.5			8.7			1.5			7.5			1			6.5			1			6.3			ns
t <sub>PLZ</sub>			5.5			1.5			8.7			1.5			7.5			1			6.5			1			6.3			

## 7.8 Switching Characteristics: $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$  (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V			V <sub>CCB</sub> = 1.5 V ± 0.1 V			V <sub>CCB</sub> = 1.8 V ± 0.15 V			V <sub>CCB</sub> = 2.5 V ± 0.2 V			V <sub>CCB</sub> = 3.3 V ± 0.3 V			UNIT												
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX													
t <sub>PLH</sub>	A	B	3.4			0.5			5.9			0.5			4.8			0.5			3.7			0.5			3.3			ns
t <sub>PHL</sub>			3.4			0.5			5.9			0.5			4.8			0.5			3.7			0.5			3.3			
t <sub>PLH</sub>	B	A	3			0.5			5.2			0.5			4.8			0.5			4.5			0.5			4.4			ns
t <sub>PHL</sub>			3			0.5			5.2			0.5			4.8			0.5			4.5			0.5			4.4			
t <sub>PZH</sub>	OE	A	3.4			1			7.8			1			7.8			1			7.8			1			7.8			ns
t <sub>PZL</sub>			3.4			1			7.8			1			7.8			1			7.8			1			7.8			
t <sub>PZH</sub>	OE	B	5.4			1			9.2			0.5			7.4			0.5			5.3			0.5			4.5			ns
t <sub>PZL</sub>			5.4			1			9.2			0.5			7.4			0.5			5.3			0.5			4.5			
t <sub>PHZ</sub>	OE	A	4.2			1.5			7.7			1.5			7.7			1.5			7.7			1.5			7.7			ns
t <sub>PLZ</sub>			4.2			1.5			7.7			1.5			7.7			1.5			7.7			1.5			7.7			
t <sub>PHZ</sub>	OE	B	5.2			1.5			8.4			1.5			7.1			1			5.9			1			5.7			ns
t <sub>PLZ</sub>			5.2			1.5			8.4			1.5			7.1			1			5.9			1			5.7			



## 7.9 Switching Characteristics: $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$  (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V			V <sub>CCB</sub> = 1.5 V ± 0.1 V			V <sub>CCB</sub> = 1.8 V ± 0.15 V			V <sub>CCB</sub> = 2.5 V ± 0.2 V			V <sub>CCB</sub> = 3.3 V ± 0.3 V			UNIT												
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX													
t <sub>PLH</sub>	A	B	3.2			0.5			5.6			0.5			4.5			0.5			3.3			0.5			2.8			ns
t <sub>PHL</sub>			3.2			0.5			5.6			0.5			4.5			0.5			3.3			0.5			2.8			
t <sub>PLH</sub>	B	A	2.6			0.5			4.1			0.5			3.7			0.5			3.3			0.5			3.2			ns
t <sub>PHL</sub>			2.6			0.5			4.1			0.5			3.7			0.5			3.3			0.5			3.2			
t <sub>PZH</sub>	OE	A	2.5			0.5			5.3			0.5			5.3			0.5			5.3			0.5			5.3			ns
t <sub>PZL</sub>			2.5			0.5			5.3			0.5			5.3			0.5			5.3			0.5			5.3			
t <sub>PZH</sub>	OE	B	5.2			0.5			9.4			0.5			7.3			0.5			5.1			0.5			4.5			ns
t <sub>PZL</sub>			5.2			0.5			9.4			0.5			7.3			0.5			5.1			0.5			4.5			
t <sub>PHZ</sub>	OE	A	3			1			6.1			1			6.1			1			6.1			1			6.1			ns
t <sub>PLZ</sub>			3			1			6.1			1			6.1			1			6.1			1			6.1			
t <sub>PHZ</sub>	OE	B	5			1			7.9			1			6.6			1			6.1			1			5.2			ns
t <sub>PLZ</sub>			5			1			7.9			1			6.6			1			6.1			1			5.2			

## 7.10 Switching Characteristics: $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$  (see [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CCB</sub> = 1.2 V			V <sub>CCB</sub> = 1.5 V ± 0.1 V			V <sub>CCB</sub> = 1.8 V ± 0.15 V			V <sub>CCB</sub> = 2.5 V ± 0.2 V			V <sub>CCB</sub> = 3.3 V ± 0.3 V			UNIT												
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX													
t <sub>PLH</sub>	A	B	3.2			0.5			5.5			0.5			4.4			0.5			3.2			0.5			2.7			ns
t <sub>PHL</sub>			3.2			0.5			5.5			0.5			4.4			0.5			3.2			0.5			2.7			
t <sub>PLH</sub>	B	A	2.8			0.5			3.7			0.5			3.3			0.5			2.8			0.5			2.7			ns
t <sub>PHL</sub>			2.8			0.5			3.7			0.5			3.3			0.5			2.8			0.5			2.7			
t <sub>PZH</sub>	OE	A	2.2			0.5			4.3			0.5			4.2			0.5			4.1			0.5			4			ns
t <sub>PZL</sub>			2.2			0.5			4.3			0.5			4.2			0.5			4.1			0.5			4			
t <sub>PZH</sub>	OE	B	5.1			0.5			9.3			0.5			7.2			0.5			4.9			0.5			4			ns
t <sub>PZL</sub>			5.1			0.5			9.3			0.5			7.2			0.5			4.9			0.5			4			
t <sub>PHZ</sub>	OE	A	3.4			0.5			5			0.5			5			0.5			5			0.5			5			ns
t <sub>PLZ</sub>			3.4			0.5			5			0.5			5			0.5			5			0.5			5			
t <sub>PHZ</sub>	OE	B	4.9			1			7.7			1			6.5			1			5.2			0.5			5			ns
t <sub>PLZ</sub>			4.9			1			7.7			1			6.5			1			5.2			0.5			5			

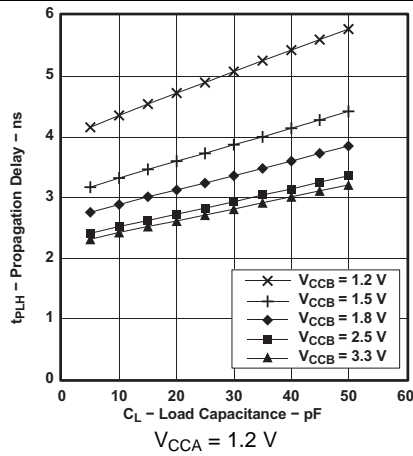
## 7.11 Operating Characteristics

$T_A = 25^\circ\text{C}$

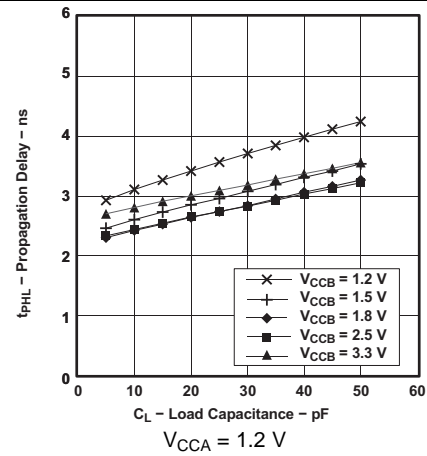
PARAMETER			TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.2\text{ V}$			$V_{CCA} = V_{CCB} = 1.5\text{ V}$			$V_{CCA} = V_{CCB} = 1.8\text{ V}$			$V_{CCA} = V_{CCB} = 2.5\text{ V}$			$V_{CCA} = V_{CCB} = 3.3\text{ V}$			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$C_{pdA}^{(1)}$	A to B	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$ , $t_r = t_f = 1\text{ ns}$	1			1			1			1			2			pF
		Outputs disabled		1			1			1			1			1			
	B to A	Outputs enabled		13			13			14			15			16			
		Outputs disabled		1			1			1			1			1			
$C_{pdB}^{(1)}$	A to B	Outputs enabled	$C_L = 0$ , $f = 10\text{ MHz}$ , $t_r = t_f = 1\text{ ns}$	13			13			14			15			16			pF
		Outputs disabled		1			1			1			1			1			
	B to A	Outputs enabled		1			1			1			1			2			
		Outputs disabled		1			1			1			1			1			

(1) Power dissipation capacitance per transceiver. Refer to the TI application report, *CMOS Power Consumption and Cpd Calculation*, [SCAA035](#)

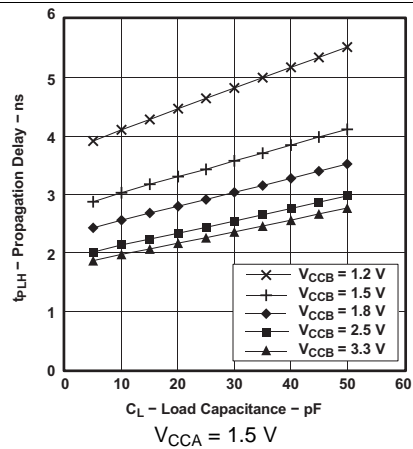
## 7.12 Typical Characteristics

 $T_A = 25^\circ\text{C}$ 


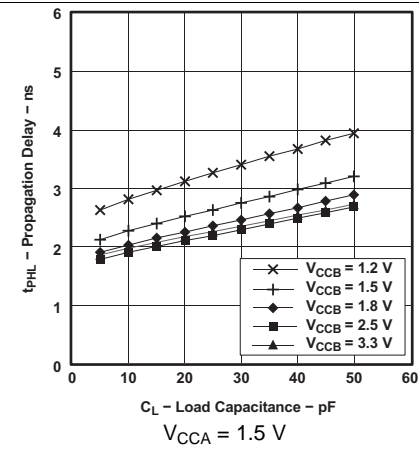
**Figure 1. Typical Propagation Delay  $t_{PLH}$  (A to B) vs Load Capacitance**



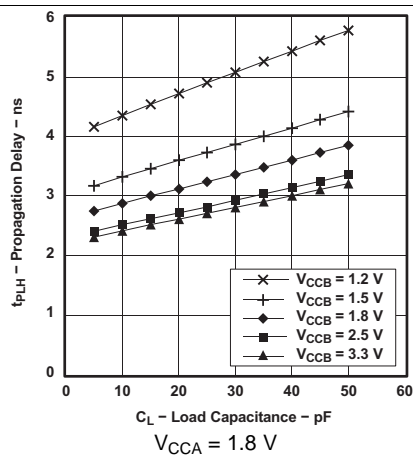
**Figure 2. Typical Propagation Delay  $t_{PHL}$  (A to B) vs Load Capacitance**



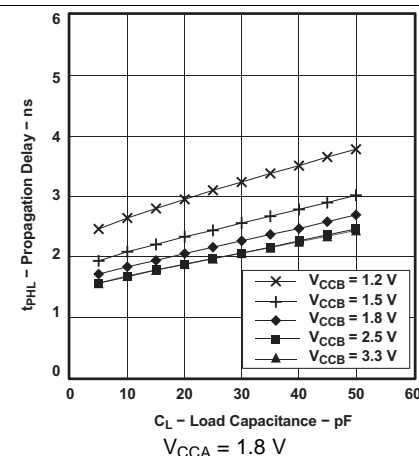
**Figure 3. Typical Propagation Delay  $t_{PLH}$  (A to B) vs Load Capacitance**



**Figure 4. Typical Propagation Delay  $t_{PHL}$  (A to B) vs Load Capacitance**



**Figure 5. Typical Propagation Delay  $t_{PLH}$  (A to B) vs Load Capacitance**



**Figure 6. Typical Propagation Delay  $t_{PHL}$  (A to B) vs Load Capacitance**

## Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$

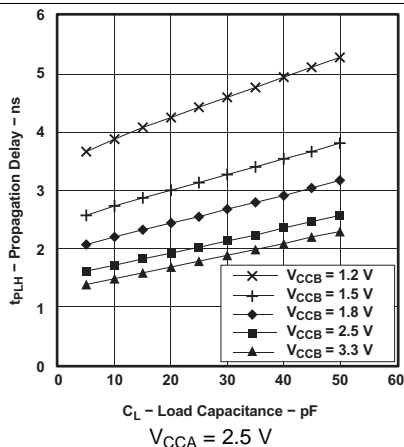


Figure 7. Typical Propagation Delay  $t_{PLH}$  (A to B) vs Load Capacitance

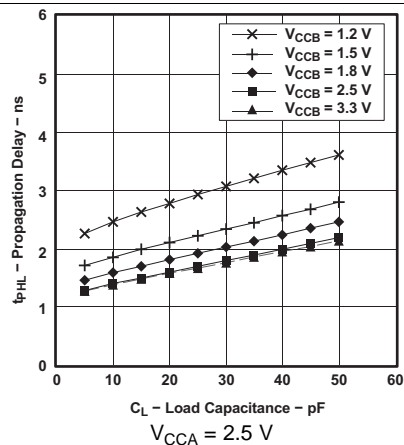


Figure 8. Typical Propagation Delay  $t_{PHL}$  (A to B) vs Load Capacitance

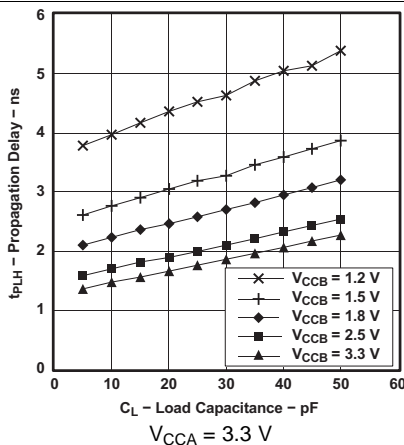


Figure 9. Typical Propagation Delay  $t_{PLH}$  (A to B) vs Load Capacitance

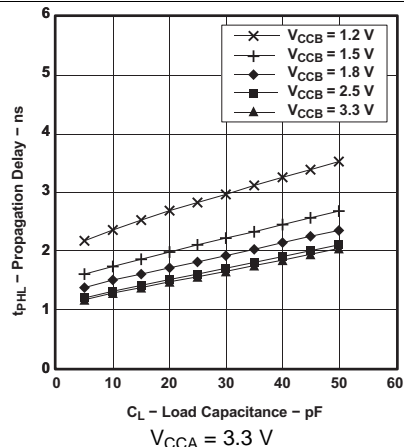
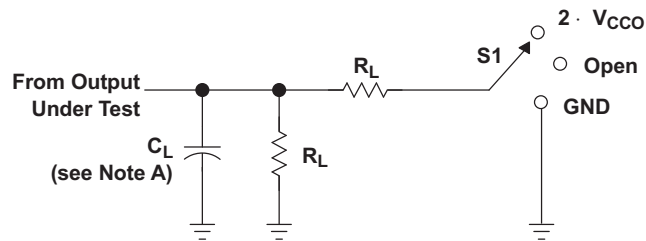


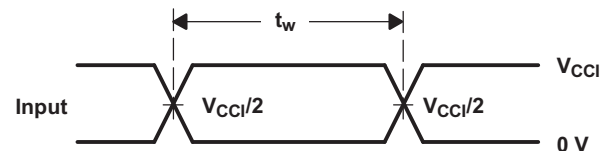
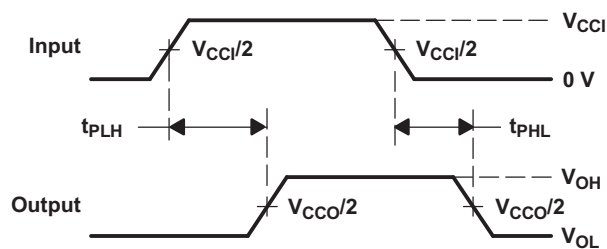
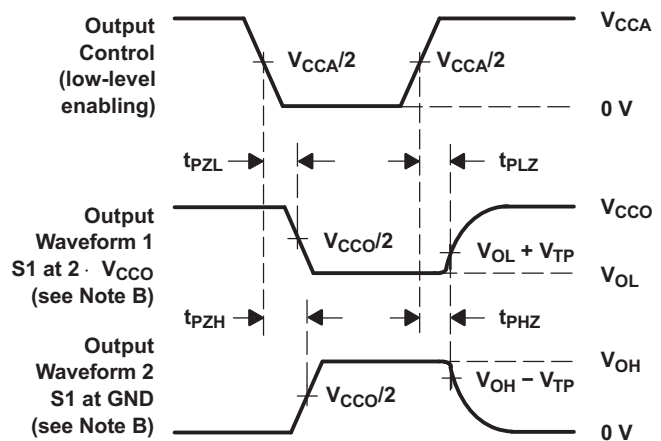
Figure 10. Typical Propagation Delay  $t_{PHL}$  (A to B) vs Load Capacitance

## 8 Parameter Measurement Information


**LOAD CIRCUIT**

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
1.2 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	2 k $\Omega$	0.3 V

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \cdot V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND


**VOLTAGE WAVEFORMS  
PULSE DURATION**

**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz,  $Z_O = 50 \Omega$ ,  $dv/dt \geq 1$  V/ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - F.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
  - G.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

**Figure 11. Load Circuit and Voltage Waveforms**

## 9 Detailed Description

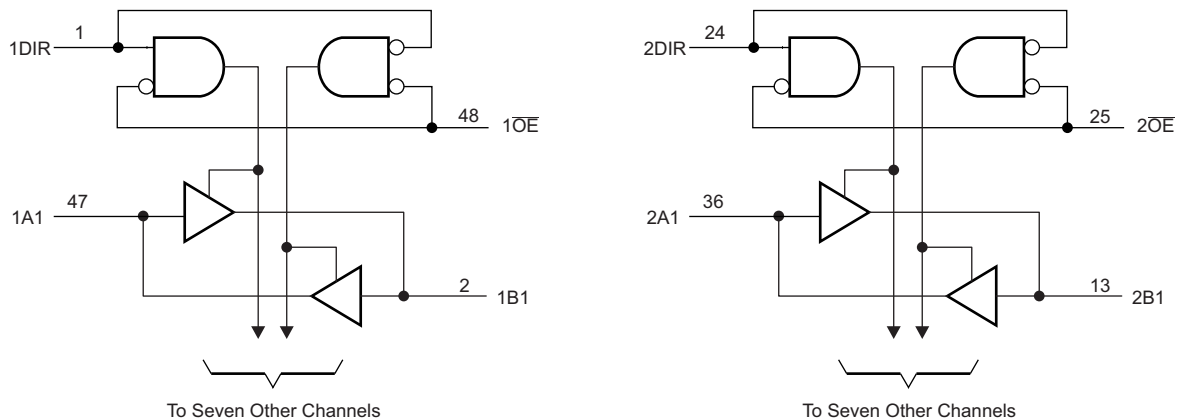
### 9.1 Overview

The SN74AVC16T245 is a 16-bit, dual-supply noninverting bidirectional voltage level translation. Pins A and control pins (DIR and  $\overline{OE}$ ) are supported by  $V_{CCA}$  and pins B are supported by  $V_{CCB}$ . The A port can accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from A to B and a low on DIR allows data transmission from B to A when  $\overline{OE}$  is set to low. When  $\overline{OE}$  is set to high, both A and B are in the high-impedance state.

This device is fully specified for partial-power-down applications using off output current ( $I_{off}$ ).

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, both ports are put in a high-impedance state.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range

Both  $V_{CCA}$  and  $V_{CCB}$  can be supplied at any voltage from 1.2 V to 3.6 V making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

#### 9.3.2 Partial-Power-Down Mode Operation

This device is fully specified for partial-power-down applications using off output current ( $I_{off}$ ). The  $I_{off}$  circuitry will prevent backflow current by disabling I/O output circuits when device is in partial power-down mode.

#### 9.3.3 $V_{CC}$ Isolation

The  $V_{CC}$  isolation feature ensures that if either  $V_{CCA}$  or  $V_{CCB}$  are at GND, both ports will be in a high-impedance state ( $I_{OZ}$  shown in [Electrical Characteristics](#)). This prevents false logic levels from being presented to either bus.

## SN74AVC16T245

SCES551E –FEBRUARY 2004–REVISED NOVEMBER 2015

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### 9.4 Device Functional Modes

The SN74AVC16T245 is a voltage level translator that can operate from 1.2 V to 3.6 V ( $V_{CCA}$ ) and 1.2 V to 3.6 V ( $V_{CCB}$ ). The signal translation between 1.2 V and 3.6 V requires direction control and output enable control. When  $\overline{OE}$  is low and DIR is high, data transmission is from A to B. When  $\overline{OE}$  is low and DIR is low, data transmission is from B to A. When  $\overline{OE}$  is high, both output ports will be high-impedance.

**Table 1. Functions Table<sup>(1)</sup>**

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The SN74AVC16T245 device can be used in level-shifting applications for interfacing devices and addressing mixed voltage incompatibility. The SN74AVC16T245 device is ideal for data transmission where direction is different for each channel.

#### 10.1.1 Enable Times

Calculate the enable times for the SN74AVC16T45 using the following formulas:

$$t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)} \quad (1)$$

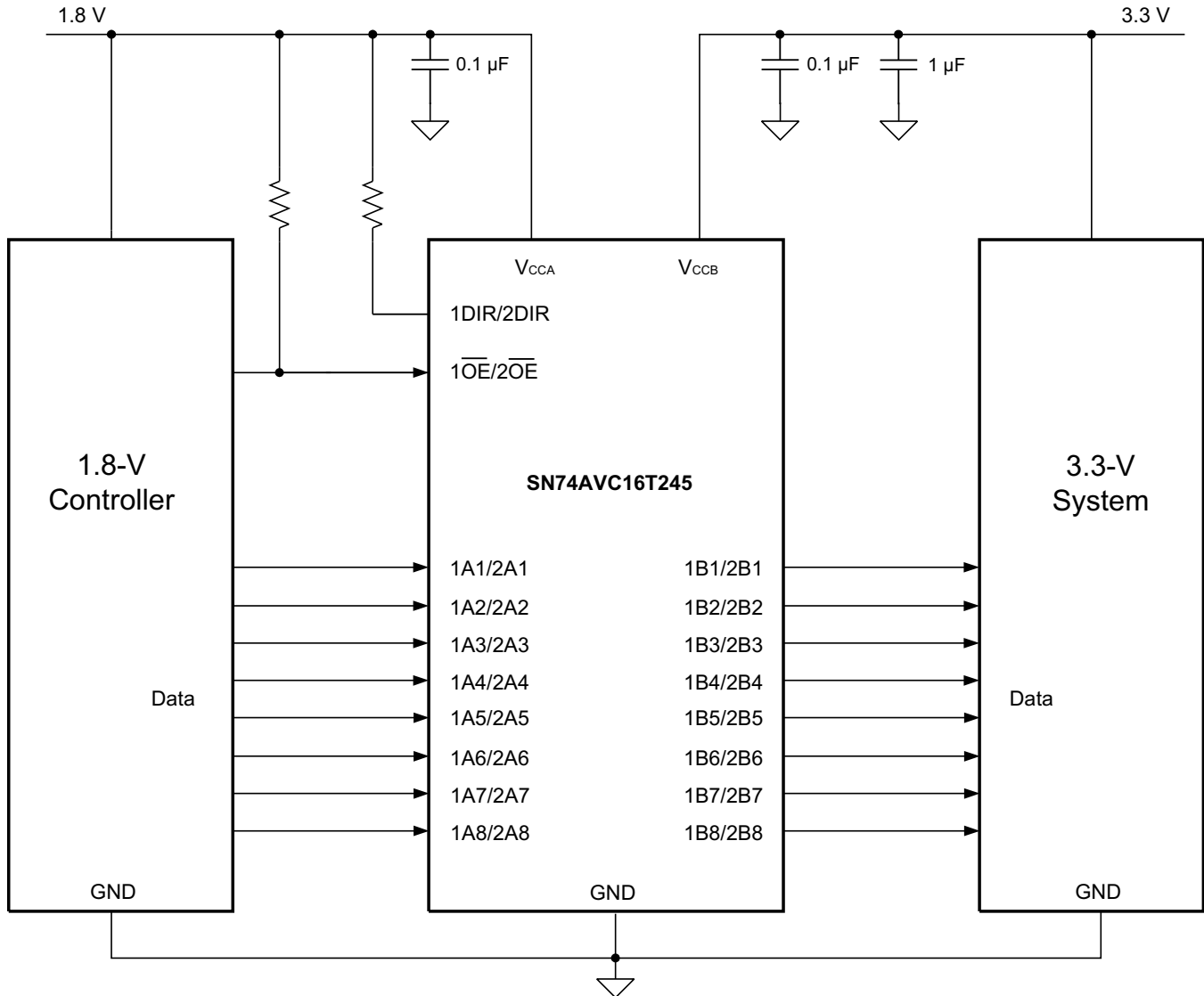
$$t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)} \quad (2)$$

$$t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)} \quad (3)$$

$$t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)} \quad (4)$$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC16T245 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

## 10.2 Typical Application



**Figure 12. Typical Application Schematic**

### 10.2.1 Design Requirements

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Tie any unused input and output ports directly to ground.

For this design example, use the parameters listed in [Table 2](#).

**Table 2. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.2 V to 3.6 V



## 10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

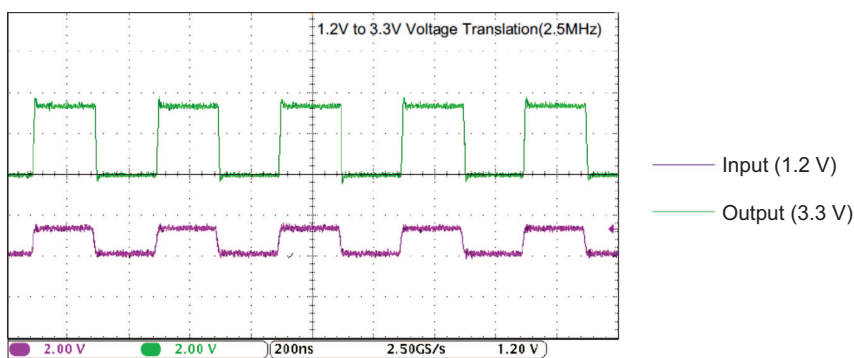
### 10.2.2.1 Input Voltage Ranges

Use the supply voltage of the device that is driving the SN74AVC16T245 device to determine the input voltage range. For a valid logic high the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value must be less than the  $V_{IL}$  of the input port.

### 10.2.2.2 Output Voltage Range

Use the supply voltage of the device that the SN74AVC16T245 device is driving to determine the output voltage range.

## 10.2.3 Application Curve



**Figure 13. Translation Up (1.2 V to 3.3 V) at 2.5 MHz**

## 11 Power Supply Recommendations

The SN74AVC16T245 device uses two separate configurable power-supply rails,  $V_{CCA}$  and  $V_{CCB}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V and  $V_{CCB}$  accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track  $V_{CCA}$  and  $V_{CCB}$ , respectively, allowing for low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes.

The output-enable  $\overline{OE}$  input circuit is designed so that it is supplied by  $V_{CCA}$  and when the  $\overline{OE}$  input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the  $\overline{OE}$  input pin must be tied to  $V_{CCA}$  through a pullup resistor and must not be enabled until  $V_{CCA}$  and  $V_{CCB}$  are fully ramped and stable. The minimum value of the pullup resistor to  $V_{CCA}$  is determined by the current-sinking capability of the driver.

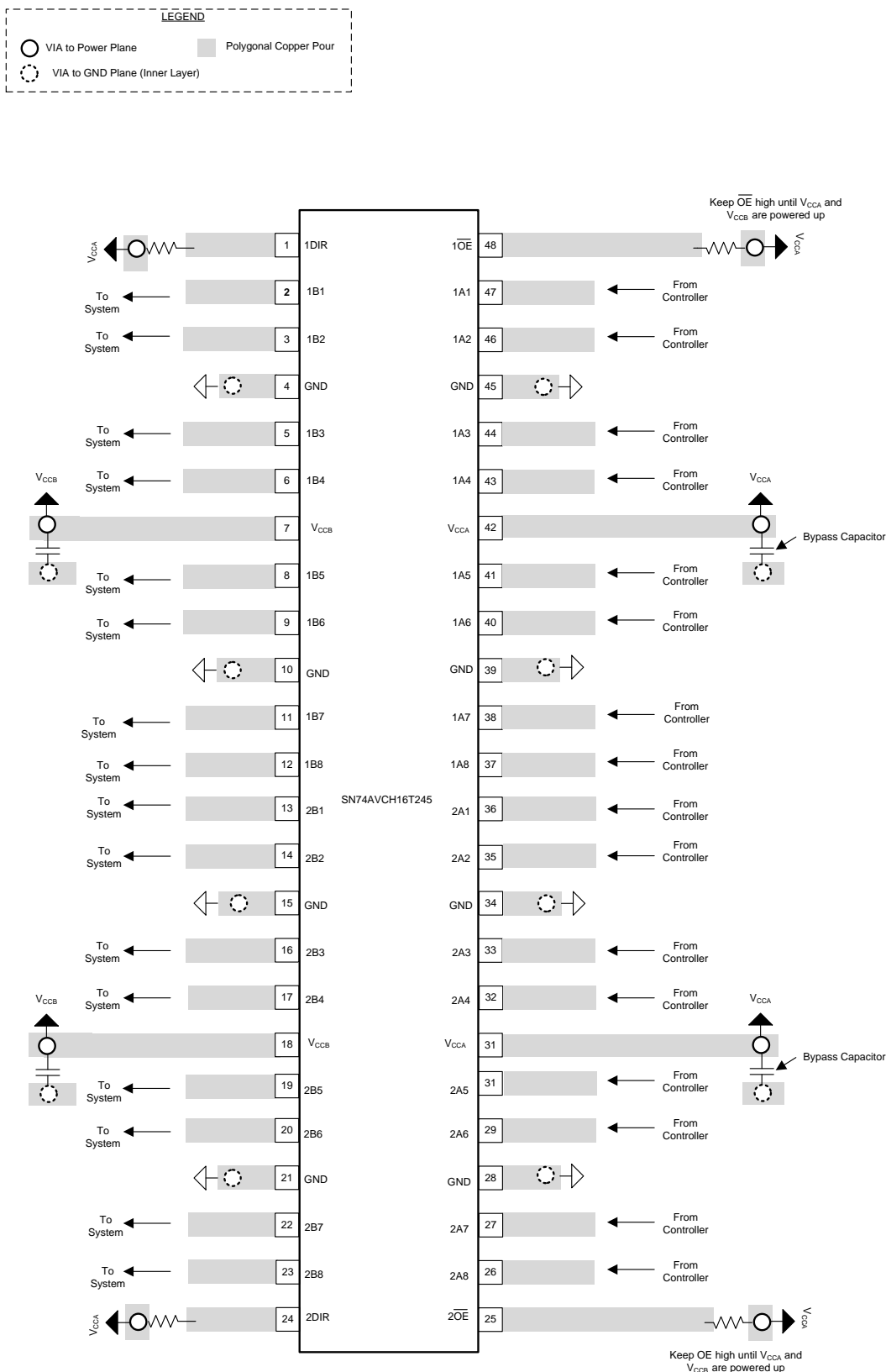
## 12 Layout

### 12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit-board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

## 12.2 Layout Example



**Figure 14. Recommended Layout Example**

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation see the following:

- *CMOS Power Consumption and Cpd Calculation*, [SCAA035](#)
- *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

### 13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVC16T245DGVRE4	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WF245	<a href="#">Samples</a>
AVC16T245DGGR-D	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC16T245	<a href="#">Samples</a>
SN74AVC16T245DGG	ACTIVE	TSSOP	DGG	48	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC16T245	<a href="#">Samples</a>
SN74AVC16T245DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC16T245	<a href="#">Samples</a>
SN74AVC16T245DGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WF245	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AVC16T245 :**

- Automotive : [SN74AVC16T245-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC16T245DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AVC16T245DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC16T245DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74AVC16T245DGVR	TVSOP	DGV	48	2000	356.0	356.0	35.0

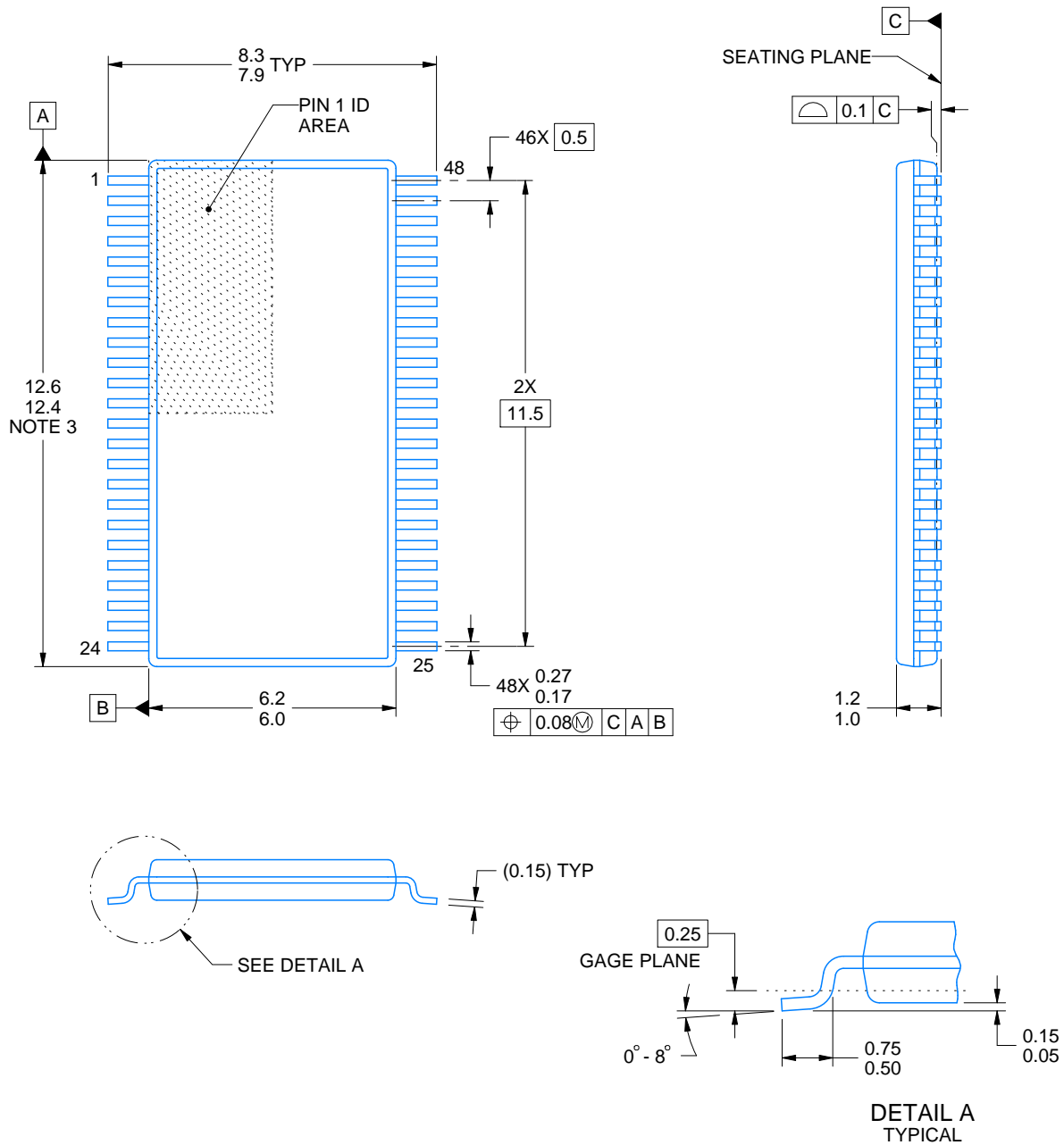
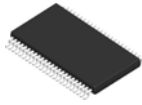


## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AVC16T245DGG	DGG	TSSOP	48	40	530	11.89	3600	4.9



4214859/B 11/2020

## NOTES:

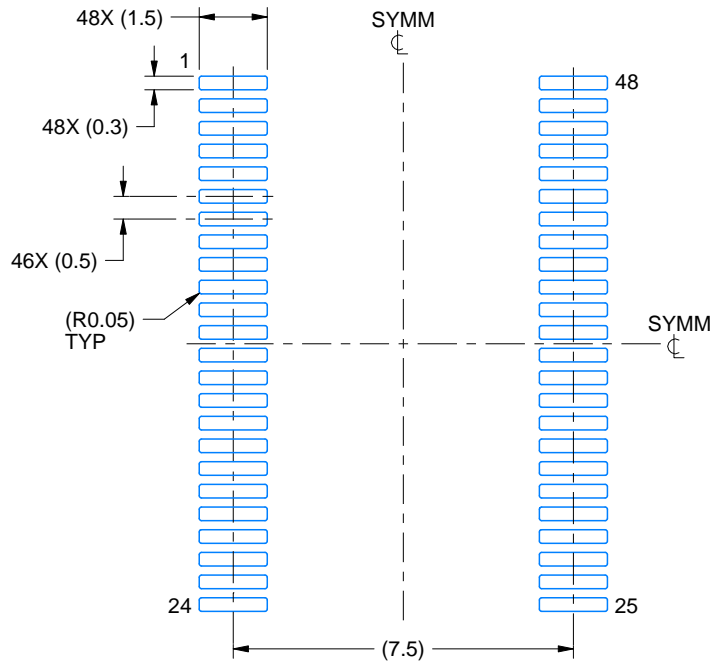
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

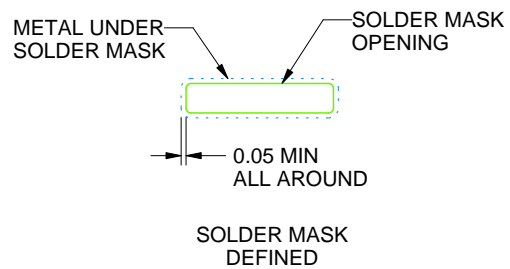
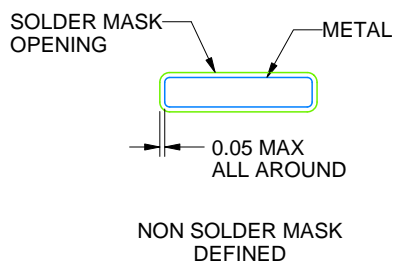
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

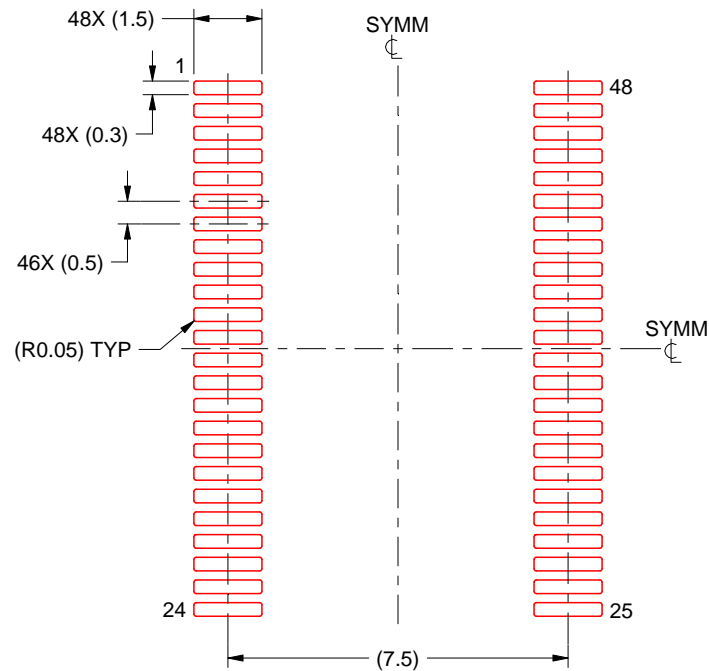
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153