HOLT INTEGRATED CIRCUITS INC.

HI-8429

June 2017

8-Channel GND/Open or Supply/Open Sensor with Programmable Thresholds and SPI Interface

GENERAL DESCRIPTION

The HI-8429 is an 8-channel discrete-to-digital sensor fabricated with Silicon-on-Insulator (SOI) technology designed to interface with a Serial Peripheral Interface (SPI).

Each input is individually configurable as either GND/Open or Supply/Open (28V/Open). Discrete input thresholds are programmable in the range of 2V to 12V. An SPI bus is used to configure the sensors and to read sensor data .

The part operates from a 3.3V (±5%) digital supply and 12V to 15V analog supply.

A 1mA wetting current is sourced from the input network on each SENSE input when GND/Open mode is selected for that pin. The wetting current serves to prevent dry relay or switch contacts. An optional debounce circuit also ensures sensor outputs respond correctly to mechanical sensor inputs. A sensor output interrupt pin alerts the system to a change in sensor input, avoiding constant polling via SPI to check status.

All sense inputs are internally lightning protected to RTCA/DO160G, Section 22 Level 3 Pin Injection Test Waveform Set A(3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) without the using external components.

Higher levels of lightning protection can be achieved with an external series resistor and transorb at each SENSE input, refer to AN305 for more details.

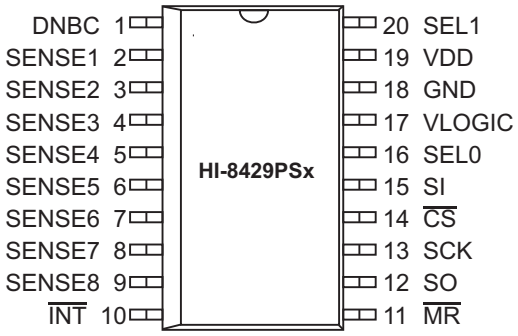
APPLICATION

- Avionics Discrete to Digital Sensing

FEATURES

- Robust CMOS Silicon-on-Insulator (SOI) technology
- Eight discrete inputs, individually configurable as GND/Open or Supply/Open
- Interrupt generated on any change of sensor state
- SPI programmable sensor thresholds
- Sensor data read through SPI bus
- Airbus ABD0100H specification compliant
- MIL-STD-704 compliant
- Sense inputs lightning protected to RTCA/DO1060G, Section 22 Level 3
- 10MHz Serial Peripheral Interface (SPI) allows daisy-chaining of parts for efficient board routing
- Withstands inadvertent application of 115V AC/400Hz power to Sense inputs.
- Internal Self-Test mode checks analog comparators

PIN CONFIGURATION



20-Pin Plastic Small Outline Wide-body Package

BLOCK DIAGRAM

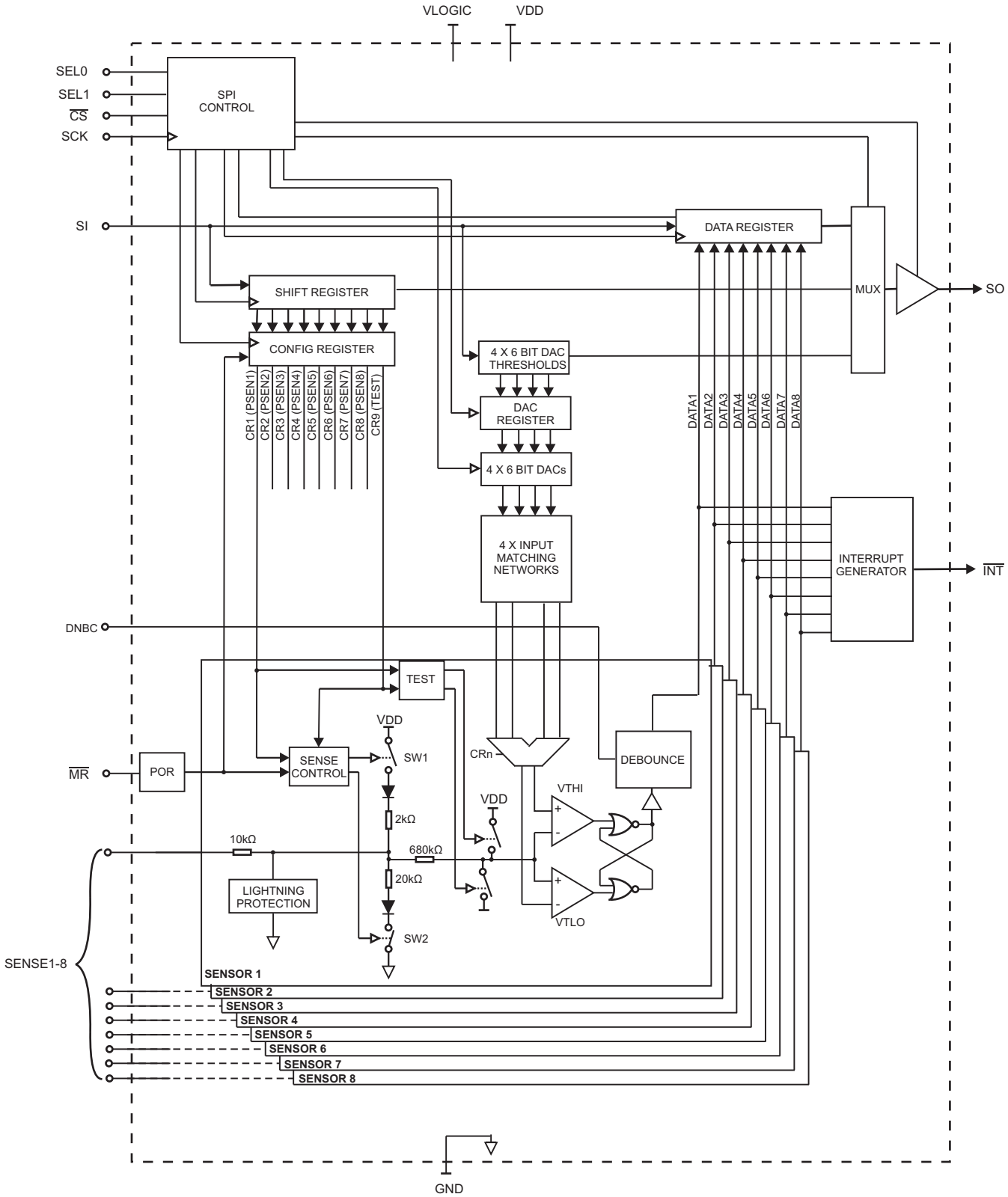


Figure 1.

PIN DESCRIPTIONS

PIN (SOIC)	PIN (QFN)	SYMBOL	FUNCTION	DESCRIPTION
1	36	DNBC	Logic Input	Debounce Enable Input; High = Enabled. Low = Disabled, 10kΩ pull-down to GND
2	2	SENSE1	Discrete Input	Sense input 1. Mapped to last (eighth) SPI bit shifted out of SO during data read
3	3	SENSE2	Discrete Input	Sense input 2. Mapped to seventh SPI bit shifted out of SO during data read
4	4	SENSE3	Discrete Input	Sense input 3. Mapped to sixth SPI bit shifted out of SO during data read
5	5	SENSE4	Discrete Input	Sense input 4. Mapped to fifth SPI bit shifted out of SO during data read
6	6	SENSE5	Discrete Input	Sense input 5. Mapped to fourth SPI bit shifted out of SO during data read
7	7	SENSE6	Discrete Input	Sense input 6. Mapped to third SPI bit shifted out of SO during data read
8	8	SENSE7	Discrete Input	Sense input 7. Mapped to second SPI bit shifted out of SO during data read
9	14	SENSE8	Discrete Input	Sense input 8. Mapped to first SPI bit shifted out of SO during data read
10	15	$\overline{\text{INT}}$	Digital Output	Interrupt output, generates a 1us low pulse when any sensor changes state, open drain
11	16	$\overline{\text{MR}}$	Logic Input	Master Reset, active low, internal 10kΩ pull-up to VLOGIC
12	17	SO	Digital Output	SPI Data out
13	22	SCK	Logic Input	SPI clock input. 10MHz maximum clock frequency.
14	23	$\overline{\text{CS}}$	Logic Input	Chip Select. SPI data transfers are enabled when $\overline{\text{CS}}$ is low
15	24	SI	Logic Input	SPI Data input.
16	25	SEL0	Logic Input	With SEL1 selects SPI function, see table 1
17	27	VLOGIC	Supply	Logic supply voltage
18	29	GND	Supply	Ground
19	34	VDD	Supply	Analog Supply voltage
20	35	SEL1	Logic Input	With SEL0 selects SPI function, see table 1, 10kΩ pull-down to GND

FUNCTIONAL DESCRIPTION

OVERVIEW

The HI-8429 is comprised of 8 sensors, which may be individually configured for GND/Open or Supply/Open (also known as 28V/Open) sensing. Eight bits of the on-chip Configuration Register are used to set the sensor configuration. A high in the Configuration Register selects GND/Open and a low selects Supply/Open mode. A ninth bit in the Configuration Register is used to enable the chip's Built-In-Test (BIT) feature. The logical output from each sensor is latched into an eight-bit Data Register on the falling edge of the $\overline{CS}$ input.

An open drain interrupt pin ($\overline{INT}$) generates a 1μs low pulse when any of the sensor outputs change state. This frees up the micro-contoller from polling the register at frequent intervals.

Four internal 6 bit DACs provide the High and Low thresholds. Reading and writing to the registers is accomplished using a serial interface compatible with the industry-standard Serial Peripheral Interface (SPI) bus.

Figure 1 shows a simplified block diagram of the HI-8429.

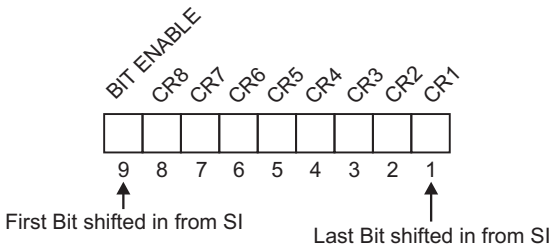
RESET AND INITIALIZATION

The HI-8429 includes an on-chip Power-On Reset (POR) circuit, which forces the SENSE inputs to a high-impedance state at power-up. Switches SW1 and SW2 (see Figure 1) are open. The inputs remain high-impedance until the Configuration Register is programmed, defining the GND/Open (SW1 closed / SW2 open), or Supply/Open (SW1 open / SW2 closed) for each sensor. The POR also resets all the registers to the all zeros default state.

The HI-8429 registers are designed to retain programmed logic states through VLOGIC power dips down to 1.5V ensuring reliable operation in noisy environments without the need to re-initialize the part.

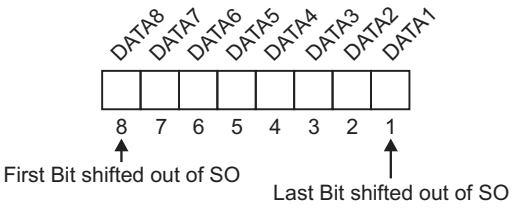
An external $\overline{MR}$ pin can also be used to reset the device. A low on this pin has the same effect as POR detailed above. During normal operation the $\overline{MR}$ pin should be left open or held high, if left open an internal 10kΩ pulls the input up to VLOGIC.

CONFIGURATION REGISTER



Configuration Register data is loaded serially from the SPI as described in the Serial Interface section below. The first bit of the Configuration Register (CR9) enables built-in-self test when set to a logic '1'. For normal sensing operation, CR9 should be zero. The next eight Configuration Register bits (CR8-1) set the sensing mode for each sensor. If set to a high, the sensor is GND/Open, and if programmed to a low, the sensor is Supply/Open. Data is shifted into the Configuration Register from the serial interface with bit CR9 first.

DATA REGISTER



The eight-bit Data Register captures the output state from the eight discrete sensors. Data is latched on the falling edge of $\overline{CS}$. The Data bits are read out from the chip over the serial interface. Sensor 8 data bit is output first at SO followed by the remaining seven sensor states. In either mode (GND/Open or Supply/Open), a logic one is output when the voltage at the sensor pin input is greater than the high threshold and a logic zero is output when the sensor voltage is lower than the low threshold.

Multiple HI-8429s may be daisy-chained together to allow a single SPI sequence to program configuration or capture data from several ICs in one operation.

SUPPLY/OPEN SENSING

When programmed as Supply/Open sensors, CRn is set to a logic 0. Referring to Figure 1, a switch in series with a diode is closed to provide a pull down to ground of 30kΩ. As with GND/Open, Supply/Open sensor levels are set by DAC thresholds VLO and VHI.

WETTING CURRENT

For the Supply/Open case the wetting current into the sense input is simply the current sunk by the effective 30kΩ to GND. For V_{SENSE} = 28V, I_{WET} is 1mA. See Figure 2.

GND/OPEN SENSING

For GND/Open sensing, the CRn bit is set to 1. Referring to the Block Diagram, Figure 1, this selection will connect a 12kΩ pull-up resistance through a diode to VDD. This resistance gives extra noise immunity for detecting the open state while providing contact wetting current. Open and Closed states are detected according to the threshold levels GLO and GHI programmed into the DAC Threshold Register, see Figures 14 - 17 for thresholds. When the SENSE input exceeds GHI, the output of the sensor goes high. The output of the sensor remains high until a voltage of less than GLO is detected at the SENSE input, representing a valid Ground state and causing the sensor output to go low. The Sensor will maintain a Ground detect state until the SENSE input becomes greater than GHI. The difference GHI - GLO represents the hysteresis which improves noise immunity and reduces output chattering.

WETTING CURRENT

In GND/Open mode a current is sourced from the SENSE pin when it is grounded and VDD is powered, see Figure 3.
This current called the “wetting current” serves to provide current through switches or relay contacts to prevent dry contacts and improve switch contact reliability.

BUILT-IN TEST

Writing a high in Control Register bit 9 puts the HI-8429 into the Built-In Test (BIT) mode. In this mode setting a CRn bit high for a particular sensor forces that comparator input high. A zero in CRn forces the comparator input low. To verify correct operation, the user must read from the Data Register and compare this with the value written to CR1-8.

NOTE: Certain flight applications require periodic sensor testing during flight. To ensure seamless transition between BIT mode and normal operation mode, the following steps should be followed:

1) The host should read and record the Configuration Register value for normal mode operation.
2) The host should read and record the last value of the Data Register before enabling BIT mode (CR9 = 1).
3) Following test completion, **but while still in BIT mode**, the host should set the sensor outputs to their pre-test values by writing bits CR8 - CR1 with their corresponding Data Register pre-test values recorded in step 2) above.
4) Normal operation (CR9 = 0) is restored by writing the Configuration Register with its pre-test value stored in step 1).

DEBOUNCE

When the input DBNC is high, a debounce circuit on the sensor outputs is enabled (see Figure 1). The comparator outputs are sampled every 60ms, the state of the sensor register bit is changed only when two consecutive samples are identical. When debounce is enabled there will be approximately 60ms delay before the sense data register is updated.

DAC THRESHOLD REGISTER

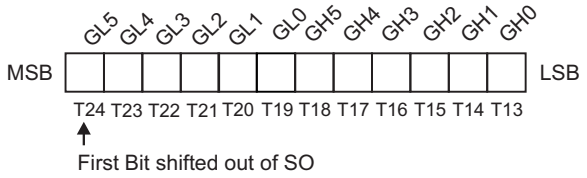
The 24-bits [T24:1] in the DAC Register program the sensor threshold levels for the eight discrete sensors. There are four 6 bit DACs:

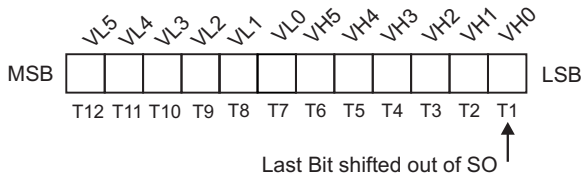
GL5:0 GND/Open Low Threshold
GH5:0 GND/Open High Threshold
VL5:0 Supply/Open Low Threshold
VH5:0 Supply/Open High Threshold

The thresholds are programmed according to the two formula below, for GND/Open and Supply/Open modes respecitvely:

Vthresh(G/O) = VDD x (0.126 + D/91.6) Volts
Vthresh(S/O) = VDD x (0.144 + D/98.9) Volts
D is a value (0 to 63) programmed into the DAC

For further details see example DAC threshold programming on page 12.





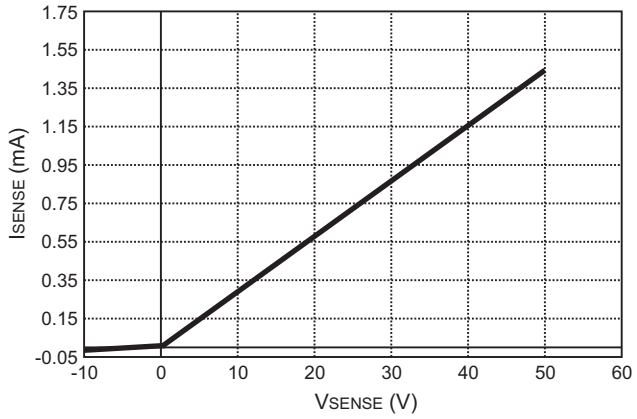


Figure 2.
Supply/Open Mode SENSE Input IV Characteristic (VDD = 15V)

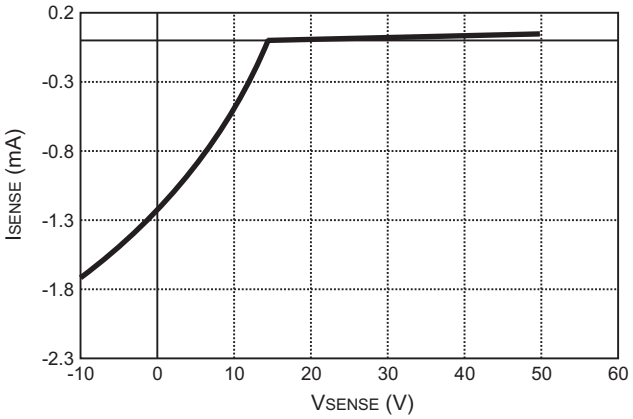


Figure 3.
GND/Open Mode SENSE Input IV Characteristic (VDD = 15V)

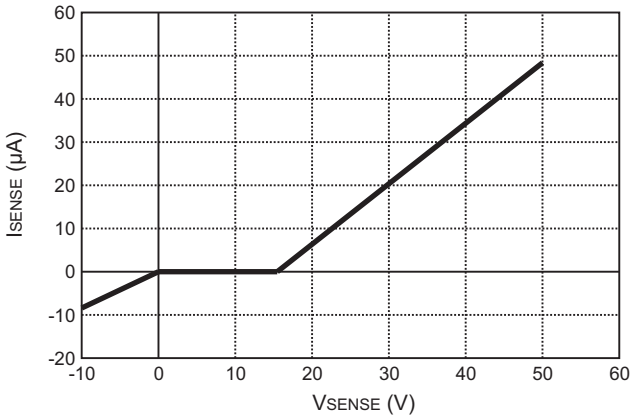


Figure 4.
Hi-Z SENSE Input IV Characteristic (VDD = 15V)

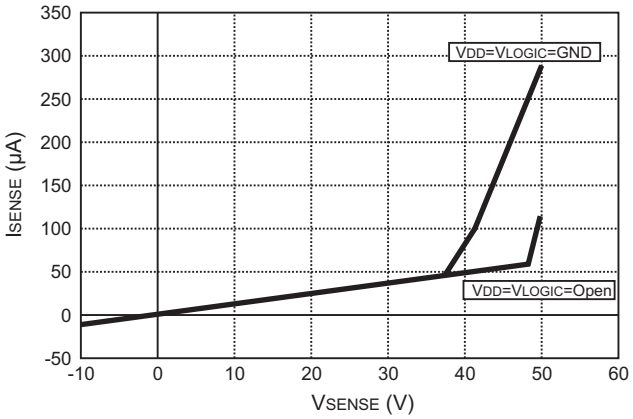


Figure 5.
Power-Off SENSE Input IV Characteristics

FUNCTIONAL DESCRIPTION (cont.)

SERIAL PERIPHERAL INTERFACE

The HI-8429 uses a SPI (Serial Peripheral Interface) for host access to the internal Configuration, DAC and Data Registers which program the sensor mode, threshold levels and store sensor status. Host serial communication is enabled through the active low, Chip Select ($\overline{CS}$) pin, and is accessed via a four-wire interface consisting of Serial Data Input (SI) from the host, Serial Data Output (SO) to the host, the Serial Clock (SCK) and the $\overline{CS}$. All read / write cycles are completely self-timed.

The SPI protocol specifies master and slave operation; the HI-8429 operates as a SPI slave.

The SPI protocol defines two parameters, CPOL (clock polarity) and CPHA (clock phase). The possible CPOL-CPHA combinations define four possible “SPI Modes”. The HI-8429 operation is based on Mode 0 (CPHA = 0, CPOL = 0), where input data for each device is clocked on the rising edge of SCK, but data is also clocked out on the positive edge, see fig 14.

As seen in SPI timing diagrams Figures 6-10, SPI Mode 0 holds SCK in the low state when idle. The SPI bus transfers serial data in multiples of 8, 9 or 24 bits, depending on the type of data and number of devices. Once $\overline{CS}$ is asserted, the rising edge of SCK shifts the input data into the slave devices, starting with each byte's most-significant bit. A rising edge on $\overline{CS}$ completes the serial transfer and re-initializes the HI-8429 SPI for the next transfer.

To improve immunity from noise on $\overline{CS}$, a write will only occur after 8 SCKs are received. However if $\overline{CS}$ goes high after this and before a word transfer is complete, the incomplete byte will be latched into the device.

Both master and slave simultaneously send and receive serial data (full duplex), per Figure 6. The HI-8429 maintains high impedance on the SO output whenever $\overline{CS}$ is high. The maximum SCK frequency is 10MHz. The HI-8429 logic is fully static and therefore there is no minimum SCK speed.

CONFIGURATION REGISTER SPI TRANSFERS

On power up or after a Hardware Reset all the sense input circuits are disabled by default, they only become enabled after a write to the configuration register. SEL0 and SEL1 are held low for sensor configuration changes, see table 1. Write / read timing is identical to Data Register transfers, except with the added complication that the Configuration Register is nine bits rather than eight bits. Care should be taken to ensure correct bit alignment when shifting data into and out of the register, particularly when daisy-chaining multiple devices. Figures 6 - 10 show examples of SPI data transfers, including a daisy-chained transfer.

SEL1	SEL0	SPI Function
0	0	Read/Write to Configuration Register (9bits)
1	0	Read/Write to Threshold Register (24 bits)
X	1	Read Sensor Data (8 bits)

Table 1. SPI Function Table

THRESHOLD REGISTER SPI TRANSFERS

To program the DAC thresholds, the SEL1 pin is held high and SEL0 held low, see table 1. Reading and Writing to threshold registers uses the same sequence and requires transferring 24 bits (four sets of 6 bits) of continuous data, see Figure 9.

Thresholds are set by adjusting the DAC settings, according to Table 2. As with the other registers, data can be daisy chained between multiple series SPI coupled devices (see Figure 12), an extra 24 clock cycles are required for each extra device.

SENSEn	Config Bit	Bit #
< GLO	1 (GND/Open)	24:19
Open or > GHI	1 (GND/Open)	18:13
Open or < VLO	0 (Supply/Open)	12:7
> VHI	0 (Supply/Open)	6-1

Table 2. Sensor Threshold Table

FUNCTIONAL DESCRIPTION (cont.)

DATA REGISTER SPI TRANSFERS

The SPI data path is selected by the control inputs SEL1:0, according to the SPI function table 1. To read sensor data the SEL0 pin should be high.

When $\overline{CS}$ goes low, the output of each sensor is latched into the Data Register and DR8 is output at SO. The next 7 rising edges of SCK shift out Data Register bits 7 through 1. Simultaneously, data presented at SI is shifted into the Data Register, DR8 is written on the first rising edge of SCK and DR1 on the eighth SCK rising edge.

The eighth SCK edge also causes the new DR8 value to be output at SO (see Figure 8). This data transfer method allows multiple HI-8429 devices to be "daisy-chained" such that the Data Registers from each device are cascaded to form a single shift register. Figure 12 shows a typical configuration of three daisy-chained HI-8429s to form a 24-input sensor array. Note that when reading from more than one device, $\overline{CS}$ must remain low throughout the data read sequence. Taking $\overline{CS}$ high and then low again between eight-bit reads will cause the sensor data to be re-latched into the Data Registers, overwriting data shifted in from earlier HI-8429s in the chain. See Figure 10 for an example of a 24-bit Data Register read operation.

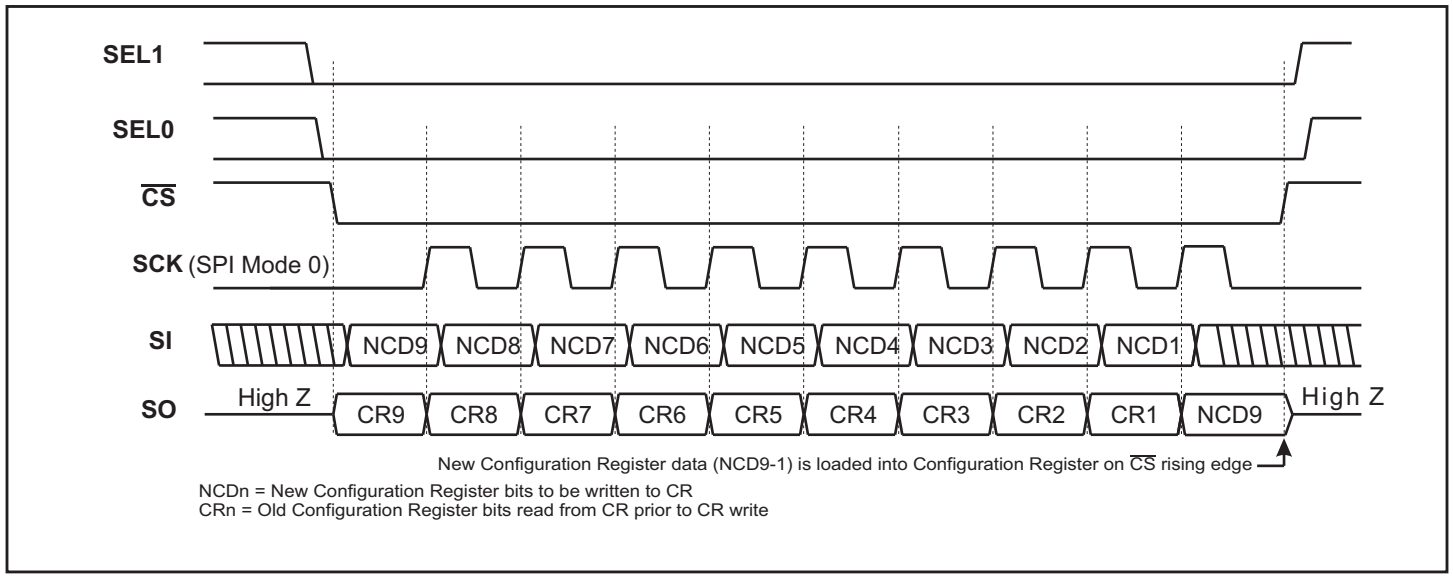


Figure 6. Nine-bit Configuration Register Write Example

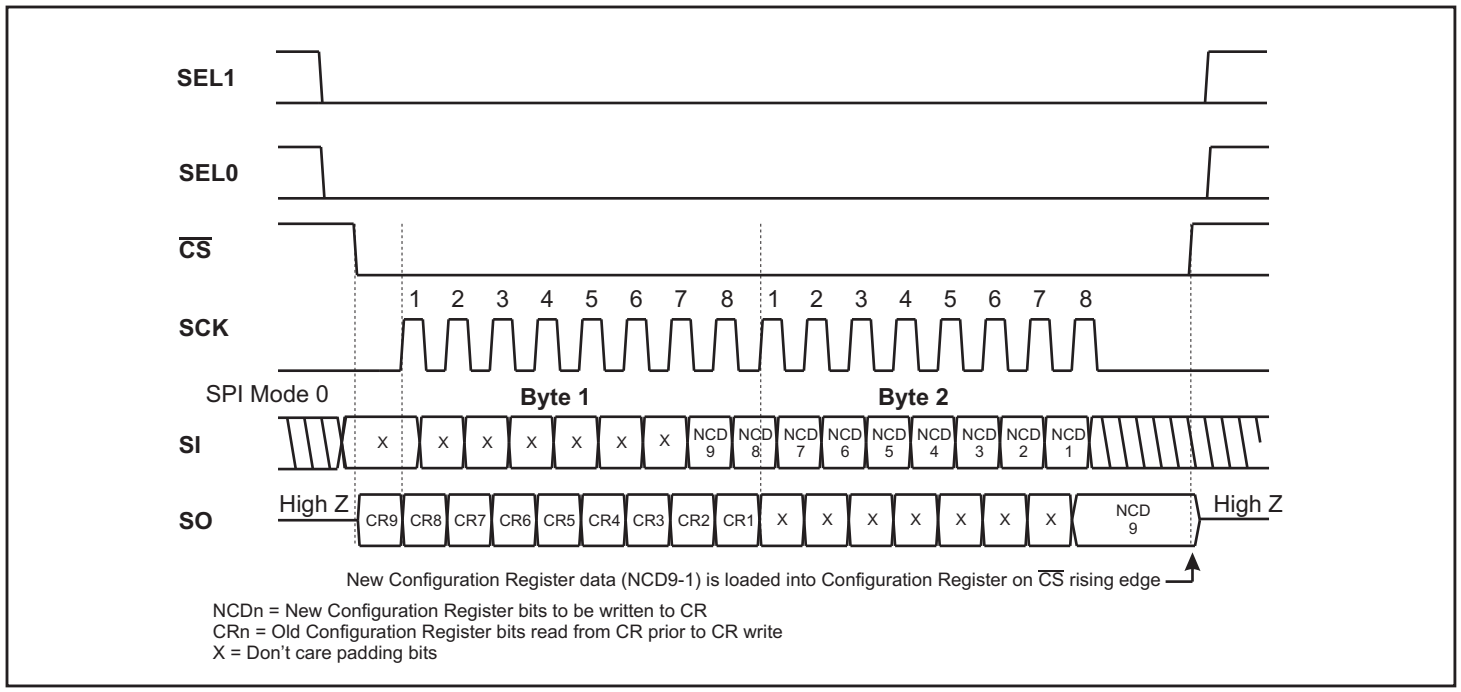


Figure 7. 9bit Configuration Register Write (padded to make 2-Bytes) Example

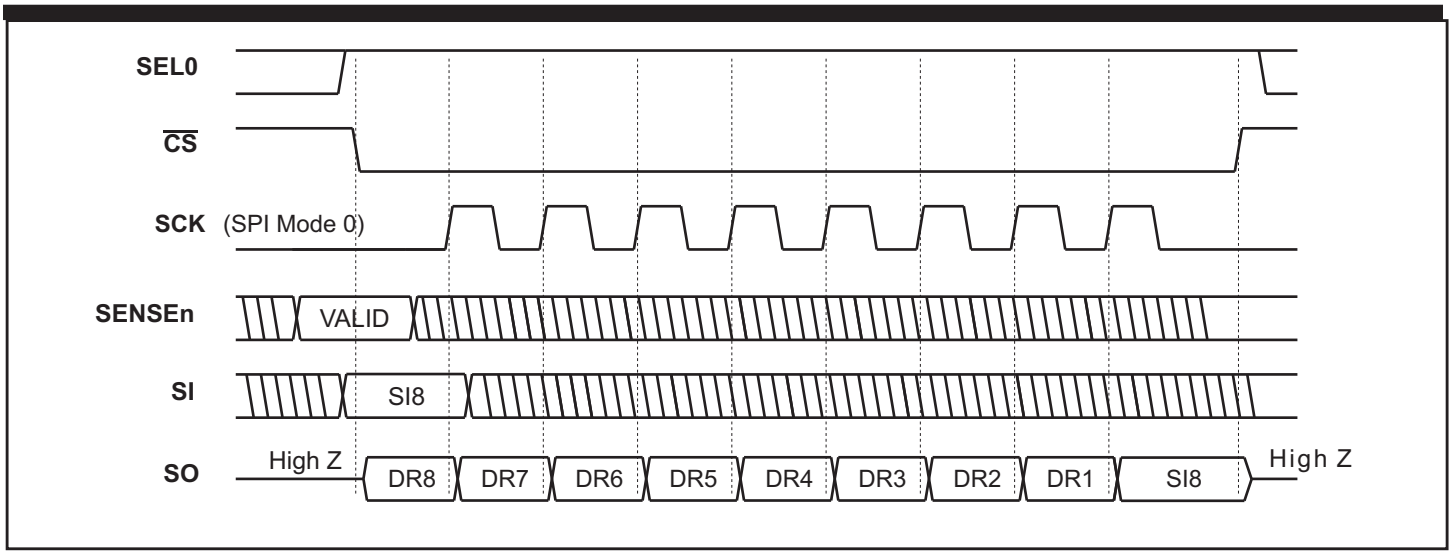


Figure 8. Single-Byte Data Register Read

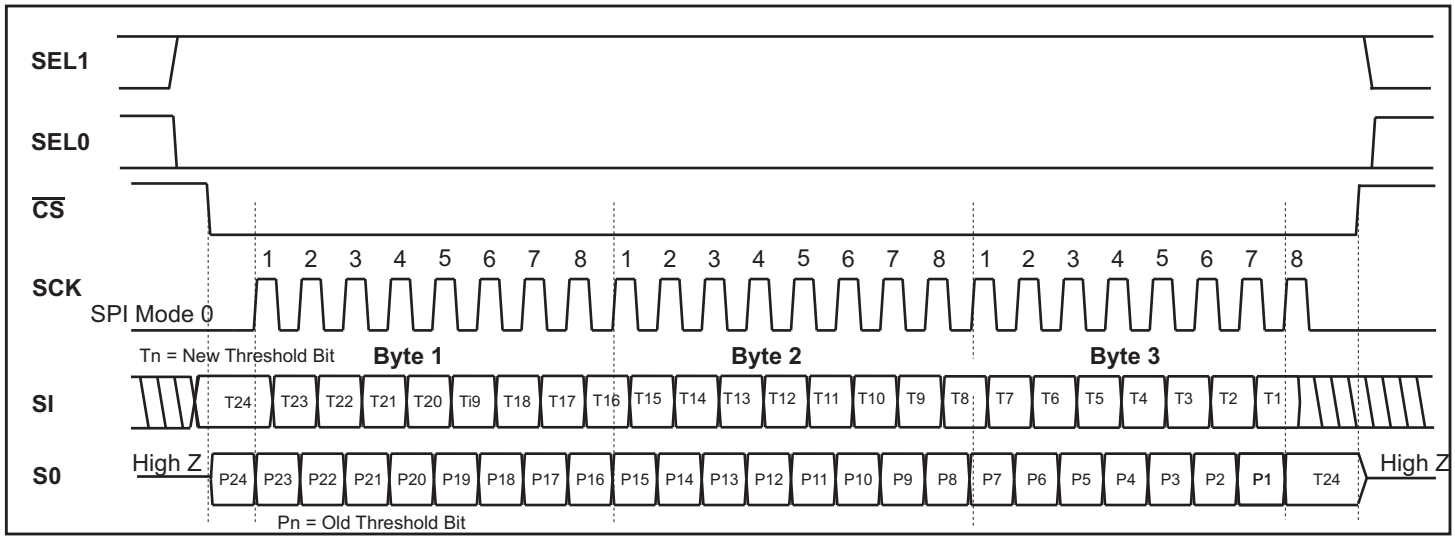


Figure 9. 24-Bit SPI Write and Read Threshold Example

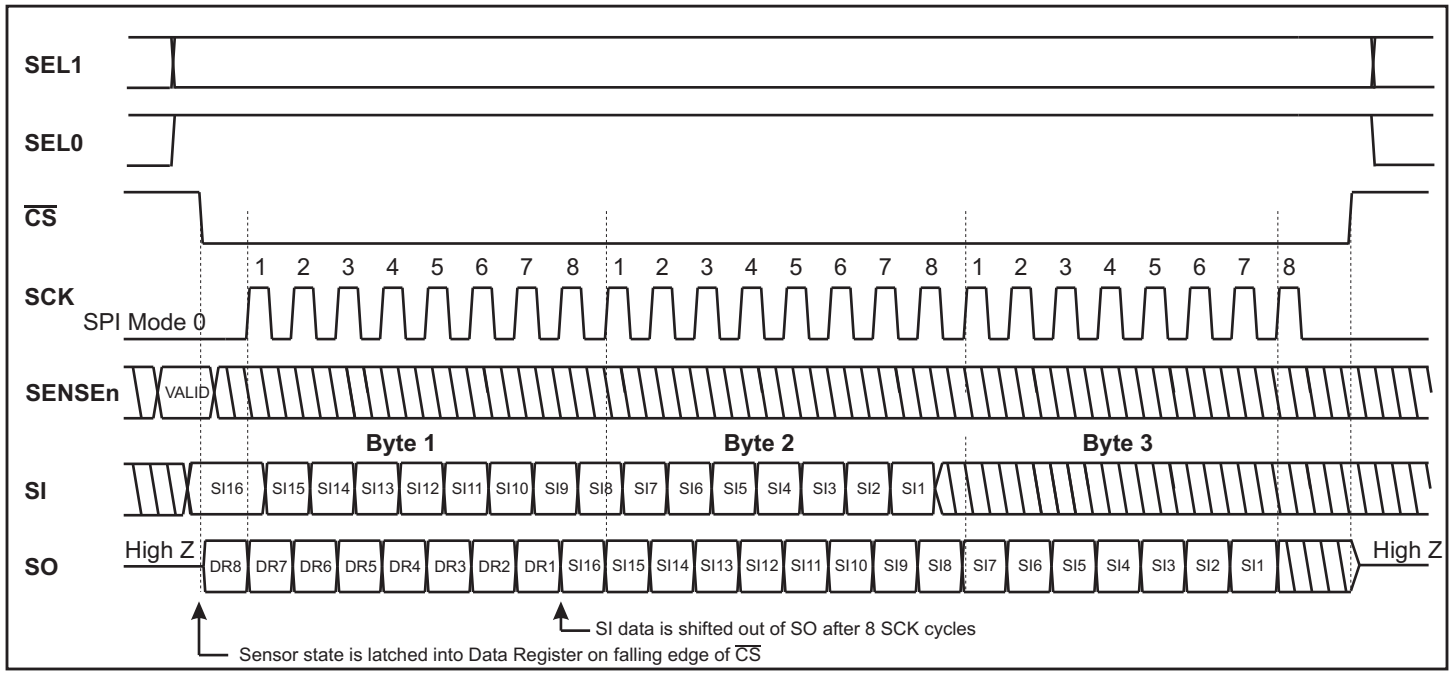


FIGURE 10. 3-Byte SPI Daisy-Chain Data Register Read Example

FUNCTIONAL DESCRIPTION (cont.)

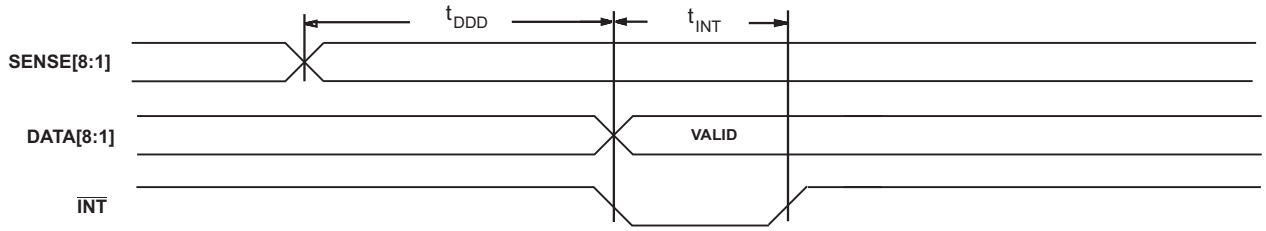


Figure 11. Debounce Data Delay

INT FUNCTION

The $\overline{INT}$ output will produce an output whenever a sensor input changes. There will be a delay before the interrupt is produced and data updated, as shown in Figure 11. This delay will depend upon the setting of DNBC, when DNBC is high the delay will be much longer due to the delay through the debounce circuitry. If the $\overline{INT}$ signal is used and mechanical contacts are also used for the sense circuit, it is recommended to enable debouce.

24 Channel Sensor Application using HI-8429

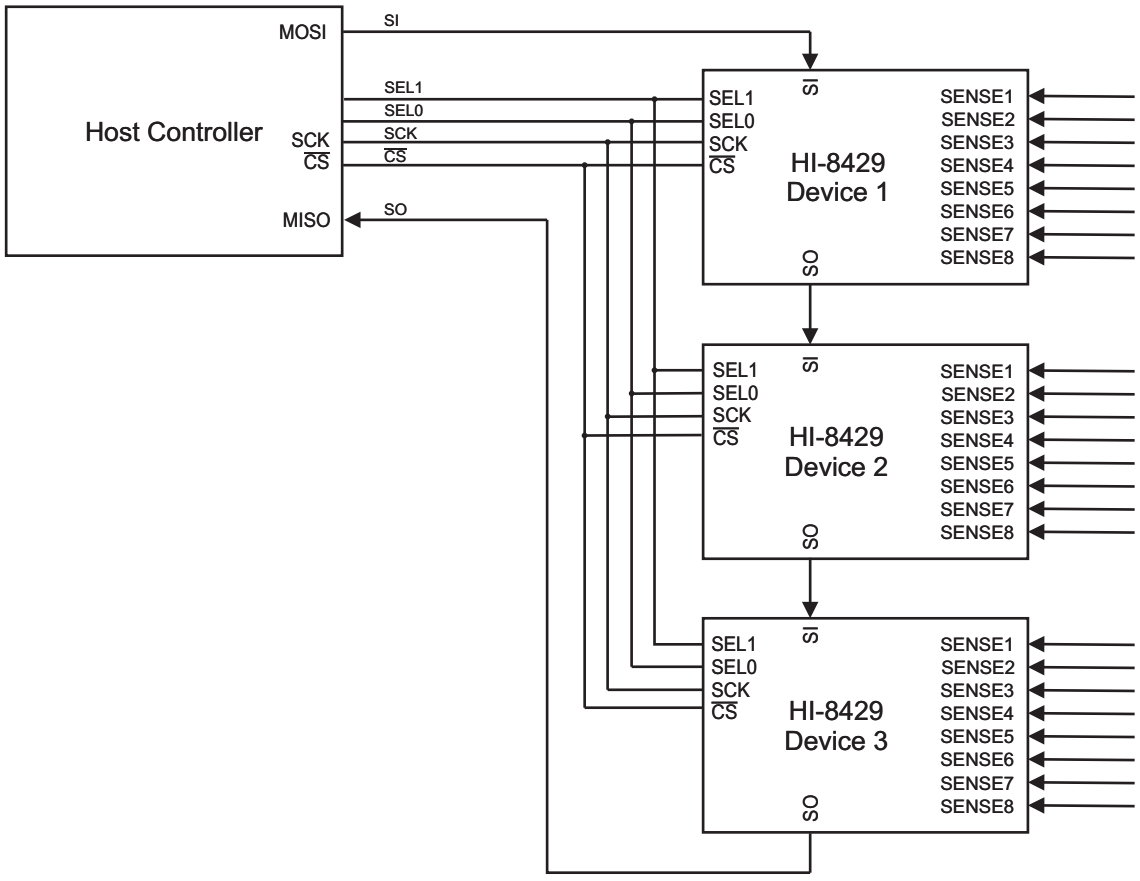


Figure 12. Multiple Chip "Daisy-Chain" Connection

FUNCTIONAL DESCRIPTION (cont.)

LIGHTNING PROTECTION

All SENSEn inputs are protected to RTCA/DO-160G, Section 22, Categories A3 and B3, Waveforms 3, 4, 5A, 5B with no external components. Table 3 and Figure 13 give values and waveforms. Higher levels of lightning protection can be implemented using a series resistor and a TVS, see Application Note AN-305 for recommendations.

Level	Waveforms			
	3/3	4/1	5A/5A	5B/5B
	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)
3	600/24	300/60	300/300	300/300

Table 3. Waveform Peak Amplitudes

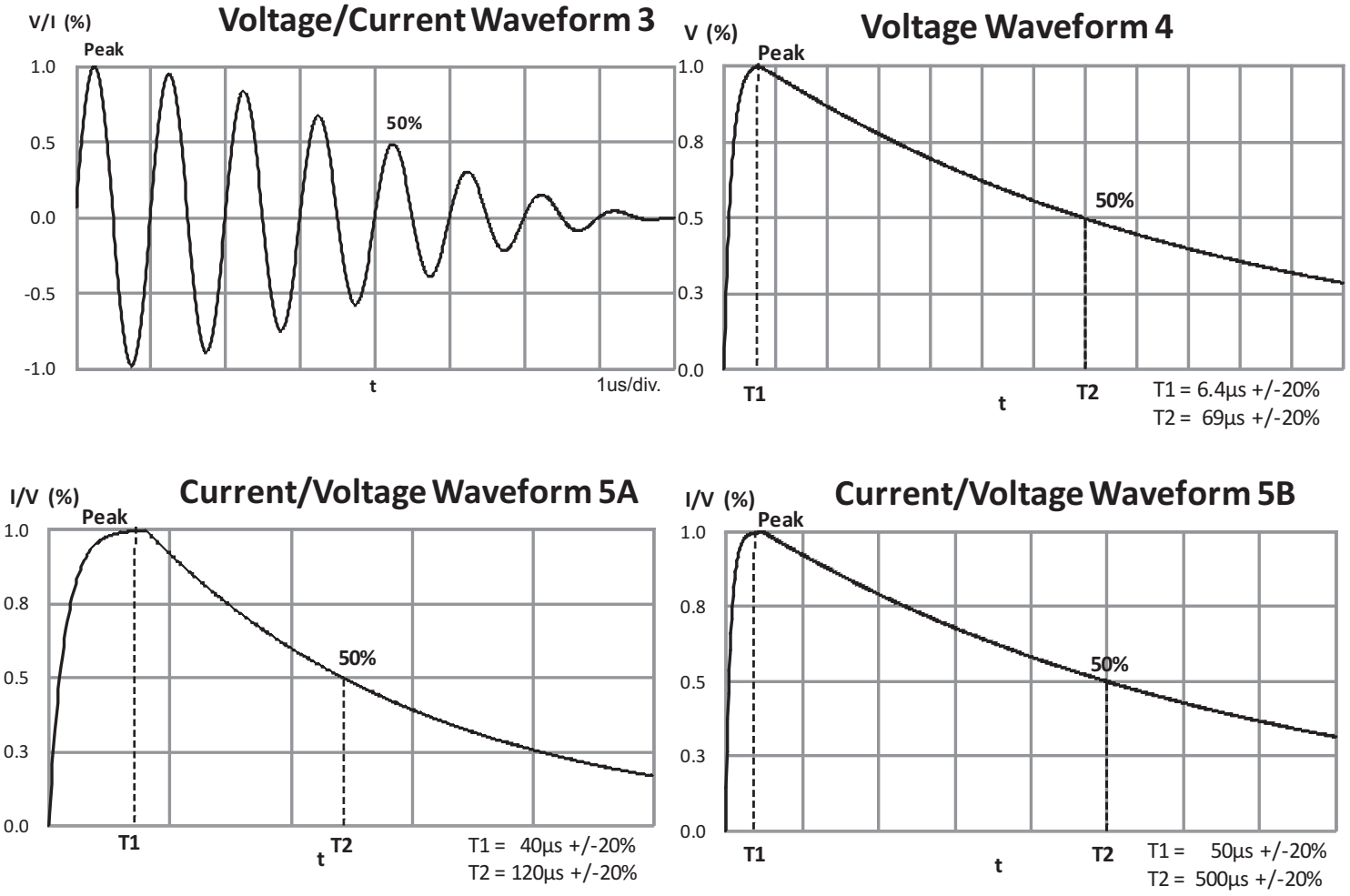


Figure 13. Lightning Waveforms

SETTING SENSOR THRESHOLDS BY PROGRAMMING DAC CODES

EXAMPLE

Assume the supply voltage is VDD = 15V and the system threshold requirements are:

GND/Open sensors with GLO < 4.5V and GHI > 10.5V.
Supply/Open sensors with VLO < 6V and VHI > 12V.

For the GND/Open thresholds, use the curves in Figure 15 for VDD = 15V. To guarantee a minimum 4.5V threshold, use the 15V minimum curve. At 4.5V, the DAC code reading is 19. This is the GLO DAC setting . Similarly for GHI, use the 15V maximum curve to guarantee a maximum 10.5V threshold. The corresponding value from the curve in this case is 47. Converting these values to hexadecimal, we get 0x13 and 0x2F respectively.

Similarly for the Supply/Open thresholds, use the curves in Figure 17 for VDD = 15V. To guarantee a minimum 6.0V threshold, use the 15V minimum curve. At 6.0V, the DAC code reading is 30. This is the VLO DAC setting. Similarly for VHI, use the 15V maximum curve to guarantee a maximum 12.0V threshold. The corresponding value from the curve in this case is 58. Converting these values to hexadecimal, we get 0x1E and 0x3A respectively.

The four DACs are programmed together by writing one 24-bit word to the DAC Threshold Register (see Functional Description section). For the above example, the values 0x13 0x2F 0x1E 0x3A are converted to the binary value 010011 101111 011110 111010 and sent to the DAC Threshold Register, MSB first.

GND/OPEN SENSE THRESHOLDS VERSUS DAC CODE

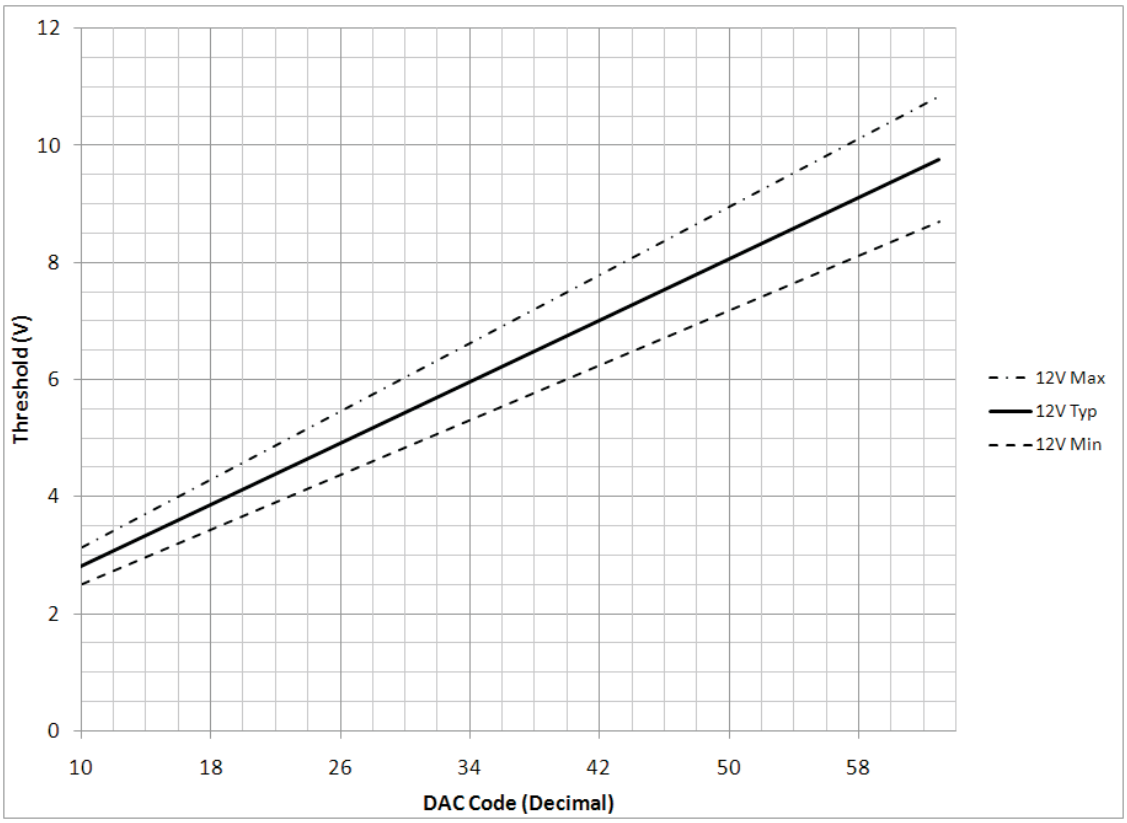


Figure 14. GND/Open sense thresholds versus DAC code for VDD = 12V

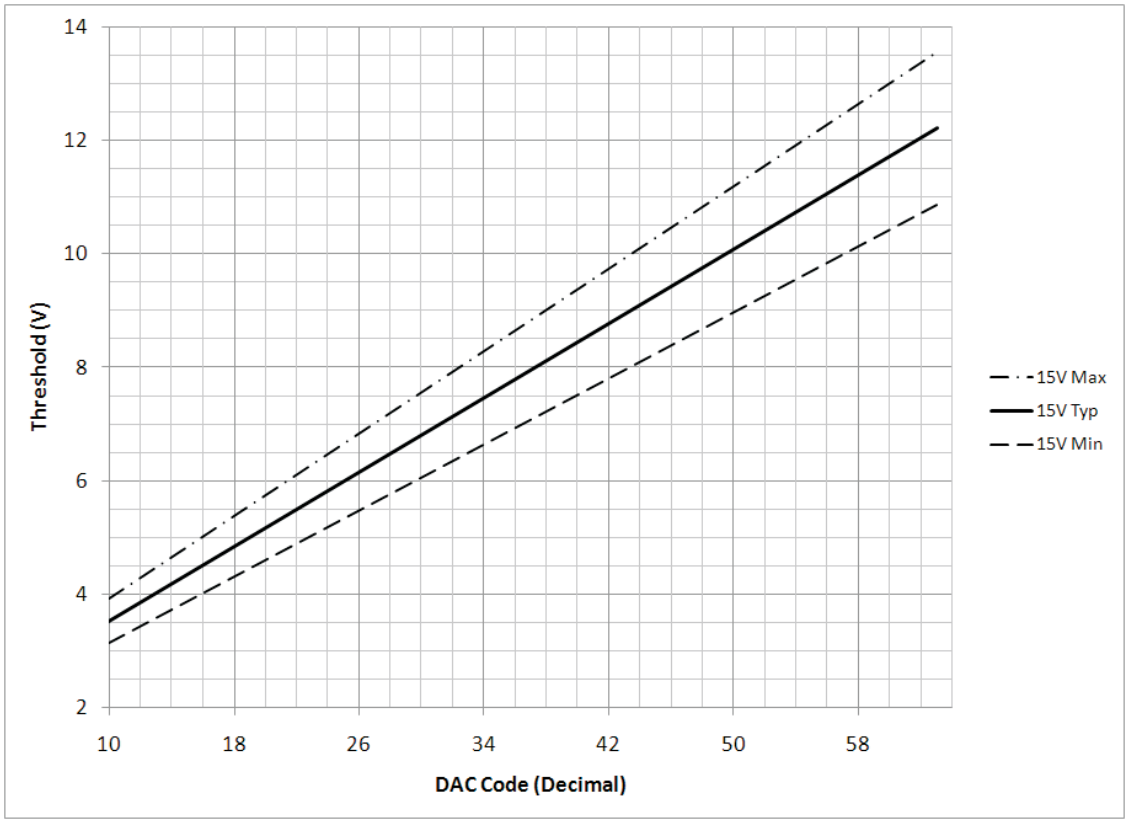


Figure 15. GND/Open sense thresholds versus DAC code for VDD = 15V

SUPPLY/OPEN SENSE THRESHOLDS VERSUS DAC CODE

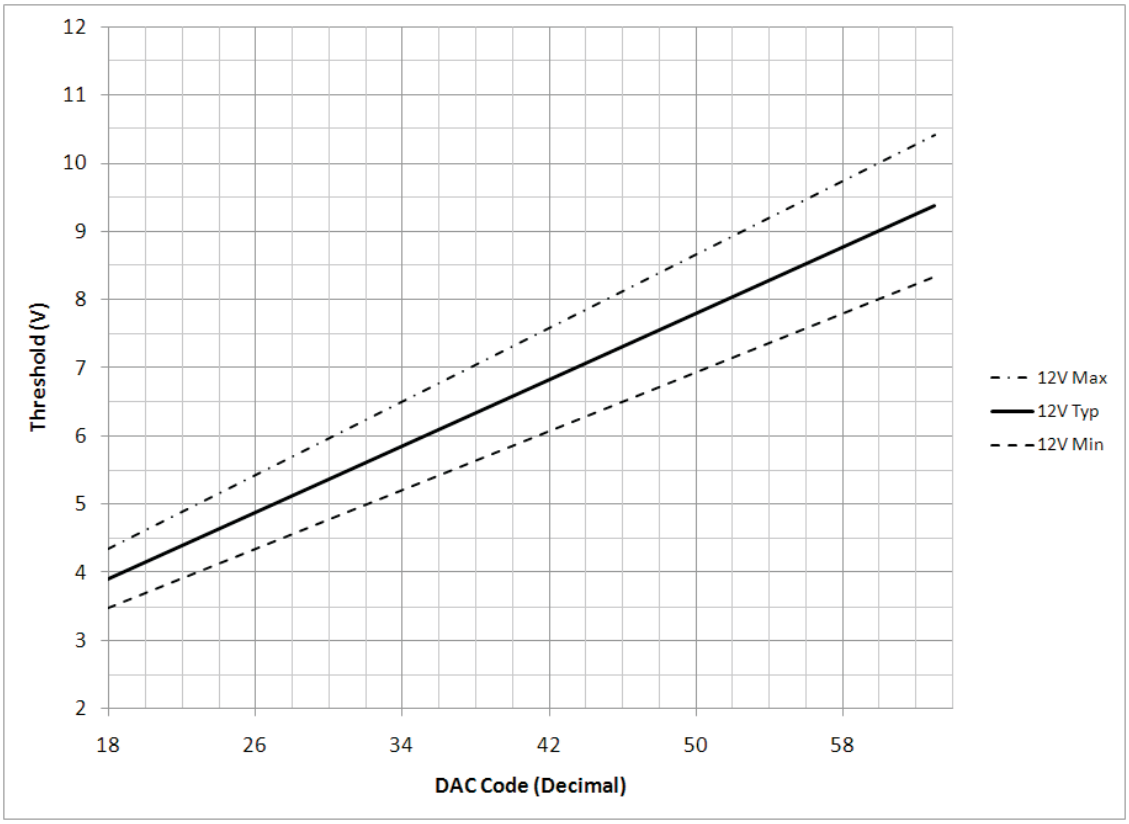


Figure 16. Supply/Open sense thresholds versus DAC code for VDD = 12V

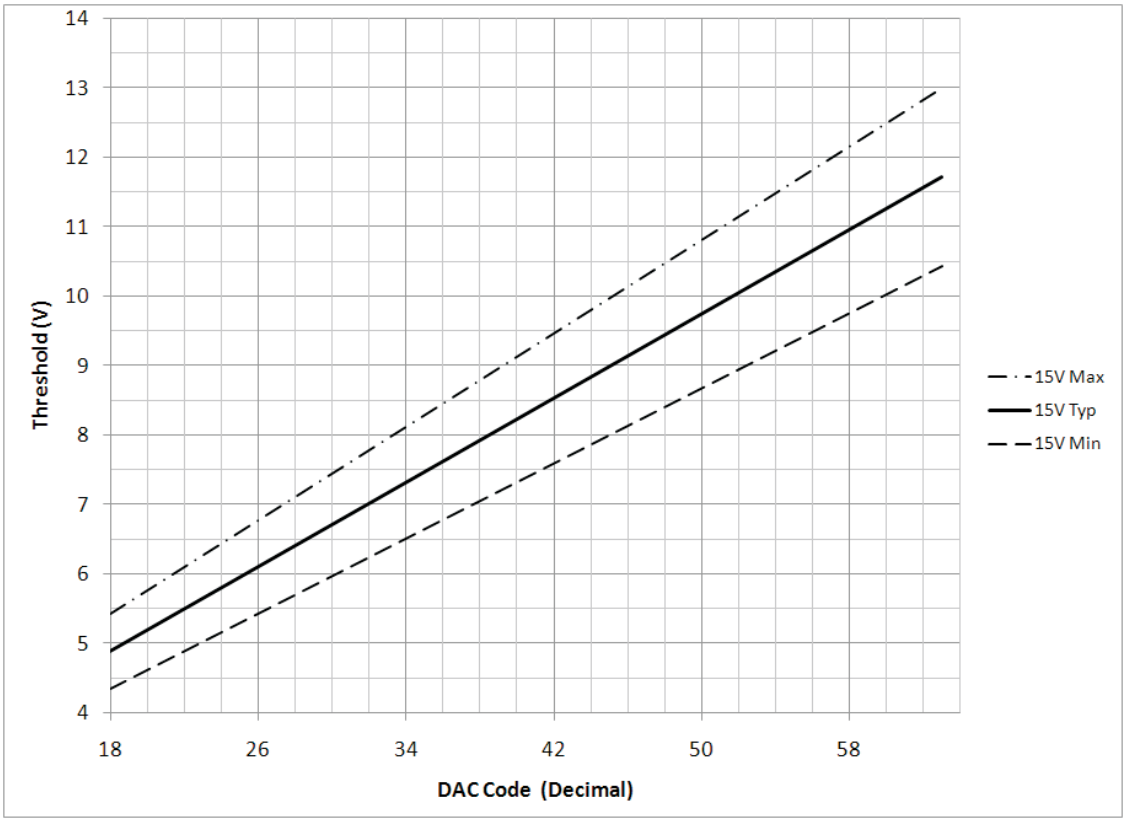


Figure 17. Supply/Open sense thresholds versus DAC code for VDD = 15V

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground	
Digital Supply Voltage (VLOGIC)	-0.3V to +5V
Analog Supply Voltage (VDD)	-0.3V to +18V
Logic Input Voltage Range	-0.3V to VLOGIC+0.3V
Discrete Input Voltage Range (DC)	-80V to +80V
(AC, 60 - 400Hz)	115Vrms
Continuous Power Dissipation (TA=+125°C)	1.7W
Solder Temperature (reflow)	260°C
Junction Temperature	175°C
Storage Temperature	-65°C to -150°C

RTCA/DO-160G, Section 22 pin injection	
Waveform	Voc/Isc
3	750V/30A
4	500V/100A
5A	500V/500A
5B	500V/500A

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	
VLOGIC	3.13V to 3.47V
VDD	11.4V to 15.75V
Digital Inputs	0 to VLOGIC
SENSE inputs	-4.0V to 49V
Operating Temperature Range	
Industrial Screening	-40°C to +85°C
Hi-Temp Screening	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

D.C. ELECTRICAL CHARACTERISTICS

V_{LOGIC} = 3.3V +/- 5%, V_{DD} = 12.0V +/-5% to 15V +/-5%, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYM	CONDITION	MIN	TYP	MAX	UNIT
Logic Inputs / Outputs						
High level input voltage	V_{IH}	V_{LOGIC} = 3.3V	2.0			V
Low level input voltage	V_{IL}	V_{LOGIC} = 3.3V			0.8	V
Input hysteresis voltage, SCK input	V_{CHYS}	Note 1.	50			mV
High level output voltage	V_{OH}	I_{OUT} = -20 µA I_{OUT} = -4 mA, V_{LOGIC} = 3.0V	V_{LOGIC} -0.1 2.4			V V
Low level output voltage	V_{OL}	I_{OUT} = 20 µA I_{OUT} = 4 mA, VLOGIC = 3.0V			0.1 0.4	V V
Input leakage current (no pull-ups or pull-downs)	I_{IN}	V_{IN} = V_{LOGIC} or Ground	-10		+10	µA
Input leakage current ($\overline{MR}$, DNBC, and SEL1 pins, 10kΩ pull-up / pull-downs)	I_{INP}	V_{IN} = V_{LOGIC} or Ground		335		µA
Tri-state leakage current, SO output	I_{OZ}	V_{OUT} = V_{LOGIC} or Ground	-10		+10	µA
SENSE Inputs, Configured as Ground / Open (internal pull-up).						
High level SENSE pin to Ground resistor	R_{IH}	Resistor from SENSE to Ground to guaranteed High input condition	50			kΩ
High level input current	I_{GHI}	V_{GHI} = 28V, VDD = 15V V_{GHI} = 49V, VDD = 15V		17 45	100 250	µA uA
Low level input current	I_{GLO}	V_{GLO} = 0V, V_{DD} = 15V	-0.8	-1.0	-1.8	mA
Low level SENSE pin to Ground resistor	R_{IL}	Resistor from SENSE to Ground to guaranteed Low input condition			500	Ω
Minimum Hysteresis (VGHI - VGLO)	HYS_{GO}		4 DAC LSBs			
SENSE Inputs, Configured as Supply / Open (internal pull-down).						
High level input current	I_{SHI}	V_{SHI} = 28V, V_{DD} = 15V	0.6	0.8	1.35	mA
Low level input current	I_{SLO}	V_{SLO} = 1V, V_{DD} = 15V			50	µA
Minimum Hysteresis (VSHI - VSLO)	HYS_{SO}		4 DAC LSBs			
Power Supply						
Logic supply current	I_{LOGIC}	V_{IN} = V_{LOGIC} or Ground, SENSE pins open		1.8	3.0	mA
Analog supply current	I_{DD}	V_{IN} = V_{LOGIC} or Ground SENSE pins open SENSE pins = Ground		 15 23	 24 33	 mA mA

Note 1. Guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS

V_{LOGIC} = 3.3V +/- 5%, V_{DD} = 12.0V +/-5% to 15V +/-5%, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYM	CONDITION	MIN	TYP	MAX	UNIT
SCK Frequency	f_{MAX}	50% Duty Cycle	0.1		10	MHz
SCK Pulse Width	t_W		50			ns
Set-up Time, SCK to $\overline{CS}$ low	t_{SU1}		30			ns
Hold Time, $\overline{CS}$ low to SCK	t_{H1}		25			ns
Set-up Time, SENSE valid to $\overline{CS}$ low	t_{SU2}		500			ns
Hold Time, $\overline{CS}$ low to SENSE not valid	t_{H2}		15			µs
Set-up Time, SI to SCK rising	t_{SU3}		25			ns
Hold Time, SCK rising to SI not valid	t_{H3}		25			ns
Set-up Time, SEL valid to $\overline{CS}$ low	t_{SU4}		30			ns
Hold Time, $\overline{CS}$ high to SEL not valid	t_{H4}		25			ns
Propagation Delay, $\overline{CS}$ low to SO valid	t_{P1}	SO loaded with 50pF to Ground			105	ns
Propagation Delay, SCK rising to SO valid	t_{P2}	SO loaded with 50pF to Ground			90	ns
Propagation Delay, $\overline{CS}$ rising to SO Hi-Z	t_{P3}	SO loaded with 50pF to Ground			80	ns
$\overline{CS}$ recovery time	t_{CSR}		20			ns
Logic Input Capacitance (SCK, $\overline{CS}$, SI)	C_{IN}	Guaranteed but not Tested			10	pF
Logic output capacitance (SO Hi-Z)	C_{OUT}	Guaranteed but not Tested			15	pF
$\overline{MR}$ Pulse Width	t_{MR}		1			µs
$\overline{INT}$ Pulse Width	INT			1		µs
Data and Interrupt delay (DNBC = Low)	t_{SD}				4	us
Data and Interrupt delay (DNBC = High)	t_{SD}				100	ms
Time Between Debounce Samples	t_{DB}		25			ms

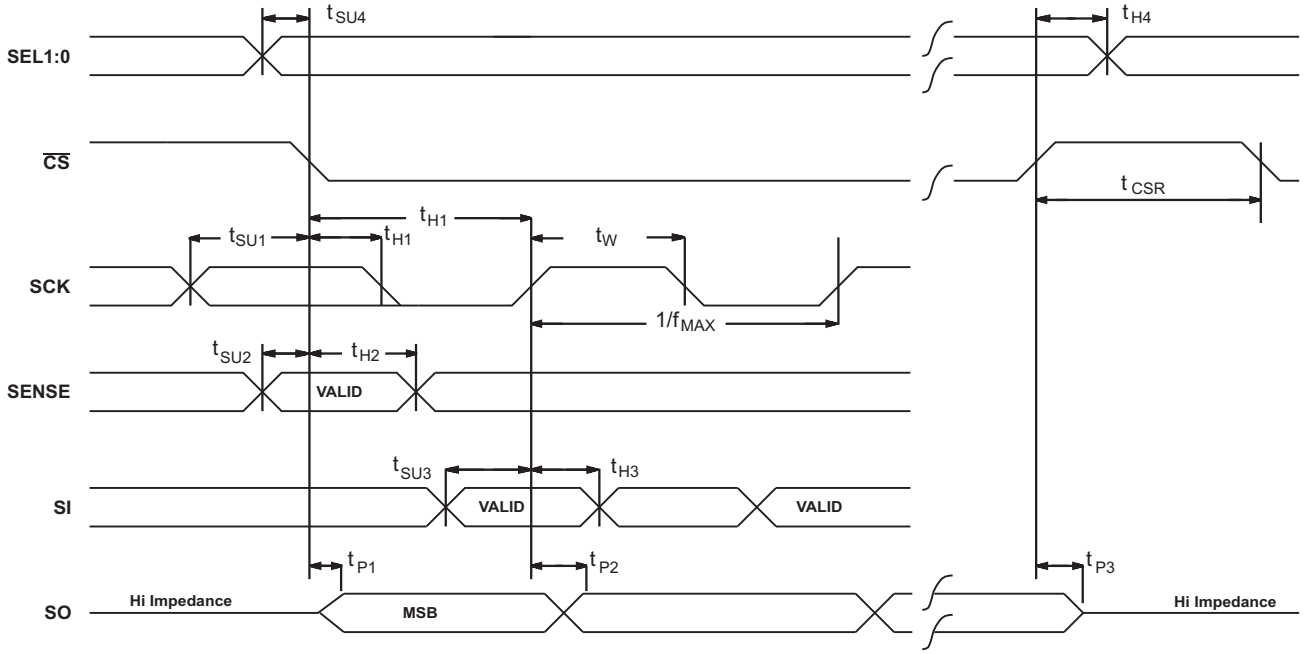
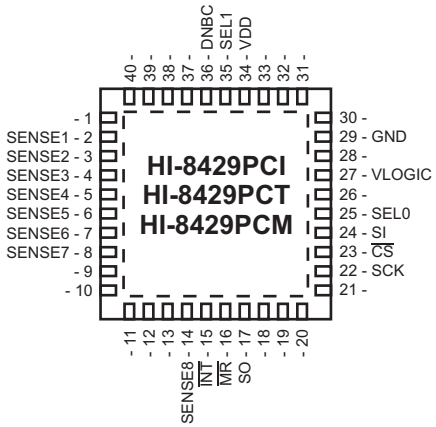


Figure 18. Switching Waveforms

Alternative Package Configurations (40-pin QFN)



ORDERING INFORMATION

HI - 8429xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn /Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
8429PS	20 PIN PLASTIC THERMALLY ENHANCED SOIC, WB (20HWE)
8429PC	40 PIN PLASTIC CHIP-SCALE, QFN (40PCS)

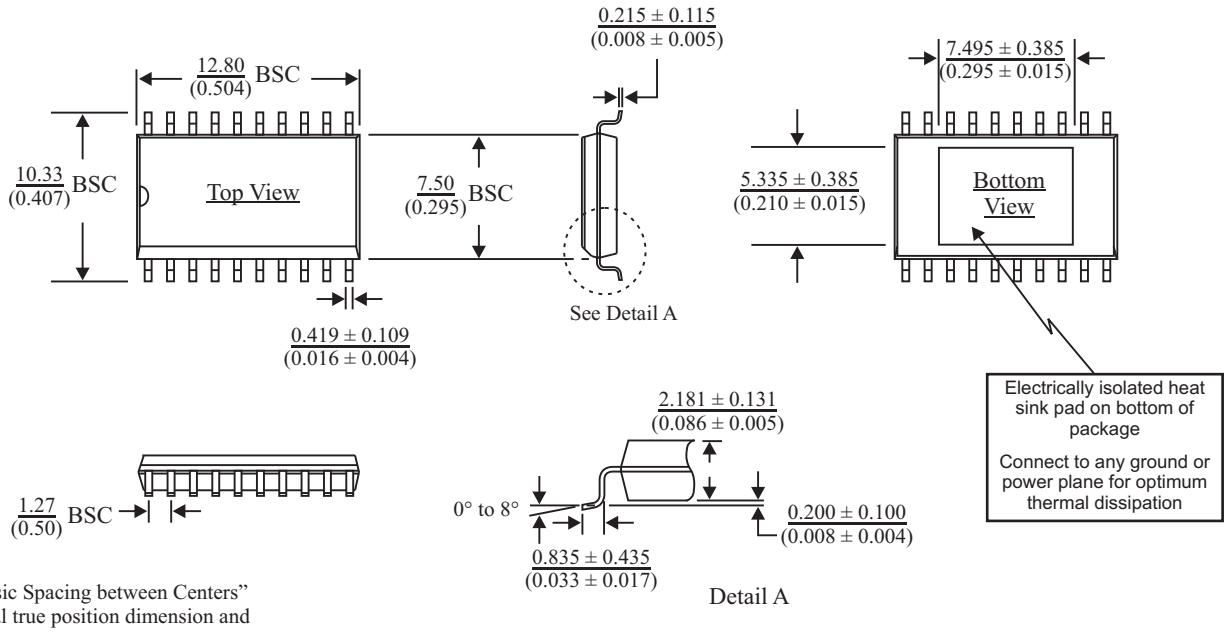
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8429	New	10/15/14	Initial Release.
	A	11/13/14	Change VDD range to (12V +/-5% to 15V +/-5%. Update DAC curves.
	B	02/19/15	Add 40-pin QFN package option.
	C	11/03/15	Add Note to clarify how to change between Test mode and normal operation mode.
	D	06/01/17	Add peak lightning I/V capability to Absolute Maximum Ratings table.

20-PIN PLASTIC SMALL OUTLINE (ESOIC) - WB
(Wide Body, Thermally Enhanced)

millimeters (inches)

Package Type: 20HWE

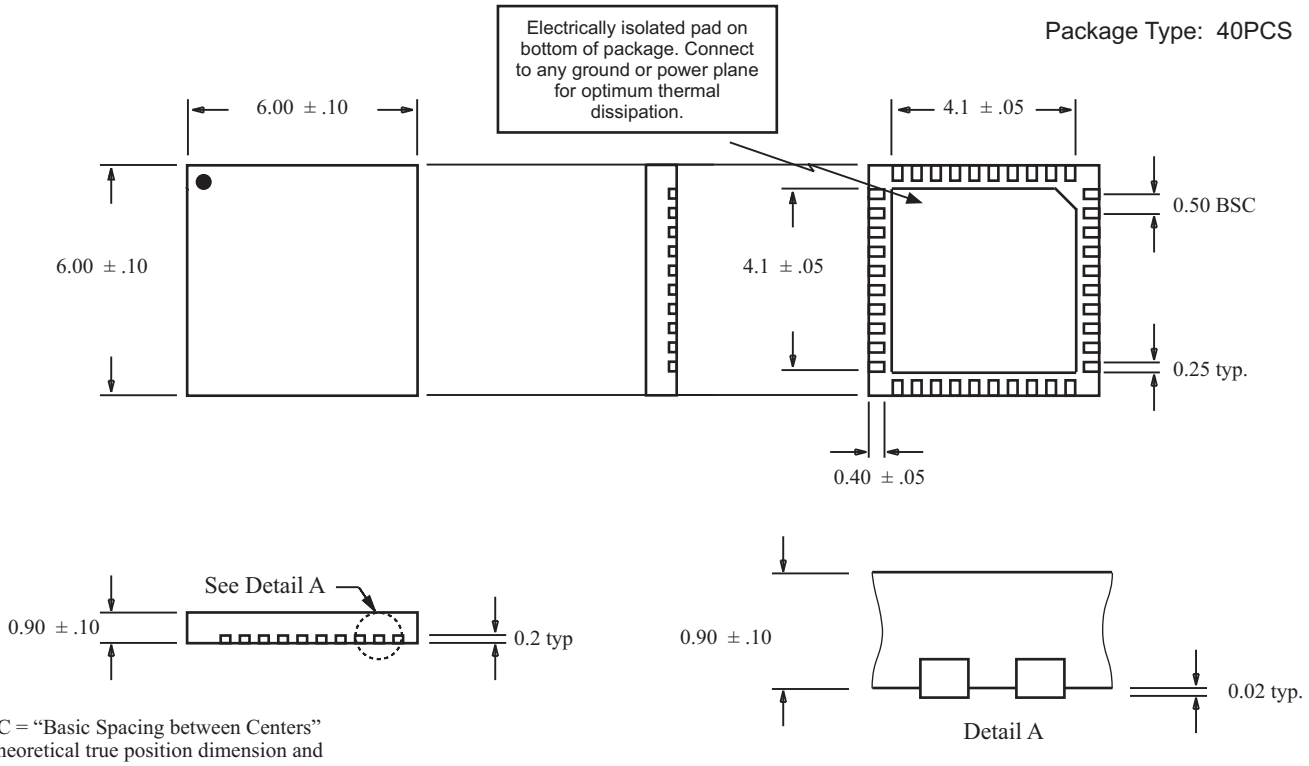


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

40-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters

Package Type: 40PCS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)