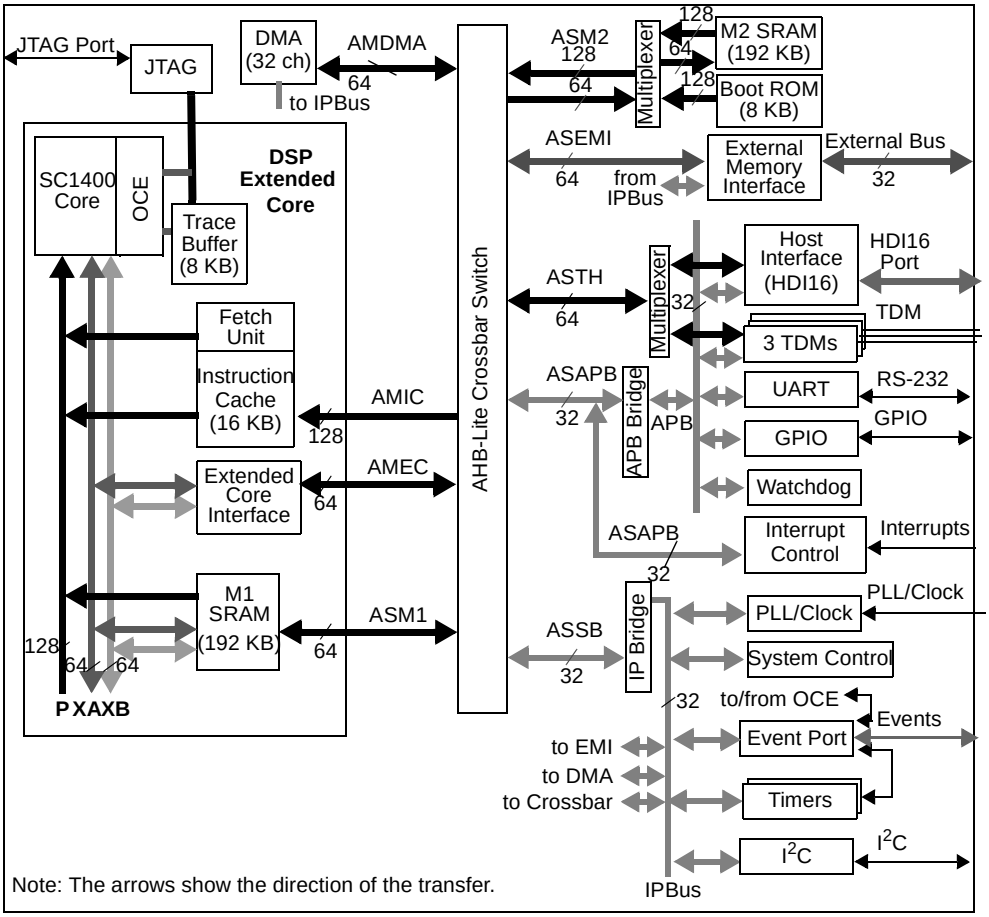
MSC7115

Low-Cost DSP with DDR Controller



The MSC7115 device targets high-bandwidth highly computational DSP applications and is optimized for Enterprise class packet telephony applications, providing a competitive price per channel for voice over packet systems.

What's New?

Rev. 9 provides:

- Corrects data signal direction in **Figure 2-12**.
- Updates boot overview in **Section 4.4.3**.

Figure 1. MSC7115 Block Diagram

The MSC7115 device is a highly integrated DSP processor that contains the StarCore™ SC1400 core, 384 KB of SRAM memory, a 16 KB instruction cache, an 8 KB boot ROM, three 128-channel time-division multiplexing (TDM) interfaces with hardware support for µ/A-law decoding/encoding, a UART, a 32-channel DMA controller, a 16-bit host interface (HDI16) to support an external host processor, a programmable interrupt controller (PIC), an I^2C interface, two 16-bit quad cascadable timers, GPIO signals, and an on-chip emulator (OCE) and an event port for enhanced debug and system integration capability. The SC1400 core has four ALUs and performs at 1000 DSP million multiply accumulates per second (MMACS) with an internal 266 MHz clock at 1.2 V.

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Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Indicates a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Features

Table 1 lists the features of the MSC7115 device.

Table 1. MSC7115 Features

Feature	Description
StarCore SC1400 Core	• Up to 1000 MMACS using an internal 266 MHz clock at 1.2 V. A multiply-accumulate operation includes a multiply-add instruction with the associated data move and pointer update. • 4 data ALUs. • 16 data registers, 40 bits each. • 27 address registers, 32 bits each. • Hardware support for fractional and integer data types. • Very rich 16-bit wide orthogonal instruction set. • Up to six instructions executed in a single clock cycle. • Variable-length execution set (VLES) that can be optimized for code density and performance. • **IEEE**® Std. 1149.1™ JTAG port. • On-Chip Emulator (OCE10) module with real-time debugging capabilities.
Extended Core	The high-performance extended core delivers up to 1000 MMACS using 4 ALUs running up to 266 MHz, including: • SC1400 core processor. • 192 KB multi-port SRAM (M1) accessed by the SC1400 core with no wait states. • 16 KB, 16-way instruction cache (ICache). • Programmable instruction fetch unit. • Write buffer (4-entry). • Extended core interface module.
Internal Memory	The large internal memory space totals 408 KB: • 192 KB of M1 memory. • 16 KB ICache. • 192 KB internal shared memory (M2), accessible from the SC1400 instruction fetch unit, extended core interface, DMA controller, and other peripherals via the crossbar switch. • 8 KB boot ROM accessible from the SC1400 core.
External Memory Interface	• DDR memory controller. • Glueless interface to 133 MHz DDR-RAM. • 14-bit external address bus, supporting up to 1 GB of external memory. • 16- or 32-bit external data bus. • Memory controller supports: – Byte enables for 32-bit external data bus. – Data pipeline to reduce data set-up time for synchronous devices.
IPBus	Programmable modules include: • Crossbar switch. • DMA controller. • DDR controller. • Clock synthesis module. • I^2C module. • System control unit. • Timers.
Crossbar Switch	AHB-Lite crossbar switch, allowing parallel data transfers between four master ports and six slave ports, where each port connects to an AHB-Lite bus.
DMA Controller	Multi-channel DMA controller: • Up to 32 time-multiplexed channels. • Priority-based time-multiplexing between channels using 32 internal priority levels • Priorities can be fixed or round-robin. • A flexible channel configuration: – All channels support all features. – All channels connect to the slave ports on the crossbar.

Table 1. MSC7115 Features (Continued)

Feature	Description
External Interfaces	External interfaces and control modules managed on the advanced peripheral bus (APB), including: • 16-bit host interface (HDI16). • Three time-division multiplexing (TDM) modules, each supporting up to 128 channels. • Two 16-bit quad timers. • RS-232 interface/universal asynchronous receiver/transmitter (UART). • I^2C interface. • General-purpose input/output (GPIO) signals. • Interrupt controller to handle external interrupt functions (input and output).
Host Interface (HDI16)	Enhanced 16-bit wide interface provides a glueless connection to industry-standard microcontrollers, microprocessors, and DSPs. The HDI16 can also operate in 8-bit data bus mode and is fully compatible with the DSP56300 HDI08 bus from the external host side.
TDM Modules	Three independent TDM modules, each with the following features: • Totally independent receive and transmit, each having one data line, one clock line, and one frame sync line. • Frame sync line and clock line can be shared between receive and transmit within a single TDM or across all TDMs. • Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses. • Hardware A-law/μ-law conversion • Up to 50 Mbps per TDM (50 MHz bit clock). • Maximum rate is 1/4 the core frequency. • Up to 128 channels. • Each channel can be programmed to be active or inactive. • 8- or 16-bit word widths. • The TDM Sync Signals (TDMxTFS/TDMxRFS) can be configured as either input or output. • The TDM Clock Signals (TDMxTCK/TDMxRCK) can be configured as either input or output. • Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock. • Frame sync can be programmed as active low or active high. • Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame. • MSB or LSB first support.
Timers	Two quad 16-bit timers, each with the following features: • Cyclic or one-shot. • Input clock polarity control. • Interrupt request when counting reaches a programmed threshold. • Pulse or level interrupts. • Dynamically updated programmed threshold. • Read counter any time. • Maximum rate is 1/4 the core frequency.

Table 1. MSC7115 Features (Continued)

Feature	Description
UART	• Two signals for transmit data and receive data. • No clock, asynchronous mode. • Full-duplex operation. • Standard mark/space non-return-to-zero (NRZ) format. • 13-bit baud rate selection. • Programmable 8-bit or 9-bit data format. • Separately enabled transmitter and receiver. • Programmable transmitter output polarity. • Two receiver wake-up methods: – Idle line wake-up. – Address mark wake-up. • Separate receiver and transmitter interrupt requests. • Eight flags, the first five can generate interrupt request: – Transmitter empty. – Transmission complete. – Receiver full. – Idle receiver input. – Receiver overrun. – Noise error. – Framing error. – Parity error. • Receiver framing error detection. • Hardware parity checking. • 1/16 bit-time noise detection. • Maximum bit rate 5.0 Mbps. • Single-wire and loop operations.
I^2C Port	• 2-wire serial interface through GPIO. • Filtered inputs for noise suppression. • Compatibility with I^2C bus standard up to 100 kbps for standard mode and up to 400 kbps for Fast mode. • Bidirectional Data Transfer Protocol. • Multiple-master operation that also allows any number of devices implementing the I^2C-master software module to access the memory simultaneously at boot or any time. • Compatible with the I^2C-serial EEPROM access protocol, allowing memory access of up to one MB.
General-Purpose I/O (GPIO) Port	Bidirectional signal lines that either serve the peripherals or act as programmable I/O ports. Each port can be programmed separately to serve up to two dedicated peripherals.
Programmable Interrupt Controller (PIC)	Consolidates maskable interrupt and non-maskable interrupt sources.
Event Port	• Collects important signal devices. • Programmable combinations to provide triggering to internal device units including interrupts, breakpoints, or wake-up from low-power stop mode. • Lines can be configured to operate independently, be sequenced, or be enabled from an external source. • Can be used independently or with the OCE10 debug module.
System Control	• Reset controller. • Clock controller module. • Hardware bus monitors for the MSC7115 buses. • Software watchdog timer function. • fieldBIST™ hardware health diagnostics that can be invoked at power-up or off-line via software. • Event port.
Internal PLL	Generates up to 266 MHz clock for the SC1400 core and up to 133 MHz for the crossbar switch, DMA channels, M2 memory, and other peripherals.
Clock Synthesis Module	• Programmable low-power Stop and Wait modes. • Generation of all device clocks. • Halt and restart capability for on-chip peripherals.
Reduced Power Dissipation	• Separate power supply for internal logic and I/O. • Low-power standby modes. • Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent).

Table 1. MSC7115 Features (Continued)

Feature	Description
fieldBIST Hardware Diagnostics	Detects and provides visibility into unlikely field failures for systems with high availability. The Freescale unique fieldBIST ensures that the device: • Has structural integrity. • Operates at the rated speed. • Is free from reliability defects. Diagnostics can report partial or complete device inoperability. fieldBIST resolution can pinpoint the following uniquely: • 6 memory blocks, including ROM. • 3 logic levels (top, extended core, and peripherals). • 1 PLL. Simple JTAG interface allows easy integration to system firmware.
Packaging	400 ball MAP-BGA. • 17 × 17 mm. • 0.8 mm pitch. • Pb-free packaging technology.
Software Support	Real-time operating systems (RTOS) that fully supports MSC7115 device architecture (multi-core, memory hierarchy, ICache, timers, DMA, interrupts, peripherals): • High-performance and deterministic, delivering predictive response time. • Optimized to provide low interrupt latency with high data throughput. • Preemptive and priority-based multitasking. • Fully interrupt/event driven. • Small memory footprint. • Comprehensive set of APIs. • Fully supports MSC7115 DMA, interrupts, and timer schemes. Distributed system support, enables transparent inter-task communications: • Messaging mechanism between tasks using mailboxes and semaphores. • Networking support; data transfer between tasks running inside and outside the device using networking protocols. • Includes integrated device drivers for such peripherals as TDM, UART, and external buses.
	Additional features: • Incorporates task debugging utilities integrated with compilers and vendors. • Board support package (BSP) for MSC7115 ADS.
	Metrowerks® CodeWarrior® Integrated Development Environment (IDE): • C/C++ compiler with in-line assembly. Enables the developer to generate highly optimized DSP code. It translates code written in C/C++ into parallel fetch sets and maintains high code density. • SC1400 Core Simulator. Allows the user to run test code to emulate operation on the SC1400 core processor. • Librarian. Enables the user to create libraries for modularity. • C libraries. A collection of C/C++ functions for the developer's use. • Linker. Highly efficient linker to produce executables from object code. • Debugger. Seamlessly integrated real-time, non-intrusive multi-mode debugger that enables debugging of highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode. • Profiler. An analysis tool using a patented Binary Code Instrumentation (BCI) technique that enables the developer to identify program design inefficiencies.
	Boot options: • HDI16. • I^2C.
MetroWerks Application Development System (ADS) Board	• Host debug through single JTAG connector supports both processors. • Two kinds of ADS configurations: one with the MSC7116 as the host CPU and one without a host CPU. • Big Flash memory for stand-alone applications. • Support for the following communications ports: – 10/100Base-T. – T1/E1 TDM interface. – H.110. – Voice codec. – RS-232. – High-density (MICTOR) logic analyzer connectors to monitor MSC7115 signals – 6U cPCI form factor.

Table 1. MSC7115 Features (Continued)

Feature	Description
MetroWerks Evaluation Module (EVM) Kits	• MSC7116 device. • Single 32-bit DDR memory. • 256 KB I^2C EEPROM to boot the MSC7116 device. • OCE10 emulator/JTAG connector for debugging. • On-board 5 V power supply. • External power supply and cables. • Kit documentation. • Power indicators for 2.5 V, 3.3 V, and 5 V. • Hard-reset push-button to reset the MSC7116 device. • Support for the following communications ports: – HDI16 host port interface header. – 10/100Base-T (RJ-45). – T1/E1 TDM interface header. – 16-bit audio codec (3.5 mm jacks). – RS-232 (UART port). – Output header for timers, interrupts, and GPIOs. • Software support: – MSC711xEVM includes full-featured CodeWarrior Development Studio for MSC711x. – MSC711xEVMT includes evaluation copy of CodeWarrior Development Studio for MSC711x.

Product Documentation

The documents listed in **Table 2** are required for a complete description of the MSC7115 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Table 2. MSC7115 Documentation

Name	Description	Order Number
MSC7115 Technical Data	MSC7115 features list and physical, electrical, timing, and package specifications	MSC7115
MSC711x Reference Manual	Detailed functional description of memory and peripheral configuration, operation, and register programming	MSC711xRM
SC1000 Family Processor Core Reference Manual	Detailed description of the SC1000 family processor cores, including the SC1400, and instruction set	10180 See the StarCore LLC website at www.starcore-dsp.com
OCE10 On-Chip Emulator Reference Manual	Detailed description of the SC1000 family on-chip emulator.	10055 See the StarCore LLC website at www.starcore-dsp.com
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the MSC7115 product website

Signals/Connections 1

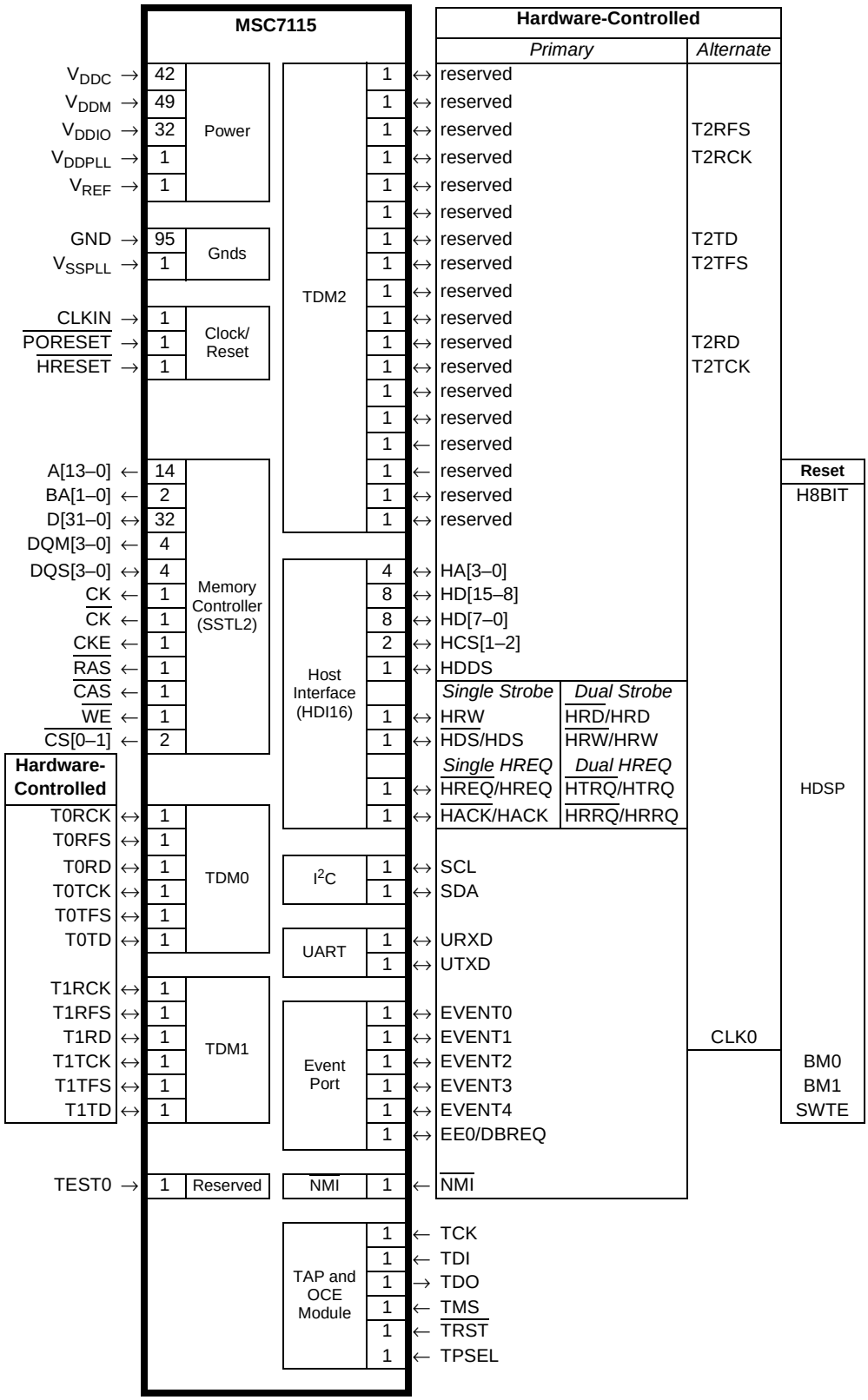
The MSC7115 external signals are organized into functional groups. **Table 1-1** lists the functional groups and the number of signal connections in each group, and it references the table that lists multiplexed signals within each group.

Most MSC7115 external peripherals are configured through ports A–D. The port configuration registers allow signal lines to be configured as software-controlled or hardware-controlled. If a signal is configured as software-controlled, it can be further defined as an input or an output. For port A, some signals configured as inputs may be configured as general-purpose signals or as maskable interrupt lines. If a signal is configured as hardware-controlled, it has a special function supporting one of the peripheral interfaces (for example, the HDI16). Some signals can also have an alternate hardware function (such as the CLKO signal). **Figure 1-1** shows the MSC7115 external signals organized by hardware-controlled function. **Figure 1-2** shows the configuration combinations for signals enabled through ports A–D.

Table 1-1. MSC7115 Functional Signal Groupings

Functional Group	Number of Signal Connections	Detailed Description
Power	125	**Table 1-2** on page 1-4.
Ground	96	**Table 1-3** on page 1-4.
Clock and Reset	3	**Table 1-4** on page 1-4.
Memory Controller	64	**Table 1-5** on page 1-5
Signals Configured through ports A–D: • TDM[0–2] • Host Interface (HDI16) • I^2C Interface • UART Interface • Event port • Boot mode (BM[3–2]) for mask set 1M88B only • GPIO only (port A, 19–26) • HDI16 Configuration (H8BIT) • Non-maskable interrupt (NMI) **Note:** Signals are grouped in this table by the principal function, but individual signal lines have alternate functions. For example, there are a total possible 42 GPIOs for mask set 1L44X or 46 GPIOs for mask set 1M88B, but only 8 lines have this as the principal function. See **Section 1.5** for details.	 18 27 2 2 5 2 8 1 1	 **Table 1-6** on page 1-7 **Table 1-7** on page 1-10 **Table 1-8** on page 1-12 **Table 1-9** on page 1-13 **Table 1-10** on page 1-14 **Table 1-11** on page 1-15 **Table 1-12** on page 1-16 **Table 1-13** on page 1-17 **Table 1-14** on page 1-17
Debugging (JTAG Test Access Port and OCE module)	7	**Table 1-15** on page 1-18
Reserved	1	**Table 1-16** on page 1-18
No connect (NC)	40	Do not connect any line, component, trace, or via to these pins.

Note: Although the package for this device uses ball connections, the connections are sometimes conventionally referred to as pins.



Note: For software-controlled functionality, see **Figure 1-2**. This figure does not include the 40 NC pins.

Figure 1-1. MSC7115 External Signals (Hardware-Controlled Functions)

Port Signal	Software Controlled (GPxCTL[x] = 0)			Hardware Controlled (GPxCTL[x] = 1)					Reset Configuration (sampled at deassertion of PORESET only)
	GPI (Default) GPxDDR[x] = 0 GPA_INTEN[x] = 0	Interrupt GPxDDR[x] = 0 GPA_INTEN[x] = 1	GPO GPxDDR[x] = 1	Primary Function CHPCFG[PAS] and CHPCFG[PDS] = 0				Alternate Function CHPCFG[PAS] = 1 CHPCFG[PDS] = 1	
								TDM2	
PA29	GPIA29	IRQ18	GPOA29	reserved				T2TFS	
PA28	GPIA28	IRQ17	GPOA28	reserved				T2RD	
PA27	GPIA27	IRQ16	GPOA27	reserved				T2RCK	
PA26	GPIA26	IRQ26	GPOA26	reserved					
PA25	GPIA25	IRQ25	GPOA25	reserved					
PA24	GPIA24	IRQ24	GPOA24	reserved					
PA23	GPIA23	IRQ23	GPOA23	reserved					
PA22	GPIA22	IRQ22	GPOA22	reserved					
PA21	GPIA21	IRQ21	GPOA21	reserved					
PA20	GPIA20	IRQ20	GPOA20	reserved					
PA19	GPIA19	IRQ19	GPOA19	reserved					
PA18	reserved	NMI	reserved		Event				Clock
PA17	GPIA17	IRQ13	GPOA17		EVNT1				CLKO
PA16	GPIA16	IRQ12	GPOA16		EVNT4	I²C			SWTE
PA15	GPIA15	IRQ14	GPOA15			SCL			
PA14	GPIA14	IRQ15	GPOA14			SDA	UART		
PA13	GPIA13	IRQ2	GPOA13				URXD		
PA12	GPIA12	IRQ3	GPOA12			TDM0	UTXD		
PA11	GPIA11	IRQ4	GPOA11			T0RCK			
PA10	GPIA10	IRQ5	GPOA10			T0RFS			
PA9	GPIA9	reserved	GPOA9			T0RD			
PA8	GPIA8	IRQ6	GPOA8			T0TCK			
PA7	GPIA7	IRQ7	GPOA7			T0TFS			
PA6	GPIA6	reserved	GPOA6			T0TD	TDM1		
PA5	GPIA5	IRQ0	GPOA5				T1RCK		
PA4	GPIA4	IRQ1	GPOA4				T1RFS		
PA3	GPIA3	IRQ8	GPOA3				T1RD		
PA2	GPIA2	IRQ9	GPOA2				T1TCK		
PA1	GPIA1	IRQ10	GPOA1				T1TFS		
PA0	GPIA0	IRQ11	GPOA0				T1TD		
							HDI16		
PB14	reserved		reserved				HDDS		
PB13	reserved		reserved				HDS or HWR		
PB12	reserved		reserved				HRW or HRD		
PB11	GPIB11[1]		GPOB11[1]				HCS2		
PB10	reserved		reserved				HCS1		
PB9	reserved		reserved				HACK or HRRQ		
PB8	reserved		reserved				HREQ or HTRQ		HDSP
PB7	reserved		reserved				HD7		
PB6	reserved		reserved				HD6		
PB5	reserved		reserved				HD5		
PB4	reserved		reserved				HD4		
PB3	reserved		reserved				HD3		
PB2	reserved		reserved				HD2		
PB1	reserved		reserved				HD1		
PB0	reserved		reserved				HD0		
PC15	GPIC15		GPOC15		EVNT3				BM1
PC14	GPIC14		GPOC14		EVNT2				BM0
PC13	reserved		reserved		EVNT0				
PC12	reserved		reserved		EE0/ DBREQ				
PC11	GPIC11[1]		GPOC11[1]				HA3		
PC10	reserved		reserved				HA2		
PC9	reserved		reserved				HA1		
PC8	reserved		reserved				HA0		
PC7	GPIC7		GPOC7				HD15		
PC6	GPIC6		GPOC6				HD14		
PC5	GPIC5		GPOC5				HD13		
PC4	GPIC4		GPOC4				HD12		
PC3	GPIC3		GPOC3				HD11		
PC2	GPIC2		GPOC2				HD10		
PC1	GPIC1		GPOC1				HD9		
PC0	GPIC0		GPOC0				HD8		
PD8	GPID8[1]		GPOD8[1]						BM3[2]
PD7	GPID7[1]		GPOD7[1]						BM2[2]
PD6	GPID6		GPOD6	reserved				T2TD	
PD5	GPID5		GPOD5	reserved				T2TCK	
PD4	GPID4		GPOD4	reserved				T2RFS	
PD2	reserved		reserved	reserved					H8BIT

Notes: **1.** Mask set 1M88B. For mask set 1L44X, these signals are reserved.
2. Mask set 1M88B only. For mask set 1L44X, these signals are not implemented.

Figure 1-2. Port A–D Signal Configuration Diagram

1.1 Power

Table 1-2. Power Inputs

Signal Name	Description
V_{DDC}	**Internal Logic Power** A dedicated well-regulated power source for the device core. Provide an extremely low impedance path to the V_{DDC} power rail.
V_{DDM}	**SSTL IO Driver Power** A dedicated power source for the DDR DRAM interface buffers. Provide adequate external decoupling capacitors.
V_{DDIO}	**Input/Output Power** The power source for the I/O buffers. Provide adequate external decoupling capacitors.
V_{DDPLL}	**System PLL Power** A dedicated well-regulated power for the system Phase Lock Loop (PLL). Provide an extremely low impedance path to the V_{DDPLL} power rail.
V_{REF}	**SSTL Reference Power** A reference power level for the SSTL2 memory interface.

1.2 Ground

Table 1-3. Ground Connections

Signal Name	Description
GND	**System Ground** An isolated common ground for the internal processing logic, I/O buffers, and the DDR DRAM interface buffers. Provide adequate external decoupling capacitors.
V_{SSPLL}	**System PLL Ground** An isolated ground for the system PLL. Provide an extremely low-impedance path to this ground.

1.3 Clock and Reset

Table 1-4. Clock and Reset Pin Definitions

Signal Name	Type	Description
CLKIN	Input	**Input Clock** Provides the primary clock source for the device.
$\overline{\text{PORESET}}$	Input	**Power-On Reset** When asserted, this line causes the MSC7115 device to enter the power-on reset state.
$\overline{\text{HRESET}}$	Input/ Output	**Hard Reset** When asserted, this open-drain line causes the MSC7115 to enter the hard reset state. **Note:** Connect an external pull-up to this pin.

1.4 Memory Controller

Refer to the memory controller chapter in the *MSC711x Reference Manual* for details on configuring these signals. To support DDR DRAM external memory, the memory controller uses SSTL2+ signal levels.

Table 1-5. Memory Controller Signals

Signal Name	Type	Description
A[13–0]	Output	**Address Bus** The memory interface address bus used to connect to external memory devices.
BA[1–0]	Output	**Bank Address** Selects the DDR DRAM bank.
D[31–0]	Input/ Output	**Data Bus** The MSC7115 device drives the bus during write cycles and the external memory drives the bus during read cycles.
DQM[3–0]	Output	**DDR DRAM DQM** Selects the specific byte lanes for DDR DRAM devices.
DQS[3–0]	Input/ Output	**DDR DRAM DQS** Strobe for byte-lane data capture.
CK	Output	**System Clock Out** The system bus clock.
$\overline{\text{CK}}$	Output	**System Clock Out Inverted** The inverted system bus clock.
CKE	Output	**Clock Enable** When asserted, this signal enables the system bus clock for the DDR DRAM.
$\overline{\text{RAS}}$	Output	**Row Address Strobe** Connects to DDR DRAM $\overline{\text{RAS}}$ input.
$\overline{\text{CAS}}$	Output	**Column Address Strobe** Connects to DDR DRAM $\overline{\text{CAS}}$ input.
$\overline{\text{WE}}$	Output	**Write Enable** Connects to DDR DRAM $\overline{\text{WE}}$ input.
$\overline{\text{CS}}$[0–1]	Output	**Chip Select 0–1** Enables specific memory devices or peripherals connected to the bus.

Note: The address and data bit ordering for the MSC7115 device differs from the MSC810x ordering. For the MSC7115 device, bit 0 is the least significant bit.

1.5 Multiplexed I/O Signal Ports A–D

Most of the MSC7115 I/O signals are multiplexed through ports A–D as shown in **Figure 1-2**. The function of the signals in this category depend on when the signals are used and how they are configured:

- Some configuration signals lines are sampled when the $\overline{\text{PORESET}}$ signal is deasserted. Pulling these signals up or down at reset configures specific aspects of device operation after reset.
- After reset, individual signals are defined by the settings of the Port Configuration Registers, with the following constraints:
  - Although the four port control registers are 32 bits wide, not all possible signal lines are implemented. The four ports support the following number of signal lines:
    - Port A supports 30 multiplexed signals.
    - Port B supports 15 multiplexed signals.
    - Port C supports 16 multiplexed signals.
    - Port D supports 4 multiplexed signals for mask set 1L44X and 6 multiplexed signals for mask set 1M88B.
  - The default configuration after reset for all port signals is software-controlled, general-purpose input (GPI), but this functionality is not implemented for all signals lines. Signal lines that cannot be defined as GPI are reserved. The four ports support the following number GPI signals:
    - Port A supports 29 GPI signals.
    - Port B does not support GPI signals for mask set 1L44x but supports 1 GPI signal for mask set 1M88B.
    - Port C supports 10 GPI signals for mask set 1L44X and 11 GPI signals for mask set 1M88B.
    - Port D supports 3 GPI signals for mask set 1L44X and 5 GPI signals for mask set 1M88B.
  - Port A supports 27 maskable interrupts ($\overline{\text{IRQ[0–26]}}$) and 1 non-maskable interrupt ($\overline{\text{NMI}}$) inputs. The $\overline{\text{NMI}}$ input line can only be used for this purpose and cannot be configured as any other signal. If the lines are configured as interrupt inputs through the Port A Interrupt Enable Register, they are not available for the other functions.
  - Leaving the port configuration for a signal line as software-controlled and changing the data direction to output changes the signal to a general-purpose output (GPO). Selecting this configuration for a port A signal disables the associated interrupt function if enabled by the Port A Interrupt Enable Register. The four ports support the following number of GPO signals:
    - Port A supports 29 GPO signals.
    - Port B does not support GPO signals for mask set 1L44X but supports 1 GPO signal for mask set 1M88B.
    - Port C supports 10 GPO signals for mask set 1L44X and 11 GPO signals for mask set 1M88B.
    - Port D supports 3 GPO signals for mask set 1L44X and 5 GPO signals for mask set 1M88B.
  - Changing the port configuration for a signal to hardware-controlled changes the signal functionality to the hardware-controlled function. For port A signals, this configuration also disables any associated interrupt function. The hardware-controlled function defines the individual signal for one of the supported interfaces, including TDM0, TDM1, the host interface (HDI16), I^2C interface, UART (RS-232) interface, or the event port. For proper operation, all the required signals in a specified interface must be enabled through the port registers and configured correctly through the individual interface configuration registers.
  - Ports A and D also have an alternate function for some signals. The ports must be configured as hardware-controlled and the PAS and PDS bits in the CHPCFG register must be set to select the alternate functionality. The alternate signals support the TDM2 interface and a clock output signal. Selecting the alternate function disables the specific signals used by the primary hardware-controlled function.

Note: Refer to the *MSC711x Reference Manual* for details on configuring these signals.

The following subsections describe the individual interfaces supported by the hardware-controlled options and indicate the other signals that are multiplexed with the supported signals.

1.5.1 TDM[0–2] Interface

Table 1-6. TDM[0–2] Interface Signals

Pin	Type	Description
GPIA11	Input	**General-Purpose Input A11 (default)** When configured through port A bit 11, performs as a general-purpose input.
$\overline{\text{IRQ4}}$	Input	**Interrupt Request 4** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA11	Output	**General-Purpose Output A11** When configured through port A bit 11, performs as a general-purpose output.
T0RCK	Input/Output	**TDM0 Receive Clock** The receive clock for TDM0. See the *MSC711x Reference Manual* for operation details.
GPIA10	Input	**General-Purpose Input A10 (default)** When configured through port A bit 10, performs as a general-purpose input.
$\overline{\text{IRQ5}}$	Input	**Interrupt Request 5** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA10	Output	**General-Purpose Output A10** When configured through port A bit 10, performs as a general-purpose output.
T0RFS	Input/Output	**TDM0 Receive Frame Sync** The receive frame sync for TDM0. See the *MSC711x Reference Manual* for operation details.
GPIA9	Input	**General-Purpose Input A9 (default)** When configured through port A bit 9, performs as a general-purpose input.
GPOA9	Output	**General-Purpose Output A9** When configured through port A bit 9, performs as a general-purpose output.
T0RD	Input/Output	**TDM0 Receive Data** The receive data for TDM0. See the *MSC711x Reference Manual* for operation details.
GPIA8	Input	**General-Purpose Input A8 (default)** When configured through port A bit 8, performs as a general-purpose input.
$\overline{\text{IRQ6}}$	Input	**Interrupt Request 6** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA8	Output	**General-Purpose Output A8** When configured through port A bit 8, performs as a general-purpose output.
T0TCK	Input/Output	**TDM0 Transmit Clock** The transmit clock for TDM0. See the *MSC711x Reference Manual* or operation details.
GPIA7	Input	**General-Purpose Input A7 (default)** When configured through port A bit 7, performs as a general-purpose input.
$\overline{\text{IRQ7}}$	Input	**Interrupt Request 7** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA7	Output	**General-Purpose Output A7** When configured through port A bit 7, performs as a general-purpose output.
T0TFS	Input/Output	**TDM0 Transmit Frame Sync** The transmit frame sync for TDM0. See the *MSC711x Reference Manual* for operation details.

Table 1-6. TDM[0–2] Interface Signals (Continued)

Pin	Type	Description
GPIA6	Input	**General-Purpose Input A9 (default)** When configured through port A bit 6, performs as a general-purpose input.
GPOA6	Output	**General-Purpose Output A6** When configured through port A bit 6, performs as a general-purpose output.
T0TD	Input/Output	**TDM0 Transmit Data** The transmit data for TDM0. See the *MSC711x Reference Manual* for operation details.
GPIA5	Input	**General-Purpose Input A5 (default)** When configured through port A bit 5, performs as a general-purpose input.
$\overline{\text{IRQ0}}$	Input	**Interrupt Request 0** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA5	Output	**General-Purpose Output A5** When configured through port A bit 5, performs as a general-purpose output.
T1RCK	Input/Output	**TDM1 Receive Clock** The receive clock for TDM1. See the *MSC711x Reference Manual* for operation details.
GPIA4	Input	**General-Purpose Input A4 (default)** When configured through port A bit 4, performs as a general-purpose input.
$\overline{\text{IRQ1}}$	Input	**Interrupt Request 1** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA4	Output	**General-Purpose Output A4** When configured through port A bit 4, performs as a general-purpose output.
T1RFS	Input/Output	**TDM1 Receive Frame Sync** The receive frame sync for TDM1. See the *MSC711x Reference Manual* for operation details.
GPIA3	Input	**General-Purpose Input A3 (default)** When configured through port A bit 3, performs as a general-purpose input.
$\overline{\text{IRQ8}}$	Input	**Interrupt Request 8** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA3	Output	**General-Purpose Output A3** When configured through port A bit 3, performs as a general-purpose output.
T1RD	Input/Output	**TDM1 Receive Data** The receive data for TDM1. See the *MSC711x Reference Manual* for operation details.
GPIA2	Input	**General-Purpose Input A2 (default)** When configured through port A bit 2, performs as a general-purpose input.
$\overline{\text{IRQ9}}$	Input	**Interrupt Request 9** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA2	Output	**General-Purpose Output A2** When configured through port A bit 2, performs as a general-purpose output.
T1TCK	Input/Output	**TDM1 Transmit Clock** The transmit clock for TDM1. See the *MSC711x Reference Manual* for operation details.

Table 1-6. TDM[0–2] Interface Signals (Continued)

Pin	Type	Description
GPIA1	Input	**General-Purpose Input A1 (default)** When configured through port A bit 1, performs as a general-purpose input.
$\overline{\text{IRQ10}}$	Input	**Interrupt Request 10** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA1	Output	**General-Purpose Output A1** When configured through port A bit 1, performs as a general-purpose output.
T1TFS	Input/Output	**TDM1 Transmit Frame Sync** The transmit frame sync for TDM1. See the *MSC711x Reference Manual* for operation details.
GPIA0	Input	**General-Purpose Input A9 (default)** When configured through port A bit 6, performs as a general-purpose input.
$\overline{\text{IRQ11}}$	Input	**Interrupt Request 11** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA0	Output	**General-Purpose Output A0** When configured through port A bit 0, performs as a general-purpose output.
T1TD	Input/Output	**TDM1 Transmit Data** The transmit data for TDM1. See the *MSC711x Reference Manual* for operation details.
GPIA27	Input	**General-Purpose Input A27 (default)** When configured through port A bit 27, performs as a general-purpose input.
$\overline{\text{IRQ16}}$	Input	**Interrupt Request 16** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA27 +	Output	**General-Purpose Output A27** When configured through port A bit 27, performs as a general-purpose output.
T2RCK	Input/Output	**TDM2 Receive Clock** The receive clock for TDM2. See the *MSC711x Reference Manual* for operation details.
GPID4	Input	**General-Purpose Input D4 (default)** When configured through port D bit 4, performs as a general-purpose input.
GPOD4	Output	**General-Purpose Output D4** When configured through port D bit 4, performs as a general-purpose output.
Reserved	Output	**Reserved D4 (hardware-controlled)** When port D bit 4 is configured as hardware-controlled, reserved signal.
T2RFS	Input/Output	**TDM2 Receive Frame Sync** The receive frame sync for TDM2. See the *MSC711x Reference Manual* for operation details.
GPIA28	Input	**General-Purpose Input A28 (default)** When configured through port A bit 28, performs as a general-purpose input.
$\overline{\text{IRQ17}}$	Input	**Interrupt Request 17** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA28	Output	**General-Purpose Output A28** When configured through port A bit 28, performs as a general-purpose output.
T2RD	Input/Output	**TDM2 Receive Data** The receive data for TDM2. See the *MSC711x Reference Manual* for operation details.

Table 1-6. TDM[0–2] Interface Signals (Continued)

Pin	Type	Description
GPID5	Input	**General-Purpose Input D5 (default)** When configured through port D bit 5, performs as a general-purpose input.
GPOD5	Output	**General-Purpose Output D5** When configured through port D bit 5, performs as a general-purpose output.
Reserved	Output	**Reserved D5 (hardware-controlled)** When port D bit 5 is configured as hardware-controlled, reserved signal.
T2TCK	Input/Output	**TDM2 Transmit Clock** The transmit clock for TDM2. See the *MSC711x Reference Manual* for operation details.
GPIA29	Input	**General-Purpose Input A29 (default)** When configured through port A bit 29, performs as a general-purpose input.
$\overline{\text{IRQ18}}$	Input	**Interrupt Request 18** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA29	Input	**General-Purpose Output A29** When configured through port A bit 29, performs as a general-purpose output.
T2TFS	Input/Output	**TDM2 Transmit Frame Sync** The transmit frame sync for TDM2. See the *MSC711x Reference Manual* for operation details.
GPID6	Input	**General-Purpose Input D6 (default)** When configured through port D bit 6, performs as a general-purpose input.
GPOD6	Output	**General-Purpose Output D6** When configured through port D bit 6, performs as a general-purpose output.
Reserved	Input	**Reserved D6 (hardware-controlled)** When port D bit 6 is configured as hardware-controlled, reserved signal.
T2TD	Input/Output	**TDM2 Transmit Data** The transmit data for TDM2. See the *MSC711x Reference Manual* for operation details.

1.5.2 Host Interface Port

Table 1-7. Host Interface Signals

Pin	Data Flow	Description
Reserved or GPIC11	Input	**Reserved C11 or General-Purpose Input C11 (default)** When configured through port C bit 11, a reserved signal (mask set 1L44X) or a general-purpose input (mask set 1M88B).
Reserved or GPOC11	Output	**Reserved C11 or General-Purpose Output C11** When configured through port C bit 11, a reserved signal (mask set 1L44X) or a general-purpose output (mask set 1M88B).
HA3	Input	**Host Address 3** Host address line 3. Tie this signal to ground.
Reserved	Input	**Reserved C10–C8 (default)** When configured through port C bits 10–8, reserved signals.
HA[2–0]	Input	**Host Address 2–0** Host address bus. See the *MSC711x Reference Manual* for operation details.

Table 1-7. Host Interface Signals (Continued)

Pin	Data Flow	Description
GPIC[7–0]	Input	**General-Purpose Inputs C7–C0 (default)** When configured through port C bits 7–0, perform as a general-purpose inputs.
GPOC[7–0]	Output	**General-Purpose Outputs C7–C0** When configured through port C bits 7–0, perform as a general-purpose outputs.
HD[15–8]	Input/Output	**Host Data Bus (Upper Half)** The host data bus is used to access the internal host registers. See the *MSC711x Reference Manual* for operation details.
Reserved	Input	**Reserved B7–B0 (default)** When configured through port B bits 7–0, reserved signals.
HD[7–0]	Input/Output	**Host Data Bus (Lower Half)** The host data bus is used to access the internal host registers. See the *MSC711x Reference Manual* for operation details.
Reserved	Input	**Reserved B10 (default)** When configured through port B bit 10, reserved signal.
$\overline{\text{HCS1}}$/HCS1	Input	**Host Chip Select 1** When the HDI16 interface is enabled, this is one of the two chip-select pins. The polarity of this pin is programmable. The HDI16 chip select is a logical OR of HCS1 and HCS2 with appropriate polarity.
Reserved or GPIB11	Input	**Reserved B11 or General-Purpose Input B11 (default)** When configured through port B bit 11, a reserved signal (mask set 1L44X) or a general-purpose input (mask set 1M88B).
Reserved or GPOB11	Output	**Reserved B11 or General-Purpose Output B11** When configured through port B bit 11, a reserved signal (mask set 1L44X) or a general-purpose output (mask set 1M88B).
$\overline{\text{HCS2}}$/HCS2	Input	**Host Chip Select 2** When the HDI16 interface is enabled, this is one of the two chip-select pins. The polarity of this pin is programmable. The HDI16 chip select is a logical OR of HCS1 and HCS2 with appropriate polarity.
Reserved	Input	**Reserved B12 (default)** When configured through port B bit 12, reserved signal.
HRW	Input	**Host Read Write** When HDI16 is configured to work in single strobe mode, this is the Read/Write input (HRW).
$\overline{\text{HRD}}$/HRD	Input	**Host Read Data Strobe** When HDI16 is programmed to interface a double data strobe host bus, this pin is the Read Data Strobe input (HRD). The polarity of the data strobe is programmable.
Reserved	Input	**Reserved B13 (default)** When configured through port B bit 13, reserved signal.
$\overline{\text{HDS}}$/HDS	Input	**Host Data Strobe** When the HDI16 is programmed to interface a single data strobe host bus, this pin is the Data Strobe input (HDS). The polarity of the data strobe is programmable.
$\overline{\text{HWR}}$/HWR	Input	**Host Write Data Strobe** When the HDI16 is programmed to interface a double data strobe host bus, this pin is the Write Data Strobe input (HWR). The polarity of the data strobe is programmable.
Reserved	Input	**Reserved B14 (default)** When configured through port B bit 14, reserved signal.
HDDS	Input	**Host Dual Data Strobe** When the HDI16 is enabled, this pin indicates whether to use Single or Dual Data Strobe mode.

Table 1-7. Host Interface Signals (Continued)

Pin	Data Flow	Description
Reserved	Input	**Reserved B8 (default)** When configured through port B bit 8, reserved signal.
$\overline{\text{HREQ}}$/HREQ	Output	**Host Request** When the HDI16 is programmed to interface a single host request host bus, this pin is the Host Request output (HREQ). The polarity of the host request is programmable. The host request may be programmed as a driven or open-drain output. When configured for open drain, an external pull-up must be used on this pin.
$\overline{\text{HTRQ}}$/HTRQ	Output	**Host Transmit Request** When the HDI16 is programmed to interface a double host request host bus, this pin is the Transmit Host Request output (HTRQ). The polarity of the host request is programmable. The host request may be programmed as a driven or open-drain output. When configured for open drain, an external pull-up must be used on this pin.
HDSP	Input	**Host Data Strobe Polarity** This pin is sampled at the deassertion of $\overline{\text{PORESET}}$. This pin defines the polarity of host port read-write strobes.
Reserved	Input	**Reserved B9 (default)** When configured through port B bit 9, reserved signal.
$\overline{\text{HACK}}$/HACK	Input	**Host Acknowledge** When the HDI16 is programmed to interface a single host request host bus, this pin is the Host Acknowledge input (HACK). The polarity of the host acknowledge is programmable.
$\overline{\text{HRRQ}}$/HRRQ	Output	**Host Receive Request** When the HDI16 is programmed to interface a double host request host bus, this pin is the Receive Host Request output (HRRQ). The polarity of the host request is programmable. The host request may be programmed as a driven or open-drain output.

1.5.3 I^2C Port

Table 1-8. I^2C Signals

Pin	Data Flow	Description
GPIA15	Input	**General-Purpose Input A15 (default)** When configured through port A bit 15, performs as a general-purpose input.
$\overline{\text{IRQ14}}$	Input	**Interrupt Request 14** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA15	Output	**General-Purpose Output A15** When configured through port A bit 15, performs as a general-purpose output.
SCL	Input/Output	**I^2C Clock** The I^2C clock signal. For I^2C, use an external pull-up on this pin. See the *MSC711x Reference Manual* for operation details.

Table 1-8. I^2C Signals (Continued)

Pin	Data Flow	Description
GPIA14	Input	**General-Purpose Input A14 (default)** When configured through port A bit 14, performs as a general-purpose input.
$\overline{\text{IRQ15}}$	Input	**Interrupt Request 15** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA14	Output	**General-Purpose Output A14** When configured through port A bit 14, performs as a general-purpose output.
SDA	Input/Output	**I^2C Data** I^2C data signal. When used for I^2C, use an external pull-up on this pin. See the *MSC711x Reference Manual* for operation details.

1.5.4 UART Port

Table 1-9. UART Signals

Pin	Data Flow	Description
GPIA13	Input	**General-Purpose Input A13 (default)** When configured through port A bit 13, performs as a general-purpose input.
$\overline{\text{IRQ2}}$	Input	**Interrupt Request 2** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA13	Output	**General-Purpose Output A13** When configured through port A bit 13, performs as a general-purpose output.
URXD	Input	**UART Receive Data** UART receive data line.
GPIA12	Input	**General-Purpose Input A12 (default)** When configured through port A bit 12, performs as a general-purpose input.
$\overline{\text{IRQ3}}$	Input	**Interrupt Request 3** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA12	Output	**General-Purpose Output A12** When configured through port A bit 12, performs as a general-purpose output.
UTXD	Output	**UART Transmit Data** UART transmit data line.

1.5.5 Event Port

Table 1-10. Event Port Signals

Pin	Data Flow	Description
Reserved	Input	**Reserved PC13 (default)** When configured through port C bit 13, reserved signal.
EVNT0	Input/ Output	**Event 0** Provides input and output events to the system control unit event multiplexers.
GPIA17	Input	**General-Purpose Input A17 (default)** When configured through port A bit 17, performs as a general-purpose input.
$\overline{\text{IRQ13}}$	Input	**Interrupt Request 13** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA17	Output	**General-Purpose Output A17** When configured through port A bit 17, performs as a general-purpose output.
EVNT1	Input/ Output	**Event 1** Provides input and output events to the system control unit event multiplexers.
CLKO	Output	**CLKO** Output clock signal when the function is enabled.
GPIC14	Input	**General-Purpose Input C14 (default)** When configured through port C bit 14, performs as a general-purpose input.
GPOC14	Output	**General-Purpose Output C14** When configured through port C bit 14, performs as a general-purpose output.
EVNT2	Input/ Output	**Event 2** Provides input and output events to the system control unit event multiplexers.
BM0	Input	**Boot Mode 0** This pin is sampled at the deassertion of $\overline{\text{PORESET}}$. With BM1, the value of this signal defines the boot mode of the MSC7115. *MSC711x Reference Manual* for operation details.
GPIC15	Input	**General-Purpose Input C15 (default)** When configured through port C bit 15, performs as a general-purpose input.
GPOC15	Output	**General-Purpose Output C15** When configured through port C bit 15, performs as a general-purpose output.
EVNT3	Input/ Output	**Event 3** Provides input and output events to the system control unit event multiplexers.
BM1	Input	**Boot Mode 1** This pin is sampled at the deassertion of $\overline{\text{PORESET}}$. With BM0, the value of this signal defines the boot mode of the MSC7115. See the *MSC711x Reference Manual* for operation details.

Table 1-10. Event Port Signals

Pin	Data Flow	Description
GPIA16	Input	**General-Purpose Input A16 (default)** When configured through port A bit 16, performs as a general-purpose input.
$\overline{\text{IRQ12}}$	Input	**Interrupt Request 12** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA16	Output	**General-Purpose Output A16** When configured through port A bit 16, performs as a general-purpose output.
EVNT4	Input/ Output	**Event 4** Provides input and output events for the system control unit event multiplexers. Can be used to indicate that the SC1400 core is in Debug mode.
SWTE	Input	**Software Watchdog Timer Disable** This pin is sampled at the deassertion of $\overline{\text{PORESET}}$. If the signal is sampled high, the watchdog timer is enabled. If it is sampled low, the watchdog timer is disabled.
Reserved	Input	**Reserved PC12 (default)** When configured through port C bit 12, reserved signal.
EE0/DBREQ	Input/ Output	**OCE Event Bit 0/Debug Request** Debug port EE0 functionality is detected by EDCA0 when EE0DEF=00, which generates an OCE event or enables EDCA0 when EE0DEF=10 in the SC1400 EE_CTRL register. When the port is programmed for Debug mode (EE0DEF=11 in the SC1400 EE_CTRL register, asserting this signal causes the core to enter Debug mode.

1.5.6 Boot Mode 3–2 (implemented in mask set 1M88B only)

Table 1-11. BM[3–2] Signals

Pin	Data Flow	Description
Reserved or GPID8	Input	**Reserved D8 or General-Purpose Input D8 (default)** When configured through port D bit 8, a reserved signal (mask set 1L44X) or a general-purpose input (mask set 1M88B).
Reserved or GPOD8	Output	**Reserved D8 or General-Purpose Output D8** When configured through port D bit 8, a reserved signal (mask set 1L44X) or a general-purpose output (mask set 1M88B).
BM3	Input	**Boot Mode 3** For the 1M88B mask set only, this pin is sampled at the deassertion of $\overline{\text{PORESET}}$. Along with BM[0–2] the value of this signal defines the boot mode for the device. For designs developed using the 1L44X mask set, this signal can be left unconnected.
Reserved or GPID7	Input	**Reserved D7 or General-Purpose Input D7 (default)** When configured through port D bit 7, a reserved signal (mask set 1L44X) or a general-purpose input (mask set 1M88B).
Reserved or GPOD7	Output	**Reserved B11 or General-Purpose Output B11** When configured through port D bit 7, a reserved signal (mask set 1L44X) or a general-purpose output (mask set 1M88B).
BM2	Input	**Boot Mode 2** For the 1M88B mask set only, this pin is sampled at the deassertion of $\overline{\text{PORESET}}$. Along with BM[0–1] and BM3, the value of this signal defines the boot mode for the device. For designs developed using the 1L44X mask set, this signal can be left unconnected.

1.5.7 GPIO

Table 1-12. GPIO Signals

Pin	Data Flow	Description
GPIA20	Input	**General-Purpose Input A20 (default)** When configured through port A bit 20, performs as a general-purpose input.
$\overline{\text{IRQ20}}$	Input	**Interrupt Request 20** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA20	Output	**General-Purpose Output A20** When configured through port A bit 20, performs as a general-purpose output.
GPIA19	Input	**General-Purpose Input A19 (default)** When configured through port A bit 19, performs as a general-purpose input.
$\overline{\text{IRQ19}}$	Input	**Interrupt Request 19** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA19	Output	**General-Purpose Output A19** When configured through port A bit 19, performs as a general-purpose output.
GPIA22	Input	**General-Purpose Input A22 (default)** When configured through port A bit 22, performs as a general-purpose input.
$\overline{\text{IRQ22}}$	Input	**Interrupt Request 22** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA22	Output	**General-Purpose Output A22** When configured through port A bit 22, performs as a general-purpose output.
GPIA21	Input	**General-Purpose Input A21 (default)** When configured through port A bit 21, performs as a general-purpose input.
$\overline{\text{IRQ21}}$	Input	**Interrupt Request 21** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA21	Output	**General-Purpose Output A21** When configured through port A bit 21, performs as a general-purpose output.
GPIA23	Input	**General-Purpose Input A23 (default)** When configured through port A bit 23, performs as a general-purpose input.
$\overline{\text{IRQ23}}$	Input	**Interrupt Request 23** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA23	Output	**General-Purpose Output A23** When configured through port A bit 23, performs as a general-purpose output.
GPIA24	Input	**General-Purpose Input A24 (default)** When configured through port A bit 24, performs as a general-purpose input.
$\overline{\text{IRQ24}}$	Input	**Interrupt Request 24** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA24	Output	**General-Purpose Output A24** When configured through port A bit 24, performs as a general-purpose output.

Table 1-12. GPIO Signals (Continued)

Pin	Data Flow	Description
GPIA25	Input	**General-Purpose Input A25 (default)** When configured through port A bit 25, performs as a general-purpose input.
$\overline{\text{IRQ25}}$	Input	**Interrupt Request 25** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA25	Output	**General-Purpose Output A25** When configured through port A bit 25, performs as a general-purpose output.
GPIA26	Input	**General-Purpose Input A26 (default)** When configured through port A bit 26, performs as a general-purpose input.
$\overline{\text{IRQ26}}$	Input	**Interrupt Request 26** One of the 27 maskable interrupts that can be configured for the MSC7115 device.
GPOA26	Output	**General-Purpose Output A26** When configured through port A bit 26, performs as a general-purpose output.

1.5.8 HDI16 Configuration

Table 1-13. HDI16 Configuration Signal

Pin	Data Flow	Description
H8BIT	Input	**Host 8/16 Bit Mode** This pin is sampled at the deassertion of $\overline{\text{PORESET}}$. If the line is sampled high at reset, the HDI16 operates in 8-bit mode when enabled. If the line is sampled low at reset, the HDI16 operates in 16-bit mode.

1.5.9 $\overline{\text{NMI}}$

Table 1-14. $\overline{\text{NMI}}$ Signal

Signal Name	Type	Signal Description
Reserved	Input	**Reserved A18 (default)** When configured through port A bit 18, reserved signal.
$\overline{\text{NMI}}$	Input	**Non-Maskable Interrupt** External device may assert this line to generate a non-maskable interrupt to the MSC7115 device.

1.6 OCE Event and JTAG Test Access Port

The MSC7115 supports the standard set of test access port (TAP) signals defined by **IEEE®** Std. 1149.1™ Test Access Port and Boundary-Scan Architecture specification and described in **Table 1-15**. The TPSEL pin should be tied to GND to access the TAP.

Table 1-15. OCE Event and JTAG TAP Signals

Pin	Data Flow	Description
TCK	Input	**Test Clock** Clock input for the MSC7115 JTAG controller to synchronize the test logic.
TDI	Input	**Test Data In** A test data input (with an internal pull-up resistor) that is sampled on the rising edge of TCK.
TDO	Output	**Test Data Out** A data output that can be three-stated and actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	**Test Mode Select** A test mode select input (with an internal pull-up resistor) that is sampled on the rising edge of TCK to sequence the TAP controllers state machine.
$\overline{\text{TRST}}$	Input	**Test Reset** The reset input to the MSC7115 JTAG controller (with an internal pull-up resistor).
TPSEL	Input	**Tap Select** When deasserted, the Boundary Scan TAP controller is selected, allowing for boundary scan. When asserted, the Debug TAP controller is selected, allowing access to the OCE port.

1.7 Reserved Signals

Table 1-16. Reserved Signals

Signal Name	Type	Signal Description
TEST0	Input	**Test** For manufacturing testing. You *must* connect this pin to GND.

Specifications 2

This chapter covers power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC711x User's Guide* and *MSC711x Reference Manual*.

Note: The MSC7115 electrical specifications are preliminary and many are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after thorough characterization and device qualifications have been completed.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 describes the maximum electrical ratings for the MSC7115.

Table 2-1. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.5	V
Memory supply voltage	V_{DDM}	4.0	V
PLL supply voltage	V_{DDPLL}	1.5	V
I/O supply voltage	V_{DDIO}	–0.2 to 4.0	V
Input voltage	V_{IN}	(GND – 0.2) to 4.0	V
Reference voltage	V_{REF}	4.0	V
Maximum operating temperature	T_J	105	°C
Minimum operating temperature	T_A	–40	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in **Table 2-2.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. **Section 4.1**, *Thermal Design Considerations* includes a formula for computing the chip junction temperature (T_J).

2.2 Recommended Operating Conditions

Table 2-2 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2-2. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.14 to 1.26	V
Memory supply voltage	V_{DDM}	2.38 to 2.63	V
PLL supply voltage	V_{DDPLL}	1.14 to 1.26	V
I/O supply voltage	V_{DDIO}	3.14 to 3.47	V
Reference voltage	V_{REF}	1.19 to 1.31	V
Operating temperature range	T_J T_A	maximum: 105 minimum: –40	°C °C

2.3 Thermal Characteristics

Table 2-3 describes thermal characteristics of the MSC7115 for the MAP-BGA package.

Table 2-3. Thermal Characteristics for MAP-BGA Package

Characteristic	Symbol	MAP-BGA 17 × 17 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	39	31	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	23	20	°C/W
Junction-to-board[4]	$R_{\theta JB}$	12		°C/W
Junction-to-case[5]	$R_{\theta JC}$	7		°C/W
Junction-to-package-top[6]	Ψ_{JT}	2		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 4.1, *Thermal Design Considerations* explains these characteristics in detail.

2.4 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC7115.

Note: The leakage current is measured for nominal voltage values must vary in the same direction (for example, both V_{DDIO} and V_{DDC} vary by +2 percent or both vary by –2 percent).

Table 2-4. DC Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
Core and PLL voltage	V_{DDC} V_{DDPLL}	1.14	1.2	1.26	V
DRAM interface I/O voltage[1]	V_{DDM}	2.375	2.5	2.625	V
I/O voltage	V_{DDIO}	3.135	3.3	3.465	V
DRAM interface I/O reference voltage[2]	V_{REF}	$0.49 \times V_{DDM}$	1.25	$0.51 \times V_{DDM}$	V
DRAM interface I/O termination voltage[3]	VTT	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V
Input high CLKIN voltage	V_{IHCLK}	2.4	3.0	3.465	V
DRAM interface input high I/O voltage	V_{IHM}	$V_{REF} + 0.28$	V_{DDM}	$V_{DDM} + 0.3$	V
DRAM interface input low I/O voltage	V_{ILM}	–0.3	GND	$V_{REF} - 0.18$	V
Input leakage current, $V_{IN} = V_{DDIO}$	I_{IN}	–1.0	0.09	1	µA
V_{REF} input leakage current	I_{VREF}	—	—	5	µA
Tri-state (high impedance off state) leakage current, $V_{IN} = V_{DDIO}$	I_{OZ}	–1.0	0.09	1	µA
Signal low input current, $V_{IL} = 0.4$ V	I_L	–1.0	0.09	1	µA
Signal high input current, $V_{IH} = 2.0$ V	I_H	–1.0	0.09	1	µA
Output high voltage, $I_{OH} = –2$ mA, except open drain pins	V_{OH}	2.0	3.0	—	V
Output low voltage, $I_{OL} = 5$ mA	V_{OL}	—	0	0.4	V
Typical core power[5] • at 200 MHz • at 266 MHz (mask set 1M88B only)	P_C	 — —	 222 293	 — —	 mW mW

Notes:
1. The value of V_{DDM} at the MSC7115 device must remain within 50 mV of V_{DDM} at the DRAM device at all times.
2. V_{REF} must be equal to 50% of V_{DDM} and track V_{DDM} variations as measured at the receiver. Peak-to-peak noise must not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the MSC7115 device. It is the level measured at the far end signal termination. It should be equal to V_{REF}. This rail should track variations in the DC level of V_{REF}.
4. Output leakage for the memory interface is measured with all outputs disabled, $0 \text{ V} \le V_{OUT} \le V_{DDM}$.
5. The core power values were measured.using a standard EFR pattern at typical conditions (25°C, 200 MHz or 266 MHz, 1.2 V core).

Table 2-5 lists the DDR DRAM capacitance.

Table 2-5. DDR DRAM Capacitance

Parameter/Condition	Symbol	Max	Unit
Input/output capacitance: DQ, DQS	C_{IO}	30	pF
Delta input/output capacitance: DQ, DQS	C_{DIO}	30	pF

Note: These values were measured under the following conditions:
- $V_{DDM} = 2.5 \text{ V} \pm 0.125 \text{ V}$
- f = 1 MHz
- $T_A = 25°C$
- $V_{OUT} = V_{DDM}/2$
- V_{OUT} (peak to peak) = 0.2 V

2.5 AC Timings

This section presents timing diagrams and specifications for individual signals and parallel I/O outputs and inputs. All AC timings are based on a 30 pF load, except where noted otherwise, and a 50 Ω transmission line. For any additional pF, use the following equations to compute the delay:

- Standard interface: $2.45 + (0.054 \times C_{load})$ ns
- DDR interface: $1.6 + (0.002 \times C_{load})$ ns

2.5.1 Clock and Timing Signals

The following tables describe clock signal characteristics. **Table 2-6** shows the maximum frequency values for internal (core, reference, and peripherals) and external (CLKO) clocks. You must ensure that maximum frequency values are not exceeded (see for the allowable ranges when using the PLL).

Table 2-6. Maximum Frequencies

Characteristic	Maximum in MHz	
	Mask Set 1L44X	Mask Set 1M88B
Core clock frequency (CLOCK)	200	266
External output clock frequency (CLKO)	50	67
Memory clock frequency (CK, $\overline{CK}$)	100	133
TDM clock frequency (TxRCK, TxTCK)	50	67

Table 2-7. Clock Frequencies in MHz

Characteristic	Symbol	Min	Max	
			Mask Set 1L44X	Mask Set 1M88B
CLKIN frequency	F_{CLKIN}	10	100	100
CLOCK frequency	F_{CORE}	—	200	266
CK, $\overline{CK}$ frequency	F_{CK}	—	100	133
TDMxRCK, TDMxTCK frequency	F_{TDMCK}	—	50	50
CLKO frequency	F_{CKO}	—	50	67
AHB/IPBus/APB clock frequency	F_{BCK}	—	100	133
Note: The rise and fall time of external clocks should be 5 ns maximum				

Table 2-8. System Clock Parameters

Characteristic	Min	Max	Unit
CLKIN frequency	10	100	MHz
CLKIN slope	—	5	ns
CLKIN frequency jitter (peak-to-peak)	—	1000	ps
CLKO frequency jitter (peak-to-peak)	—	150	ps

2.5.2 Configuring Clock Frequencies

This section describes important requirements for configuring clock frequencies in the MSC7115 device when using the PLL block. To configure the device clocking, you must program four fields in the Clock Control Register (CLKCTL):

- PLLDVF field. Specifies the PLL division factor. The output of the divider block is the input to the multiplier block.
- PLLMLTF field. Specifies the PLL multiplication factor. The output from the multiplier block is the VCO.
- RNG field. Selects the available PLL frequency range.
- CKSEL field. Selects the source for the core clock.

There are restrictions on the frequency range permitted at the beginning of the multiplication portion of the PLL that affect the allowable values for the PLLDVF and PLLMLTF fields. The following sections define these restrictions and provide guidelines to configure the device clocking when using the PLL. Refer to the Clock and Power Management chapter in the *MSC711x Reference Manual* for details on the clock programming model.

2.5.2.1 PLL Multiplier Restrictions

There are two restrictions for correct usage of the PLL block:

- The input frequency to the PLL multiplier block (that is, the output of the divider) must be in the range 10.5–19.5 MHz.
- The output frequency of the PLL multiplier must be in the range 300-600 MHz.

When programming the PLL for a desired output frequency using the PLLDVF, PLLMLTF, and RNG fields, you must meet these constraints.

2.5.2.2 Division Factors and Corresponding CLKIN Frequency Range

The value of the PLLDVF field determines the allowable CLKIN frequency range, as shown in **Table 2-9**.

Table 2-9. CLKIN Frequency Ranges by Divide Factor Value

PLLDVF Field Value	Divide Factor	CLKIN Frequency Range	Comments
0x00	1	10.5 to 19.5 MHz	Pre-Division by 1
0x01	2	21 to 39 MHz	Pre-Division by 2
0x02	3	31.5 to 58.5 MHz	Pre-Division by 3
0x03	4	42 to 78 MHz	Pre-Division by 4
0x04	5	52.5 to 97.5 MHz	Pre-Division by 5
0x05	6	63 to 100 MHz	Pre-Division by 6
0x06	7	73.5 to 100 MHz	Pre-Division by 7
0x07	8	84 to 100 MHz	Pre-Division by 8
0x08	9	94.5 to 100 MHz	Pre-Division by 9
Note: The maximum CLKIN frequency is 100 MHz. Therefore, the PLLDVF value must be in the range from 1–9.			

2.5.2.3 Multiplication Factor Range

The multiplier block output frequency ranges depend on the input clock frequency as shown in **Table 2-10**.

Table 2-10. PLLMLTF Ranges

Multiplier Block (Loop) Output Range	Minimum PLLMLTF Value	Maximum PLLMLTF Value
300 ≤ [Pre-Divided Clock × (PLLMLTF + 1)] ≤ 600 MHz	300/Pre-Divided Clock	600/Pre-Divided Clock
Note: This table results from the allowed range for F_{Loop}. The minimum and maximum multiplication factors are dependent on the frequency of the Pre-Divided Clock.		

2.5.2.4 Allowed Core Clock Frequency Range

The frequency delivered to the core, extended core, and peripheral depends on the value of the CLKCTRL[RNG] bit as shown in **Table 2-11**.

Table 2-11. F_{vco} Frequency Ranges

CLKCTRL[RNG] Value	Allowed Range of F_{vco}
1	$300 \le F_{vco} \le 600$ MHz
0	$150 \le F_{vco} \le 300$ MHz
Note: This table results from the allowed range for F_{vco}, which is F_{Loop} modified by CLKCTRL[RNG].	

This bit along with the CKSEL determines the frequency range of the core clock.

Table 2-12. Resulting Ranges Permitted for the Core Clock

CLKCTRL[CKSEL]	CLKCTRL[RNG]	Resulting Division Factor	Allowed Range of Core Clock	Comments
11	1	1	Reserved	Reserved
11	0	2	150 ≤ Core_Clk ≤ 200 MHz	Limited by range of PLL
01	1	2	150 ≤ Core_Clk ≤ 200 MHz	Limited by range of PLL
01	0	4	75 ≤ Core_Clk ≤ 150 MHz	Limited by range of PLL
Note: This table results from the allowed range for F_{OUT}, which depends on clock selected via CLKCTRL[CKSEL].				

2.5.2.5 Core Clock Frequency Range When Using DDR Memory

The core clock can also be limited by the frequency range of the DDR devices in the system. **Table 2-13** summarizes this restriction.

Table 2-13. Core Clock Ranges When Using DDR

DDR Type	Allowed Frequency Range for DDR CK	Corresponding Range for the Core Clock	Comments
DDR 200 (PC-1600)	83–100 MHz	166 ≤ core clock ≤ 200 MHz	Core limited to 2 × maximum DDR frequency
DDR 266 (PC-2100)	83–133 MHz	166 ≤ core clock ≤ 266 MHz	Core limited to 2 × maximum DDR frequency
DDR 333 (PC-2600)	83–150 MHz	166 ≤ core clock ≤ 300 MHz	Core limited to 2 × maximum DDR frequency

2.5.3 Reset Timing

The MSC7115 device has several inputs to the reset logic. All MSC7115 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. **Table 2-14** describes the reset sources.

Table 2-14. Reset Sources

Name	Direction	Description
Power-on reset (PORESET)	Input	Initiates the power-on reset flow that resets the MSC7115 and configures various attributes of the MSC7115. On PORESET, the entire MSC7115 device is reset. SPLL and DLL states are reset, HRESET is driven, the SC1400 extended core is reset, and system configuration is sampled. The system is configured only when PORESET is asserted.
External Hard reset (HRESET)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC7115. While HRESET is asserted, HRESET is an open-drain output. Upon hard reset, HRESET is driven and the SC1400 extended core is reset.
Software watchdog reset	Internal	When the MSC7115 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
Bus monitor reset	Internal	When the MSC7115 bus monitor count reaches zero, a bus monitor hard reset is asserted. The enabled bus monitor event then generates an internal hard reset sequence.
JTAG EXTEST, CLAMP, or HIGHZ command	Internal	When a Test Access Port (TAP) executes an EXTEST, CLAMP, or HIGHZ command, the TAP logic asserts an internal reset signal that generates an internal soft reset sequence.

Table 2-15 summarizes the reset actions that occur as a result of the different reset sources.

Table 2-15. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)
	External only	External or Internal (Software Watchdog or Bus Monitor)	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (refer to **Section 2.5.3.1** for details)**.**	Yes	No	No
PLL and clock synthesis states Reset	Yes	No	No
HRESET Driven	Yes	Yes	No
Software watchdog and bus time-out monitor registers	Yes	Yes	Yes
Clock synthesis modules (STOPCTRL, HLTREQ, and HLTACK) reset	Yes	Yes	Yes
Extended core reset	Yes	Yes	Yes
Peripheral modules reset	Yes	Yes	Yes

2.5.3.1 Power-On Reset ($\overline{\text{PORESET}}$) Pin

Asserting $\overline{\text{PORESET}}$ initiates the power-on reset flow. $\overline{\text{PORESET}}$ must be asserted externally for at least 16 CLKIN cycles after external power to the MSC7115 reaches at least 2/3 V_{DD}.

2.5.3.2 Reset Configuration

The MSC7115 has two mechanisms for writing the reset configuration:

- From a host through the host interface (HDI16)
- From memory through the I^2C interface

Five signal levels (see **Chapter 1** for signal description details) are sampled on $\overline{\text{PORESET}}$ deassertion to define the boot and operating conditions:

- BM[0–1]
- SWTE
- H8BIT
- HDSP

2.5.3.3 Reset Timing Tables

Table 2-16 and **Figure 2-1** describe the reset timing for a reset configuration write.

Table 2-16. Timing for a Reset Configuration Write

No.	Characteristics	Expression	Unit
1	Required external $\overline{\text{PORESET}}$ duration minimum	$16/F_{CLKIN}$	clocks
2	Delay from $\overline{\text{PORESET}}$ deassertion to $\overline{\text{HRESET}}$ deassertion	$521/F_{CLKIN}$	clocks
Note: Timings are not tested, but are guaranteed by design.			

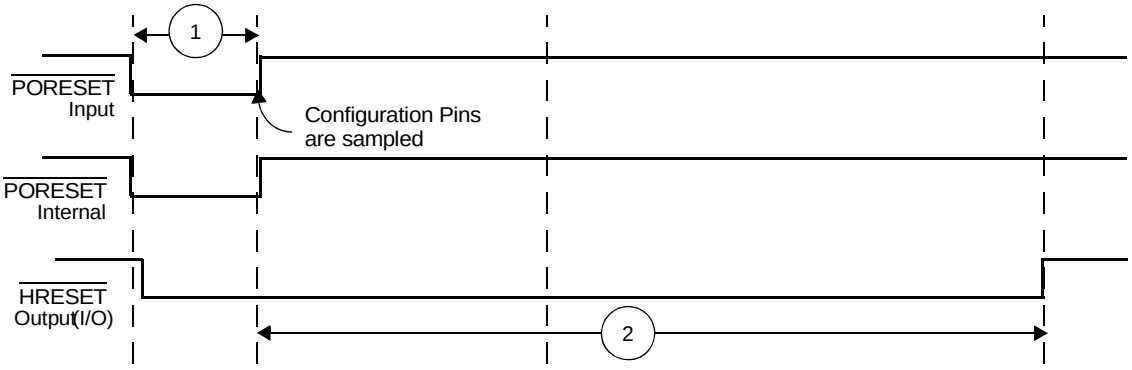


Figure 2-1. Timing Diagram for a Reset Configuration Write

2.5.4 DDR DRAM Controller Timing

This section provides the AC electrical characteristics for the DDR DRAM interface.

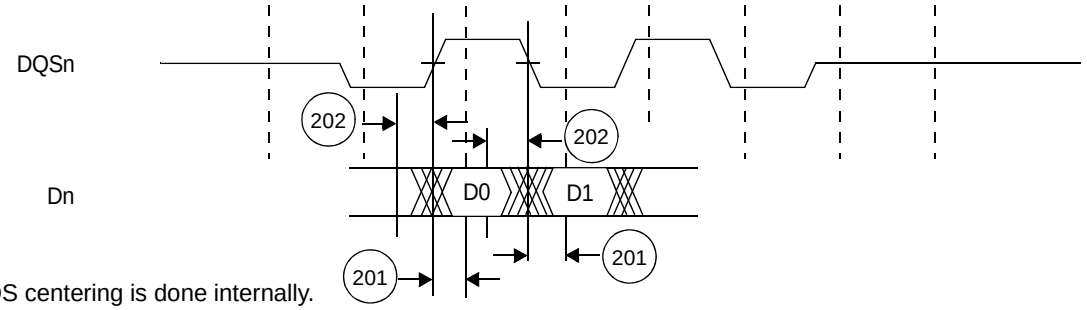
2.5.4.1 DDR DRAM Input AC Timing Specifications

Table 2-17 provides the input AC timing specifications for the DDR DRAM interface.

Table 2-17. DDR DRAM Input AC Timing

No.	Parameter	Symbol	Min	Max		Unit
				Mask Set 1L44X	Mask Set 1M88B	
—	AC input low voltage	V_{IL}	—	V_{REF} – 0.31	V_{REF} – 0.31	V
—	AC input high voltage	V_{IH}	V_{REF} + 0.31	V_{DDM} + 0.3	V_{DDM} + 0.3	V
201	Maximum Dn input setup skew relative to DQSn input	—	—	1026	900	ps
202	Maximum Dn input hold skew relative to DQSn input	—	—	386	900	ps

Notes:
1. Maximum possible skew between a data strobe (DQSn) and any corresponding bit of data (D[8n + {0...7}] if $0 \le n \le 7$).
2. See **Table 2-18** for t_{CK} value.
3. Dn should be driven at the same time as DQSn. This is necessary because the DQSn centering on the DQn data tenure is done internally.



Note: DQS centering is done internally.

Figure 2-2. DDR DRAM Input Timing Diagram

2.5.4.2 DDR DRAM Output AC Timing Specifications

Table 2-18 and **Table 2-19** list the output AC timing specifications and measurement conditions for the DDR DRAM interface.

Table 2-18. DDR DRAM Output AC Timing

No.	Parameter	Symbol	Min		Max	Unit
			Mask Set 1L44X	Mask Set 1M88B		
200	CK cycle time, (CK/$\overline{CK}$ crossing)[1] • 100 MHz (DDR200) • 133 MHz (DDR266)	t_{CK}	 10 Not applicable	 1.0 7.52	 — —	 ns ns
204	An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE output setup with respect to CK	t_{DDKHAS}	$0.5 \times t_{CK} - 2250$	$0.5 \times t_{CK} - 1000$	—	ps
205	An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE output hold with respect to CK	t_{DDKHAX}	$0.5 \times t_{CK} - 1250$	$0.5 \times t_{CK} - 1000$	—	ps
206	$\overline{CSn}$ output setup with respect to CK	t_{DDKHCS}	$0.5 \times t_{CK} - 2250$	$0.5 \times t_{CK} - 1000$	—	ps
207	$\overline{CSn}$ output hold with respect to CK	t_{DDKHCX}	$0.5 \times t_{CK} - 1250$	$0.5 \times t_{CK} - 1000$	—	ps
208	CK to DQSn[2]	t_{DDKHMH}	–600	–600	600	ps
209	Dn/DQMn output setup with respect to DQSn[3]	t_{DDKHDS}, t_{DDKLDS}	$0.25 \times t_{MCK} - 1050$	$0.25 \times t_{CK} - 750$	—	ps
210	Dn/DQMn output hold with respect to DQSn[3]	t_{DDKHDX}, t_{DDKLDX}	$0.25 \times t_{CK} - 1050$	$0.25 \times t_{CK} - 750$	—	ps
211	DQSn preamble start[4]	t_{DDKHMP}	$-0.25 \times t_{CK}$	$-0.25 \times t_{CK}$	—	ps
212	DQSn epilogue end[5]	t_{DDKHME}	–600	–600	600	ps

Notes:
1. All CK/$\overline{CK}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
2. t_{DDKHMH} can be modified through the TCFG2[WRDD] DQSS override bits. The DRAM requires that the first write data strobe arrives 75–125% of a DRAM cycle after the write command is issued. Any skew between DQSn and CK must be considered when trying to achieve this 75%–125% goal. The TCFG2[WRDD] bits can be used to shift DQSn by 1/4 DRAM cycle increments. The skew in this case refers to an internal skew existing at the signal connections. By default, the CK/$\overline{CK}$ crossing occurs in the middle of the control signal (An/$\overline{RAS}$/$\overline{CAS}$/$\overline{WE}$/CKE) tenure. Setting TCFG2[ACSM] bit shifts the control signal assertion 1/2 DRAM cycle earlier than the default timing. This means that the signal is asserted no earlier than 410 ps before the CK/$\overline{CK}$ crossing and no later than 677 ps after the crossing time; the device uses 1087 ps of the skew budget (the interval from –410 to +677 ps). Timing is verified by referencing the falling edge of CK. See Chapter 10 of the *MSC711x Reference Manual* for details.
3. Determined by maximum possible skew between a data strobe (DQS) and any corresponding bit of data. The data strobe should be centered inside of the data eye.
4. Please note that this spec is in reference to the DQSn first rising edge. It could also be referenced from CK(r), but due to programmable delay of the write strobes (TCFG2[WRDD]), there pre-amble may be extended for a full DRAM cycle. For this reason, we reference from DQSn.
5. All outputs are referenced to the rising edge of CK. Note that this is essentially the CK/DQSn skew in spec 208. In addition there is no real “maximum” time for the epilogue end. JEDEC does not require this is as a device limitation, but simply for the chip to guarantee fast enough write to read turn-around times. This is already guaranteed by the memory controller operation.

Figure 2-3 shows the DDR DRAM output timing diagram.

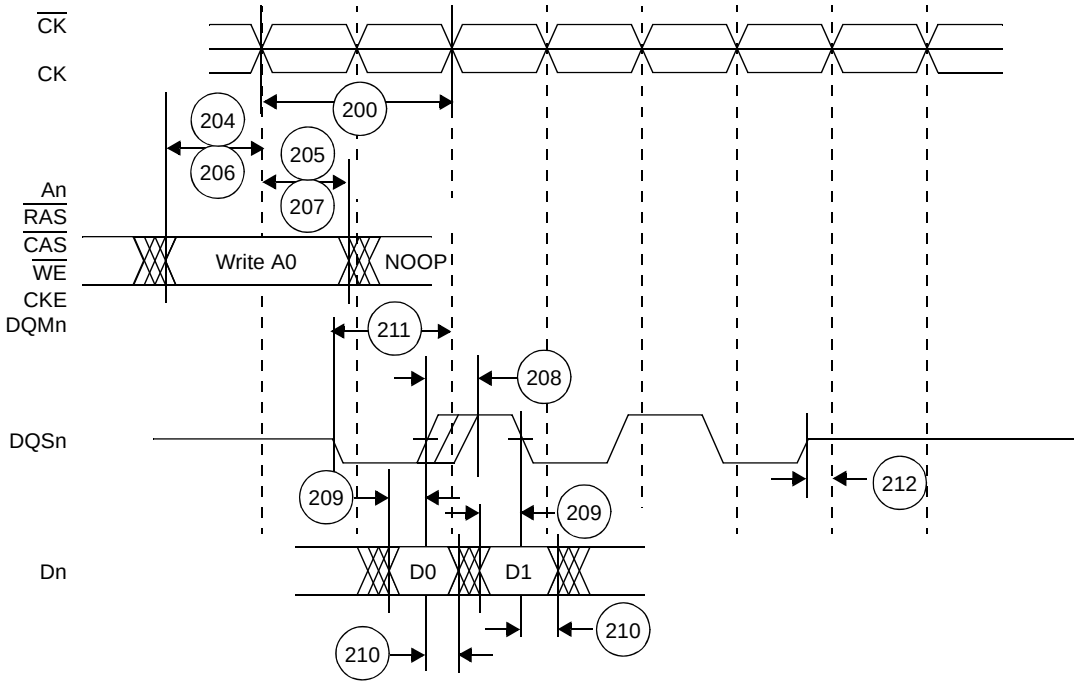


Figure 2-3. DDR DRAM Output Timing Diagram

Figure 2-4 provides the AC test load for the DDR DRAM bus.

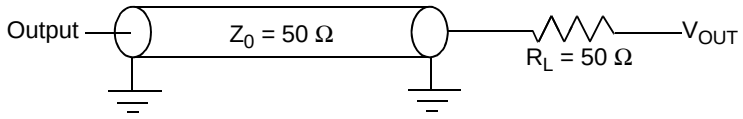


Figure 2-4. DDR DRAM AC Test Load

Table 2-19. DDR DRAM Measurement Conditions

Symbol	DDR DRAM	Unit
V_{TH}[1]	V_{REF} ± 0.31 V	V
V_{OUT}[2]	0.5 × V_{DDM}	V

Notes: **1.** Data input threshold measurement point.
2. Data output measurement point.

2.5.5 TDM Timing

Table 2-20. TDM Timing

No.	Characteristic	Expression	Min	Max	Units
300	TDMxRCK/TDMxTCK	TC	20.0	—	ns
301	TDMxRCK/TDMxTCK High Pulse Width	0.4 × TC	8.0	—	ns
302	TDMxRCK/TDMxTCK Low Pulse Width	0.4 × TC	8.0	—	ns
303	TDM all input Setup time		3.0	—	ns
304	TDMxRD Hold time		3.5	—	ns
305	TDMxTFS/TDMxRFS input Hold time		2.0	—	ns
306	TDMxTCK High to TDMxTD output active		4.0	—	ns
307	TDMxTCK High to TDMxTD output valid		—	14.0	ns
308	TDMxTD hold time		2.0	—	ns
309	TDMxTCK High to TDMxTD output high impedance		—	10.0	ns
310	TDMXTFS/TDMxRFS output valid		—	13.5	ns
311	TDMxTFS/TDMxRFS output hold time		2.5	—	ns

Notes:
1. Output values are based on 30 pF capacitive load.
2. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. Refer to the *MSC711x Reference Manual* for details. TDMxTCK and TDMxRCK are shown using the rising edge.

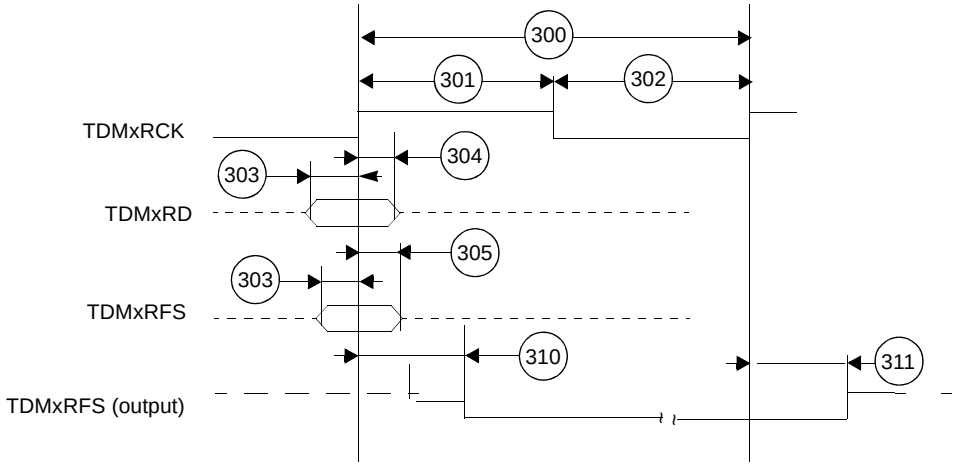


Figure 2-5. TDM Receive Signals

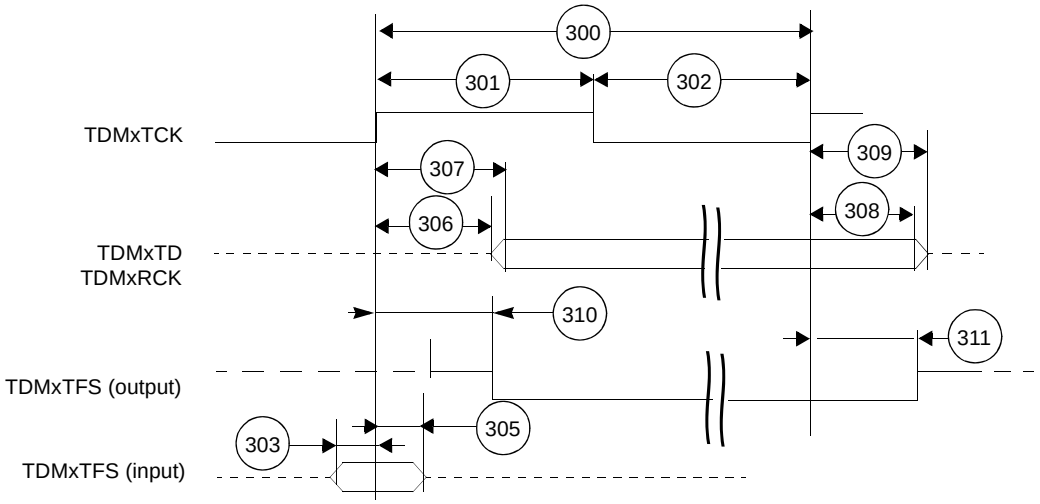


Figure 2-6. TDM Transmit Signals

2.5.6 HDI16 Signals

Table 2-21. Host Interface (HDI16) Timing[1, 2]

No.	Characteristics[3]	Mask Set 1L44X		Mask Set 1M88B		Unit
		Expression	Value	Expression	Value	
40	Host Interface Clock period	T_{HCLK}	Note 1	T_{CORE}	Note 1	ns
44a	Read data strobe minimum assertion width[4] HACK read minimum assertion width	$3.0 \times T_{HCLK}$	Note 11	$2.0 \times T_{CORE} + 9.0$	Note 11	ns
44b	Read data strobe minimum deassertion width[4] HACK read minimum deassertion width	$1.5 \times T_{HCLK}$	Note 11	$1.5 \times T_{CORE}$	Note 11	ns
44c	Read data strobe minimum deassertion width[4] after "Last Data Register" reads[5,6], or between two consecutive CVR, ICR, or ISR reads[7] HACK minimum deassertion width after "Last Data Register" reads[5,6]	$2.5 \times T_{HCLK}$	Note 11	$2.5 \times T_{CORE}$	Note 11	ns
45	Write data strobe minimum assertion width[8] HACK write minimum assertion width	$1.5 \times T_{HCLK}$	Note 11	$1.5 \times T_{CORE}$	Note 11	ns
46	Write data strobe minimum deassertion width[8] HACK write minimum deassertion width after ICR, CVR and Data Register writes[5]	$2.5 \times T_{HCLK}$	Note 11	$2.5 \times T_{CORE}$	Note 11	ns
47	Host data input minimum setup time before write data strobe deassertion[8] Host data input minimum setup time before HACK write deassertion	—	3.0	—	2.5	ns
48	Host data input minimum hold time after write data strobe deassertion[8] Host data input minimum hold time after HACK write deassertion	—	4.0	—	2.5	ns
49	Read data strobe minimum assertion to output data active from high impedance[4] HACK read minimum assertion to output data active from high impedance	—	1.0	—	1.0	ns
50	Read data strobe maximum assertion to output data valid[4] HACK read maximum assertion to output data valid	$(2.0 \times T_{HCLK}) + 8.0$	Note 11	$(2.0 \times T_{CORE}) + 8.0$	Note 11	ns
51	Read data strobe maximum deassertion to output data high impedance[4] HACK read maximum deassertion to output data high impedance	—	8.0	—	9.0	ns
52	Output data minimum hold time after read data strobe deassertion[4] Output data minimum hold time after HACK read deassertion	—	1.0	—	1.0	ns
53	HCS[1–2] minimum assertion to read data strobe assertion[4]	—	0.0	—	0.5	ns
54	HCS[1–2] minimum assertion to write data strobe assertion[8]	—	0.0	—	0.0	ns
55	HCS[1–2] maximum assertion to output data valid	$(2.0 \times T_{HCLK}) + 8.0$	Note 11	$(2.0 \times T_{CORE}) + 6.0$	Note 11	ns
56	HCS[1–2] minimum hold time after data strobe deassertion[9]	—	0.0	—	0.5	ns
57	HA[0–3], HRW minimum setup time before data strobe assertion[9]	—	5.0	—	5.0	ns
58	HA[0–3], HRW minimum hold time after data strobe deassertion[9]	—	5.0	—	5.0	ns
61	Maximum delay from read data strobe deassertion to host request deassertion for "Last Data Register" read[4, 5, 10]	$(3.0 \times T_{HCLK}) + 8.0$	Note 11	$(3.0 \times T_{CORE}) + 6.0$	Note 11	ns
62	Maximum delay from write data strobe deassertion to host request deassertion for "Last Data Register" write[5,8,10]	$(3.0 \times T_{HCLK}) + 8.0$	Note 11	$(3.0 \times T_{CORE}) + 6.0$	Note 11	ns
63	Minimum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) deassertion to HREQ assertion.	$(2.0 \times T_{HCLK}) + 1.0$	Note 11	$(2.0 \times T_{CORE}) + 1.0$	Note 11	ns
64	Maximum delay from DMA HACK (OAD=0) or Read/Write data strobe(OAD=1) assertion to HREQ deassertion	$(5.0 \times T_{HCLK}) + 8.0$	Note 11	$(5.0 \times T_{CORE}) + 6.0$	Note 11	ns

Table 2-21. Host Interface (HDI16) Timing[1, 2] (Continued)

No.	Characteristics[3]	Mask Set 1L44X		Mask Set 1M88B		Unit
		Expression	Value	Expression	Value	

Notes:
1. T_{HCLK} = 2/ (Core Clock). At 200 MHz, T_{HCLK} = 10 ns. T_{CORE} = core clock period. At 266 MHz, T_{CORE} = 3.75 ns.
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. V_{DD} = 3.3 V ± 0.15 V; T_J = –40°C to +105 °C, C_L = 30 pF for maximum delay timings and C_L = 0 pF for minimum delay timings.
4. The read data strobe is $\overline{\text{HRD}}$/HRD in the dual data strobe mode and $\overline{\text{HDS}}$/HDS in the single data strobe mode.
5. For 64-bit transfers, The “last data register” is the register at address 0x7, which is the last location to be read or written in data transfers. This is RX0/TX0 in the little endian mode (HBE = 0), or RX3/TX3 in the big endian mode (HBE = 1).
6. This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the $\overline{\text{HREQ}}$/HREQ signal.
7. This timing is applicable only if two consecutive reads from one of these registers are executed.
8. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
9. The data strobe is host read ($\overline{\text{HRD}}$/HRD) or host write ($\overline{\text{HWR}}$/HWR) in the dual data strobe mode and host data strobe ($\overline{\text{HDS}}$/HDS) in the single data strobe mode.
10. The host request is $\overline{\text{HREQ}}$/HREQ in the single host request mode and $\overline{\text{HRRQ}}$/HRRQ and $\overline{\text{HTRQ}}$/HTRQ in the double host request mode. $\overline{\text{HRRQ}}$/HRRQ is deasserted only when HOTX fifo is empty, $\overline{\text{HTRQ}}$/HTRQ is deasserted only if HORX fifo is full (treat as level Host Request).
11. Compute the value using the expression.
12. For mask set 1M88B, the read and write data strobe minimum deassertion width for non-”last data register” accesses in single and dual data strobe modes is based on timings 57 and 58.

Figure 2-7 and **Figure 2-8** show HDI16 read signal timing. **Figure 2-9** and **Figure 2-10** show HDI16 write signal timing.

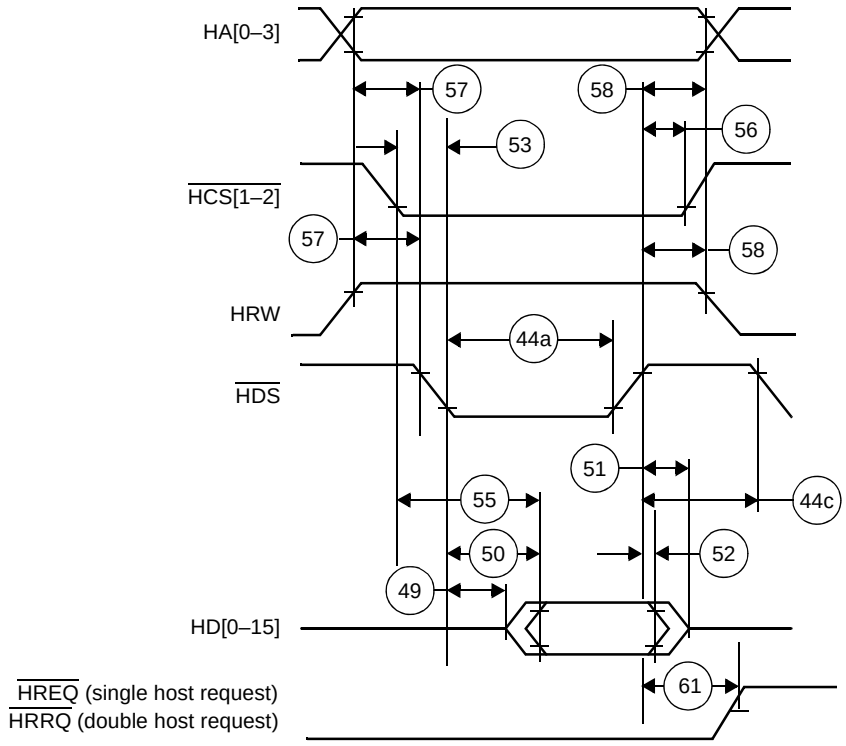


Figure 2-7. Read Timing Diagram, Single Data Strobe

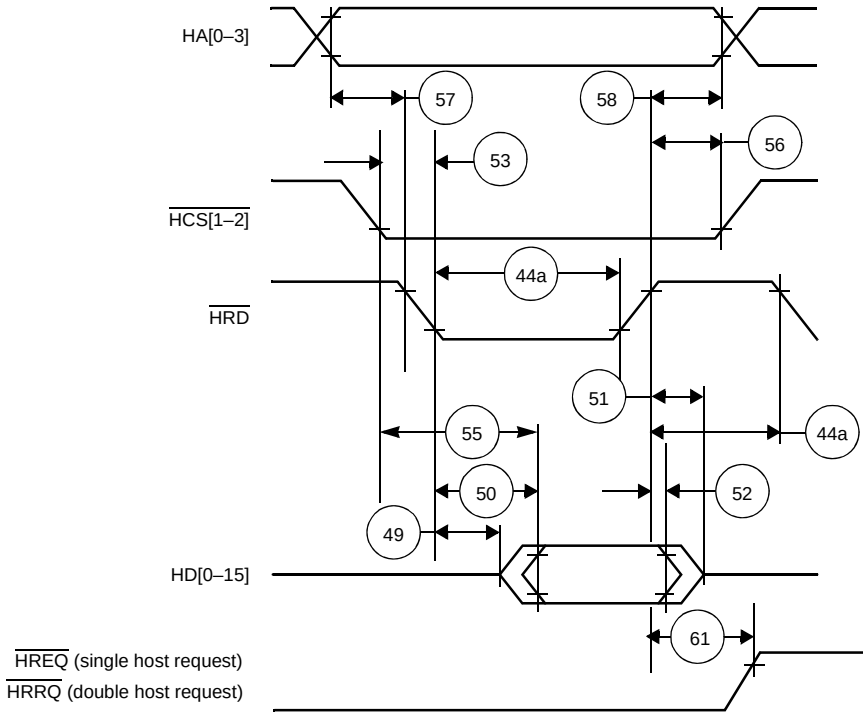


Figure 2-8. Read Timing Diagram, Double Data Strobe

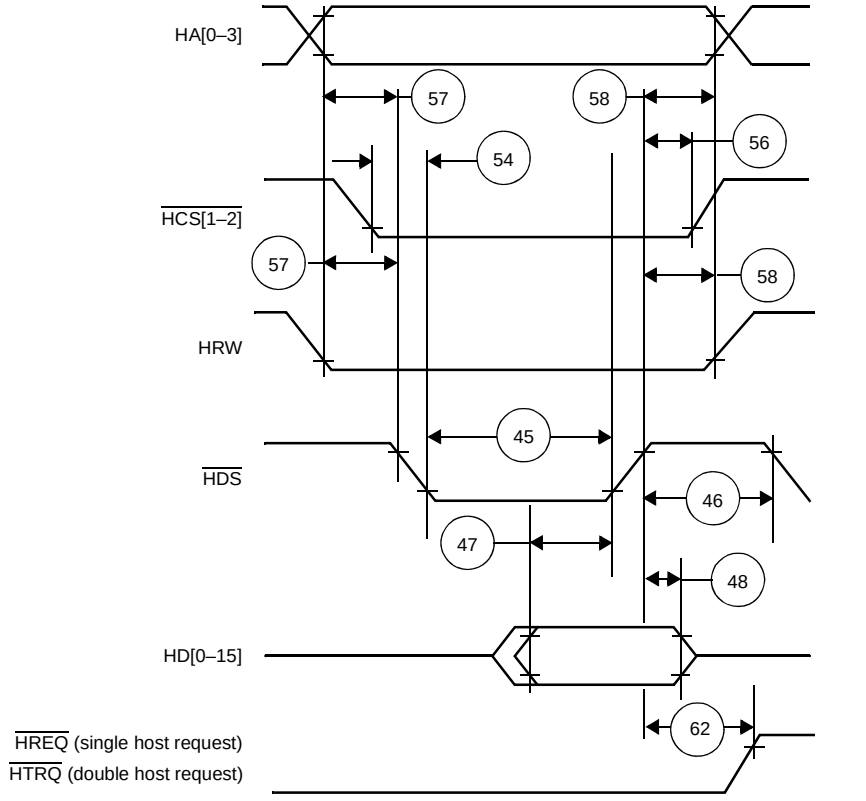


Figure 2-9. Write Timing Diagram, Single Data Strobe

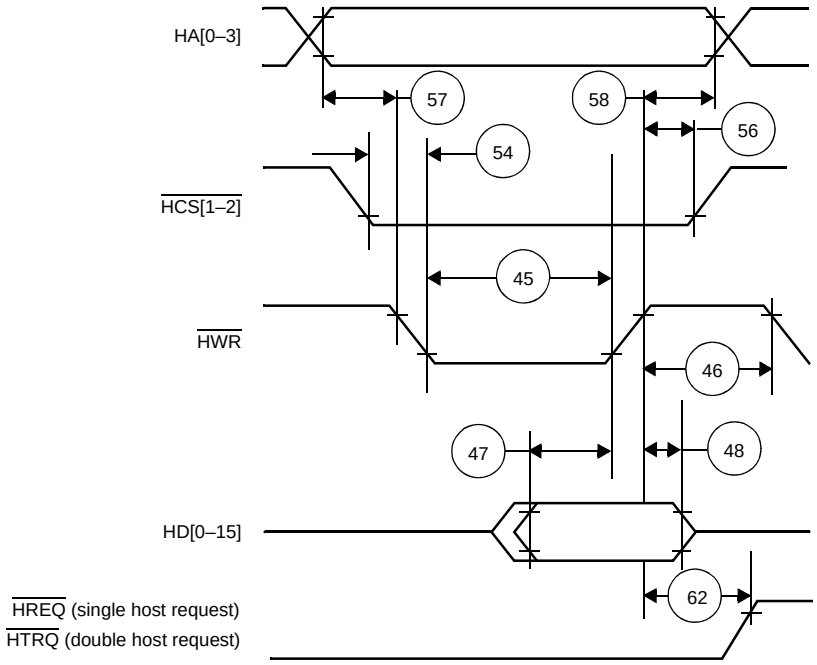


Figure 2-10. Write Timing Diagram, Double Data Strobe

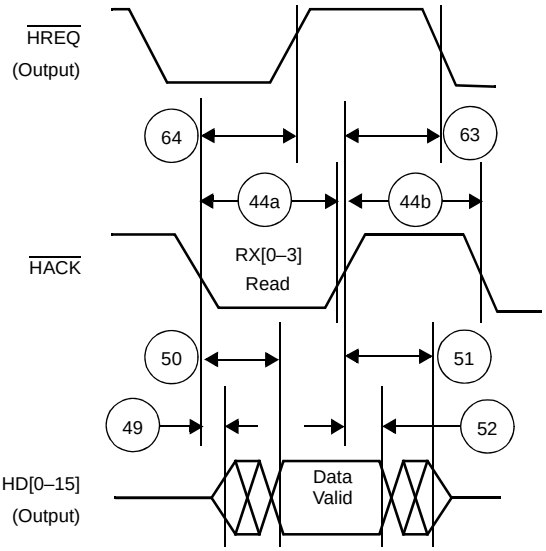


Figure 2-11. Host DMA Read Timing Diagram, HPCR[OAD] = 0

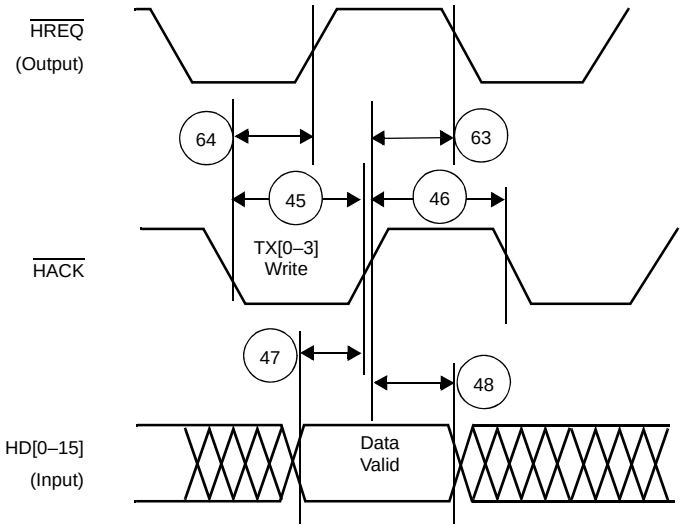


Figure 2-12. Host DMA Write Timing Diagram, HPCR[OAD] = 0

2.5.7 I²C Timing

Table 2-22. I²C Timing

No.	Characteristic	Fast		Unit
		Min	Max	
450	SCL clock frequency	0	400	kHz
451	Hold time START condition	(Clock period/2) – 0.3	—	µs
452	SCL low period	(Clock period/2) – 0.3	—	µs
453	SCL high period	(Clock period/2) – 0.1	—	µs
454	Repeated START set-up time (not shown in figure)	$2 \times 1/F_{BCK}$	—	µs
455	Data hold time	0	—	µs
456	Data set-up time	250	—	ns
457	SDA and SCL rise time	—	700	ns
458	SDA and SCL fall time	—	300	ns
459	Set-up time for STOP	(Clock period/2) – 0.7	—	µs
460	Bus free time between STOP and START	(Clock period/2) – 0.3	—	µs
Note:	SDA set-up time is referenced to the rising edge of SCL. SDA hold time is referenced to the falling edge of SCL. Load capacitance on SDA and SCL is 400 pF.			

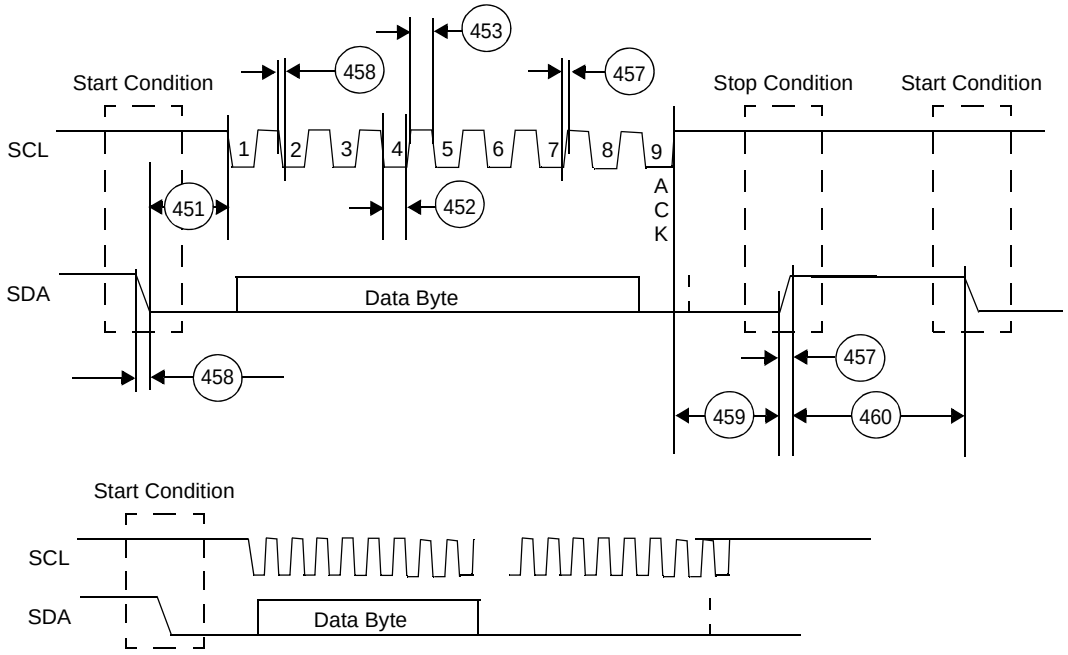


Figure 2-13. I^2C Timing Diagram

2.5.8 UART Timing

Table 2-23. UART Timing

No.	Characteristics	Expression	Mask Set 1L44X		Mask Set 1M88B		Unit
			Min	Max	Min	Max	
—	Internal bus clock (APBCLK)	$F_{CORE}/2$	—	100	—	133	MHz
—	Internal bus clock period (1/APBCLK)	T_{APBCLK}	10.0	—	7.52	—	ns
400	URXD and UTXD inputs high/low duration	$16 \times T_{APBCLK}$	160.0	—	120.3	—	ns
401	URXD and UTXD inputs rise/fall time		—	5	—	5	ns
402	UTXD output rise/fall time		—	5	—	5	ns

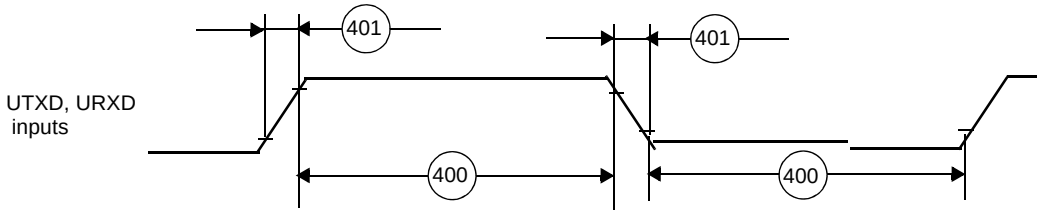


Figure 2-14. UART Input Timing

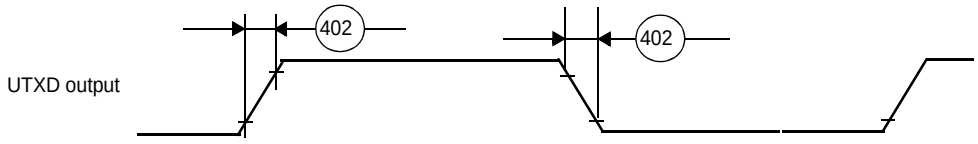


Figure 2-15. UART Output Timing

2.5.9 EE Timing

Table 2-24. EE0 Timing

Number	Characteristics	Type	Min
65	EE0 input to the core	Asynchronous	4 core clock periods
66	EE0 output from the core	Synchronous to core clock	1 core clock period

Notes:
1. The core clock is the SC1400 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Configure the direction of the EE pin in the EE_CTRL register (see the *SC1400 Core Reference Manual* for details.
3. Refer to **Table 1-12** for details on EE pin functionality.

Figure 2-17 shows the signal behavior of the EE pin.

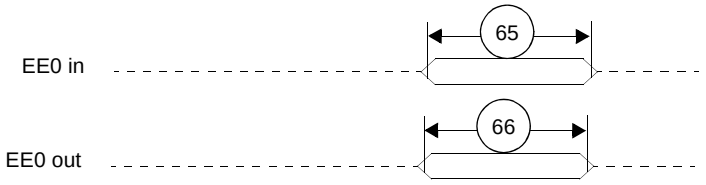


Figure 2-16. EE Pin Timing

2.5.10 Event Timing

Table 2-25. EVNT Signal Timing

Number	Characteristics	Type	Min
67	EVNT as input	Asynchronous	1.5 × APBCLK periods
68	EVNT as output	Synchronous to core clock	1 APBCLK period

Notes:
1. Refer to **Table 2-23** for a definition of the APBCLK period.
2. Direction of the EVNT signal is configured through the GPIO and Event port registers.
3. Refer to **Table 1-10** on page 1-12 for details on EVNT pin functionality.

Figure 2-17 shows the signal behavior of the EVNT pin.

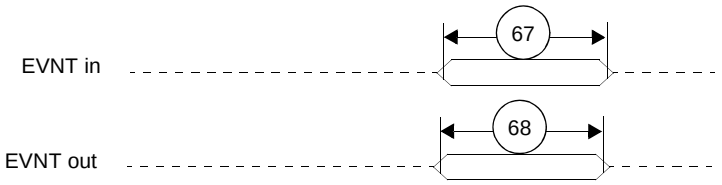


Figure 2-17. EVNT Pin Timing

2.5.11 GPIO Timing

Table 2-26. GPIO Signal Timing[1,2,3]

Number	Characteristics	Type	Min
601	GPI[4.5]	Asynchronous	1.5 × APBCLK periods
602	GPO[5]	Synchronous to core clock	1 APBCLK period
603	Port A edge-sensitive interrupt	Asynchronous	1.5 × APBCLK periods
604	Port A level-sensitive interrupt	Asynchronous	3 × APBCLK periods[6]

Notes:
1. Refer to **Table 2-23** for a definition of the APBCLK period.
2. Direction of the GPIO signal is configured through the GPIO port registers.
3. Refer to **Table 1-12** on page 1-14 for details on GPIO pin functionality.
4. GPI data is synchronized to the APBCLK internally and the minimum listed is the capability of the hardware to capture data into a register when the GPA_DR is read. The specification is not tested due to the asynchronous nature of the input and dependence on the state of the DSP core. It is guaranteed by design.
5. The input and output signals cannot toggle faster than 50 MHz.
6. Level-sensitive interrupts should be held low until the system determines (via the service routine) that the interrupt is acknowledged.

Figure 2-18 shows the signal behavior of the GPI/GPO pin.

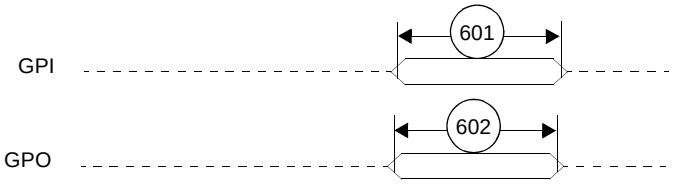


Figure 2-18. GPI/GPO Pin Timing

2.5.12 JTAG Signals

Table 2-27. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
700	TCK frequency of operation (1/($T_C \times 3$); maximum 22 MHz)	0.0	40.0	MHz
701	TCK cycle time	25.0	—	ns
702	TCK clock pulse width measured at V_M = 1.6 V	11.0	—	ns
703	TCK rise and fall times	0.0	3.0	ns
704	Boundary scan input data set-up time	5.0	—	ns
705	Boundary scan input data hold time	14.0	—	ns
706	TCK low to output data valid	0.0	20.0	ns
707	TCK low to output high impedance	0.0	20.0	ns
708	TMS, TDI data set-up time	5.0	—	ns
709	TMS, TDI data hold time	25.0	—	ns
710	TCK low to TDO data valid	0.0	24.0	ns
711	TCK low to TDO high impedance	0.0	10.0	ns
712	$\overline{\text{TRST}}$ assert time	100.0	—	ns
Note:	All timings apply to OCE module data transfers as the OCE module uses the JTAG port as an interface.			

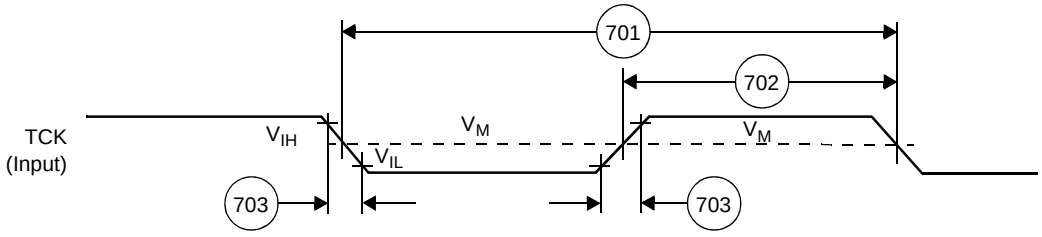


Figure 2-19. Test Clock Input Timing Diagram

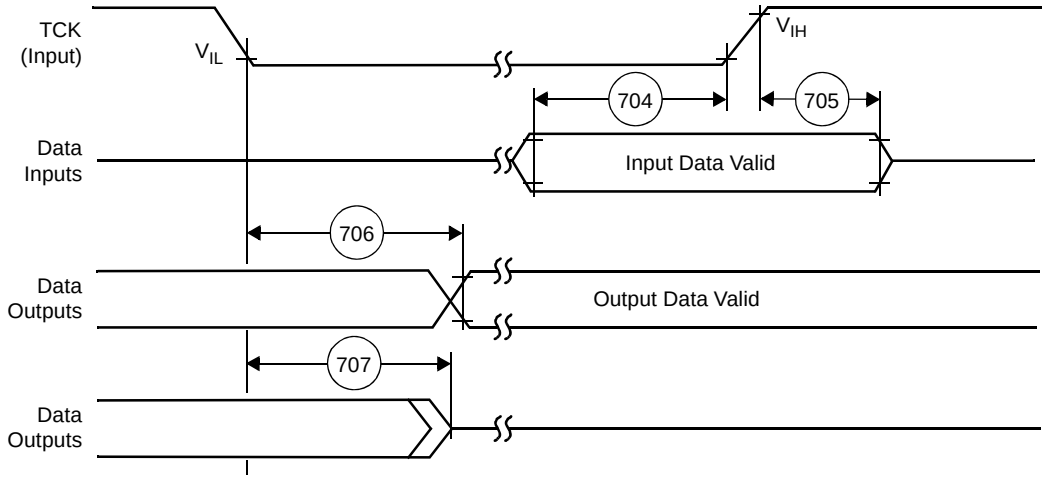


Figure 2-20. Boundary Scan (JTAG) Timing Diagram

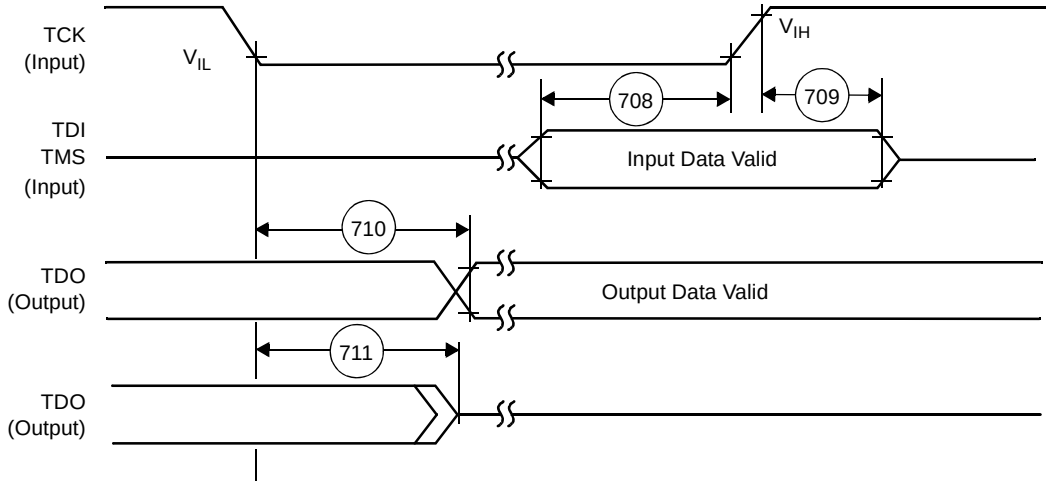


Figure 2-21. Test Access Port Timing Diagram

Figure 2-22. $\overline{\text{TRST}}$ Timing Diagram

Packaging 3

This section on the MSC7115 package includes diagrams of the package ball layout and tables showing how the signals discussed in **Chapter 1** are allocated. The MSC7115 is available in a 400-pin molded array process-ball grid array (MAP-BGA) package with either lead-free or lead-bearing solder spheres.

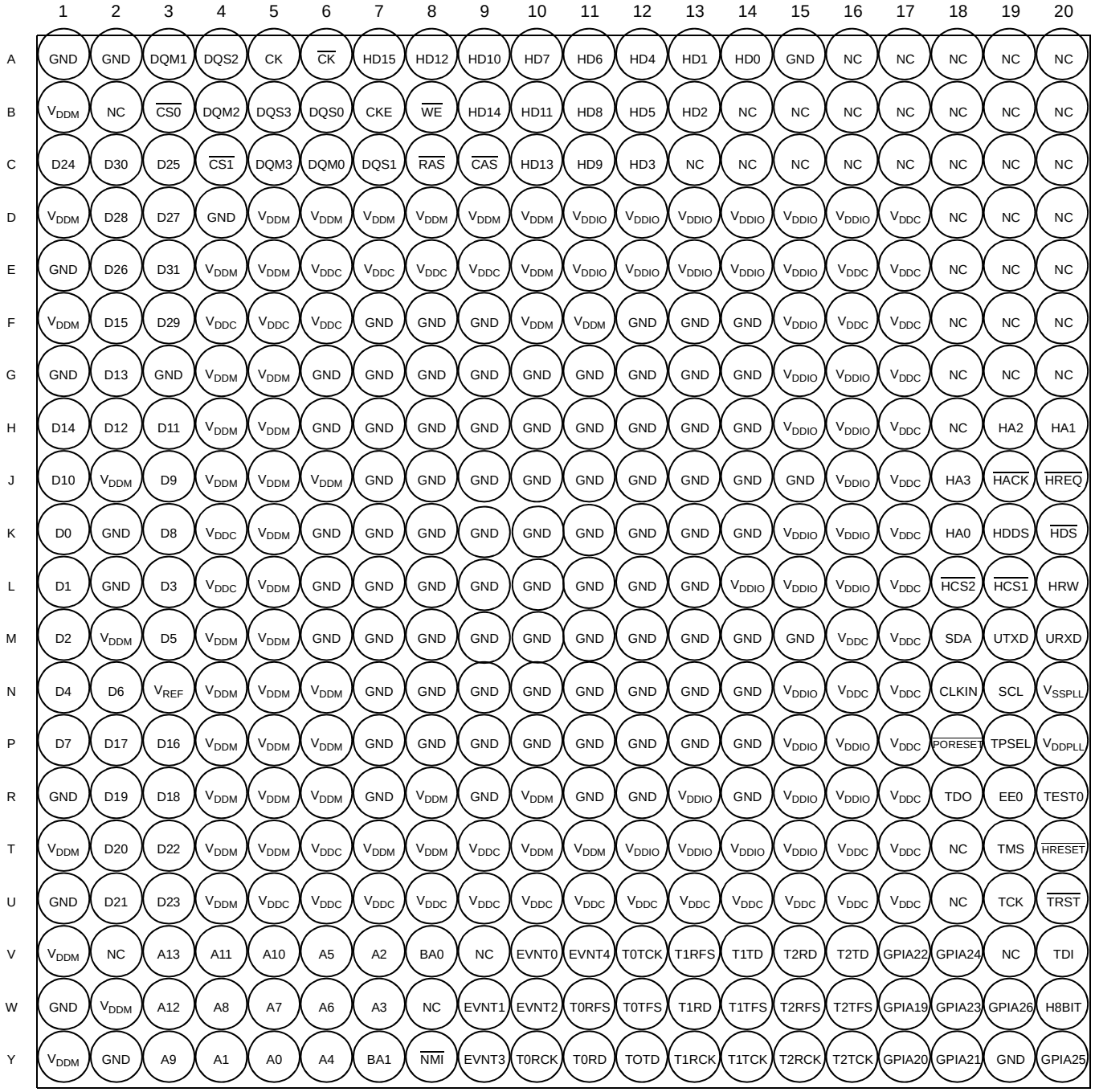
Note: See *Lead-Free BGA Solder Joint Assembly Evaluation* (EB635) for manufacturing and assembly guidelines.

3.1 MAP-BGA Package

Figure 3-1 and **Figure 3-2** show top and bottom views of the MAP-BGA package, including ball location. Signal names shown in the figures represent the only signal assigned to the location or, for multiplexed signals, the primary hardware-controlled option. Signals used only during power-on reset (SWTE, HDSP, and BM[0–1]) are not shown in these figures.

Table 3-1 lists the MSC7115 signals alphabetically by signal name. Connections with multiple names are listed individually by each name. Signals with programmable polarity are shown both as asserted low (default) and high (that is, $\overline{\text{NAME}}$/NAME). **Table 3-2** lists the signals numerically by pin number. Each pin number is listed once with the various signals that are multiplexed to it categorized by the configuration or state that defines the signal. Four host interface signals have alternate functions (single or double host request and single or double data strobe) that are configured by the host interface registers.

Top View



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	DQM1	DQS2	CK	$\overline{CK}$	HD15	HD12	HD10	HD7	HD6	HD4	HD1	HD0	GND	NC	NC	NC	NC	NC
B	V_{DDM}	NC	$\overline{CS0}$	DQM2	DQS3	DQS0	CKE	$\overline{WE}$	HD14	HD11	HD8	HD5	HD2	NC	NC	NC	NC	NC	NC	NC
C	D24	D30	D25	$\overline{CS1}$	DQM3	DQM0	DQS1	$\overline{RAS}$	$\overline{CAS}$	HD13	HD9	HD3	NC	NC	NC	NC	NC	NC	NC	NC
D	V_{DDM}	D28	D27	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	NC	NC
E	GND	D26	D31	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	V_{DDC}	NC	NC	NC
F	V_{DDM}	D15	D29	V_{DDC}	V_{DDC}	V_{DDC}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DDIO}	V_{DDC}	V_{DDC}	NC	NC	NC
G	GND	D13	GND	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	NC	NC
H	D14	D12	D11	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	HA2	HA1
J	D10	V_{DDM}	D9	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDC}	HA3	$\overline{HACK}$	$\overline{HREQ}$
K	D0	GND	D8	V_{DDC}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	HA0	HDDS	$\overline{HDS}$
L	D1	GND	D3	V_{DDC}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	$\overline{HCS2}$	$\overline{HCS1}$	HRW
M	D2	V_{DDM}	D5	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDC}	V_{DDC}	SDA	UTXD	URXD
N	D4	D6	V_{REF}	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDC}	V_{DDC}	CLKIN	SCL	V_{SSPLL}
P	D7	D17	D16	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	$\overline{PORESET}$	TPSEL	V_{DDPLL}
R	GND	D19	D18	V_{DDM}	V_{DDM}	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	GND	GND	V_{DDIO}	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	TDO	EE0	TEST0
T	V_{DDM}	D20	D22	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDM}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	V_{DDC}	NC	TMS	$\overline{HRESET}$
U	GND	D21	D23	V_{DDM}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	NC	TCK	$\overline{TRST}$
V	V_{DDM}	NC	A13	A11	A10	A5	A2	BA0	NC	EVNT0	EVNT4	T0TCK	T1RFS	T1TD	T2RD	T2TD	GPIA22	GPIA24	NC	TDI
W	GND	V_{DDM}	A12	A8	A7	A6	A3	NC	EVNT1	EVNT2	T0RFS	T0TFS	T1RD	T1TFS	T2RFS	T2TFS	GPIA19	GPIA23	GPIA26	H8BIT
Y	V_{DDM}	GND	A9	A1	A0	A4	BA1	$\overline{NMI}$	EVNT3	T0RCK	T0RD	TOTD	T1RCK	T1TCK	T2RCK	T2TCK	GPIA20	GPIA21	GND	GPIA25

Figure 3-1. MSC7115 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

Bottom View

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	NC	NC	NC	NC	NC	GND	HD0	HD1	HD4	HD6	HD7	HD10	HD12	HD15	$\overline{CK}$	CK	DQS2	DQM1	GND	GND
B	NC	NC	NC	NC	NC	NC	NC	HD2	HD5	HD8	HD11	HD14	$\overline{WE}$	CKE	DQS0	DQS3	DQM2	$\overline{CS0}$	NC	V_{DDM}
C	NC	NC	NC	NC	NC	NC	NC	NC	HD3	HD9	HD13	$\overline{CAS}$	$\overline{RAS}$	DQS1	DQM0	DQM3	$\overline{CS1}$	D25	D30	D24
D	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	GND	D27	D28	V_{DDM}
E	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	V_{DDM}	D31	D26	GND
F	NC	NC	NC	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DD}	V_{DD}	V_{DD}	D29	D15	V_{DDM}
G	NC	NC	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	GND	D13	GND
H	HA1	HA2	NC	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D11	D12	D14
J	$\overline{HREQ}$	$\overline{HACK}$	HA3	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D9	V_{DDM}	D10
K	$\overline{HDS}$	HDDS	HA0	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D8	GND	D0
L	HRW	$\overline{HCS1}$	$\overline{HCS2}$	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DD}	D3	GND	D1
M	URXD	UTXD	SDA	V_{DD}	V_{DD}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	D5	V_{DDM}	D2
N	V_{SSPLL}	SCL	CLKIN	V_{DD}	V_{DD}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{REF}	D6	D4
P	V_{DDPLL}	TPSEL	$\overline{PORESET}$	V_{DD}	V_{DDIO}	V_{DDIO}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDM}	V_{DDM}	V_{DDM}	D16	D17	D7
R	TEST0	EE0	TDO	V_{DD}	V_{DDIO}	V_{DDIO}	GND	V_{DDIO}	GND	GND	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	V_{DDM}	V_{DDM}	D18	D19	GND
T	$\overline{HRESET}$	TMS	NC	V_{DD}	V_{DD}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	V_{DD}	V_{DDM}	V_{DDM}	D22	D20	V_{DDM}
U	$\overline{TRST}$	TCK	NC	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DDM}	D23	D21	GND
V	TDI	NC	GPIA24	GPIA22	T2TD	T2RD	T1TD	T1RFS	T0TCK	EVNT4	EVNT0	NC	BA0	A2	A5	A10	A11	A13	NC	V_{DDM}
W	H8BIT	GPIA26	GPIA23	GPIA19	T2TFS	T2RFS	T1TFS	T1RD	T0TFS	T0RFS	EVNT2	EVNT1	NC	A3	A6	A7	A8	A12	V_{DDM}	GND
Y	GPIA25	GND	GPIA21	GPIA20	T2TCK	T2RCK	T1TCK	T1RCK	TOTD	T0RD	T0RCK	EVNT3	$\overline{NMI}$	BA1	A4	A0	A1	A9	GND	V_{DDM}

Figure 3-2. MSC7115 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

Table 3-1. MSC7115 Signals By Name

Signal Name	Ball Designator
A0	Y5
A1	Y4
A2	V7
A3	W7
A4	Y6
A5	V6
A6	W6
A7	W5
A8	W4
A9	Y3
A10	V5
A11	V4
A12	W3
A13	V3
BA0	V8
BA1	Y7
BM0	W10
BM1	Y9
BM2 (mask set 1M88B only)	B15
BM3 (mask set 1M88B only)	A16
$\overline{\text{CAS}}$	C9
CK	A5
$\overline{\text{CK}}$	A6
CKE	B7
CLKIN	N18
CLKO	W9
$\overline{\text{CS0}}$	B3
$\overline{\text{CS1}}$	C4
D0	K1
D1	L1
D2	M1
D3	L3
D4	N1
D5	M3
D6	N2
D7	P1
D8	K3
D9	J3
D10	J1

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
D11	H3
D12	H2
D13	G2
D14	H1
D15	F2
D16	P3
D17	P2
D18	R3
D19	R2
D20	T2
D21	U2
D22	T3
D23	U3
D24	C1
D25	C3
D26	E2
D27	D3
D28	D2
D29	F3
D30	C2
D31	E3
DBREQ	R19
DQM0	C6
DQM1	A3
DQM2	B4
DQM3	C5
DQS0	B6
DQS1	C7
DQS2	A4
DQS3	B5
EE0	R19
EVNT0	V10
EVNT1	W9
EVNT2	W10
EVNT3	Y9
EVNT4	V11
GND	A1
GND	A2
GND	A15

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
GND	D4
GND	E1
GND	F7
GND	F8
GND	F9
GND	F12
GND	F13
GND	F14
GND	G1
GND	G3
GND	G6
GND	G7
GND	G8
GND	G9
GND	G10
GND	G11
GND	G12
GND	G13
GND	G14
GND	H6
GND	H7
GND	H8
GND	H9
GND	H10
GND	H11
GND	H12
GND	H13
GND	H14
GND	J7
GND	J8
GND	J9
GND	J10
GND	J11
GND	J12
GND	J13
GND	J14
GND	J15
GND	K2
GND	K6

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
GND	K7
GND	K8
GND	K9
GND	K10
GND	K11
GND	K12
GND	K13
GND	K14
GND	L2
GND	L6
GND	L7
GND	L8
GND	L9
GND	L10
GND	L11
GND	L12
GND	L13
GND	M6
GND	M7
GND	M8
GND	M9
GND	M10
GND	M11
GND	M12
GND	M13
GND	M14
GND	M15
GND	N7
GND	N8
GND	N9
GND	N10
GND	N11
GND	N12
GND	N13
GND	N14
GND	P7
GND	P8
GND	P9
GND	P10

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
GND	P11
GND	P12
GND	P13
GND	P14
GND	R1
GND	R7
GND	R9
GND	R11
GND	R12
GND	R14
GND	U1
GND	W1
GND	Y2
GND	Y19
GPIA0	V14
GPIA1	W14
GPIA2	Y14
GPIA3	W13
GPIA4	V13
GPIA5	Y13
GPIA6	Y12
GPIA7	W12
GPIA8	V12
GPIA9	Y11
GPIA10	W11
GPIA11	Y10
GPIA12	M19
GPIA13	M20
GPIA14	M18
GPIA15	N19
GPIA16	V11
GPIA17	W9
GPIA19	W17
GPIA20	Y17
GPIA21	Y18
GPIA22	V17
GPIA23	W18
GPIA24	V18
GPIA25	Y20

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
GPIA26	W19
GPIA27	W16
GPIA28	V15
GPIA29	Y15
GPIB11 (mask set 1M88B only)	L18
GPIC0	B11
GPIC1	C11
GPIC2	A9
GPIC3	B10
GPIC4	A8
GPIC5	C10
GPIC6	B9
GPIC7	A7
GPIC11 (mask set 1M88B only)	J18
GPIC14	W10
GPIC15	Y9
GPID4	W15
GPID5	Y16
GPID6	V16
GPID7 (mask set 1M88B only)	B15
GPID8 (mask set 1M88B only)	A16
GPOA0	V14
GPOA1	W14
GPOA2	Y14
GPOA3	W13
GPOA4	V13
GPOA5	Y13
GPOA6	Y12
GPOA7	W12
GPOA8	V12
GPOA9	Y11
GPOA10	W11
GPOA11	Y10
GPOA12	M19
GPOA13	M20
GPOA14	M18
GPOA15	N19
GPOA16	V11
GPOA17	W9

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
GPOA19	W17
GPOA20	Y17
GPOA21	Y18
GPOA22	V17
GPOA23	W18
GPOA24	V18
GPOA25	Y20
GPOA26	W19
GPOA27	W16
GPOA28	V15
GPOA29	Y15
GPOB11 (mask set 1M88B only)	L18
GPOC0	B11
GPOC1	C11
GPOC2	A9
GPOC3	B10
GPOC4	A8
GPOC5	C10
GPOC6	B9
GPOC7	A7
GPOC11 (mask set 1M88B only)	J18
GPOC14	W10
GPOC15	Y9
GPOD4	W15
GPOD5	Y16
GPOD6	V16
GPOD7 (mask set 1M88B only)	B15
GPOD8 (mask set 1M88B only)	A16
H8BIT	W20
HA0	K18
HA1	H20
HA2	H19
HA3	J18
$\overline{\text{HACK}}$/HACK	J19
$\overline{\text{HCS1}}$/HCS1	L19
$\overline{\text{HCS2}}$/HCS2	L18
HD0	A14
HD1	A13
HD10	A9

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
HD11	B10
HD12	A8
HD13	C10
HD14	B9
HD15	A7
HD2	B13
HD3	C12
HD4	A12
HD5	B12
HD6	A11
HD7	A10
HD8	B11
HD9	C11
HDDS	K19
$\overline{\text{HDS}}$/HDS	K20
HDSP	J20
$\overline{\text{HRD}}$/HRD	L20
$\overline{\text{HREQ}}$/HREQ	J20
$\overline{\text{HRESET}}$	T20
$\overline{\text{HRRQ}}$/HRRQ	J19
HRW	L20
$\overline{\text{HTRQ}}$/HTRQ	J20
$\overline{\text{HWR}}$/HWR	K20
$\overline{\text{IRQ0}}$	Y13
$\overline{\text{IRQ1}}$	V13
$\overline{\text{IRQ10}}$	W14
$\overline{\text{IRQ11}}$	V14
$\overline{\text{IRQ12}}$	V11
$\overline{\text{IRQ13}}$	W9
$\overline{\text{IRQ14}}$	N19
$\overline{\text{IRQ15}}$	M18
$\overline{\text{IRQ16}}$	Y15
$\overline{\text{IRQ17}}$	V15
$\overline{\text{IRQ18}}$	W16
$\overline{\text{IRQ19}}$	W17
$\overline{\text{IRQ2}}$	M20
$\overline{\text{IRQ20}}$	Y17
$\overline{\text{IRQ21}}$	Y18
$\overline{\text{IRQ22}}$	V17

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
$\overline{\text{IRQ23}}$	W18
$\overline{\text{IRQ24}}$	V18
$\overline{\text{IRQ25}}$	Y20
$\overline{\text{IRQ26}}$	W19
$\overline{\text{IRQ3}}$	M19
$\overline{\text{IRQ4}}$	Y10
$\overline{\text{IRQ5}}$	W11
$\overline{\text{IRQ6}}$	V12
$\overline{\text{IRQ7}}$	W12
$\overline{\text{IRQ8}}$	W13
$\overline{\text{IRQ9}}$	Y14
NC	A16
NC	A17
NC	A18
NC	A19
NC	A20
NC	B2
NC	B14
NC	B15
NC	B16
NC	B17
NC	B18
NC	B19
NC	B20
NC	C13
NC	C14
NC	C15
NC	C16
NC	C17
NC	C18
NC	C19
NC	C20
NC	D18
NC	D19
NC	D20
NC	E18
NC	E19
NC	E20
NC	F18

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
NC	F19
NC	F20
NC	G18
NC	G19
NC	G20
NC	H18
NC	T18
NC	U18
NC	V2
NC	V9
NC	V19
NC	W8
$\overline{\text{NMI}}$	Y8
$\overline{\text{PORESET}}$	P18
$\overline{\text{RAS}}$	C8
SCL	N19
SDA	M18
SWTE	V11
T0RCK	Y10
T0RD	Y11
T0RFS	W11
T0TCK	V12
T0TD	Y12
T0TFS	W12
T1RCK	Y13
T1RD	W13
T1RFS	V13
T1TCK	Y14
T1TD	V14
T1TFS	W14
T2RCK	Y15
T2RD	V15
T2RFS	W15
T2TCK	Y16
T2TD	V16
T2TFS	W16
TCK	U19
TDI	V20
TDO	R18

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
TEST0	R20
TMS	T19
TPSEL	P19
$\overline{\text{TRST}}$	U20
URXD	M20
UTXD	M19
V_{DDC}	D17
V_{DDC}	E6
V_{DDC}	E7
V_{DDC}	E8
V_{DDC}	E9
V_{DDC}	E16
V_{DDC}	E17
V_{DDC}	F4
V_{DDC}	F5
V_{DDC}	F6
V_{DDC}	F16
V_{DDC}	F17
V_{DDC}	G17
V_{DDC}	H17
V_{DDC}	J17
V_{DDC}	K4
V_{DDC}	K17
V_{DDC}	L4
V_{DDC}	L17
V_{DDC}	M16
V_{DDC}	M17
V_{DDC}	N16
V_{DDC}	N17
V_{DDC}	P17
V_{DDC}	R17
V_{DDC}	T6
V_{DDC}	T9
V_{DDC}	T16
V_{DDC}	T17
V_{DDC}	U5
V_{DDC}	U6
V_{DDC}	U7
V_{DDC}	U8

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
V_{DDC}	U9
V_{DDC}	U10
V_{DDC}	U11
V_{DDC}	U12
V_{DDC}	U13
V_{DDC}	U14
V_{DDC}	U15
V_{DDC}	U16
V_{DDC}	U17
V_{DDIO}	D11
V_{DDIO}	D12
V_{DDIO}	D13
V_{DDIO}	D14
V_{DDIO}	D15
V_{DDIO}	D16
V_{DDIO}	E11
V_{DDIO}	E12
V_{DDIO}	E13
V_{DDIO}	E14
V_{DDIO}	E15
V_{DDIO}	F15
V_{DDIO}	G15
V_{DDIO}	G16
V_{DDIO}	H15
V_{DDIO}	H16
V_{DDIO}	J16
V_{DDIO}	K15
V_{DDIO}	K16
V_{DDIO}	L14
V_{DDIO}	L15
V_{DDIO}	L16
V_{DDIO}	N15
V_{DDIO}	P15
V_{DDIO}	P16
V_{DDIO}	R13
V_{DDIO}	R15
V_{DDIO}	R16
V_{DDIO}	T12
V_{DDIO}	T13

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
V_{DDIO}	T14
V_{DDIO}	T15
V_{DDM}	B1
V_{DDM}	D1
V_{DDM}	D5
V_{DDM}	D6
V_{DDM}	D7
V_{DDM}	D8
V_{DDM}	D9
V_{DDM}	D10
V_{DDM}	E4
V_{DDM}	E5
V_{DDM}	E10
V_{DDM}	F1
V_{DDM}	F10
V_{DDM}	F11
V_{DDM}	G4
V_{DDM}	G5
V_{DDM}	H4
V_{DDM}	H5
V_{DDM}	J2
V_{DDM}	J4
V_{DDM}	J5
V_{DDM}	J6
V_{DDM}	K5
V_{DDM}	L5
V_{DDM}	M2
V_{DDM}	M4
V_{DDM}	M5
V_{DDM}	N4
V_{DDM}	N5
V_{DDM}	N6
V_{DDM}	P4
V_{DDM}	P5
V_{DDM}	P6
V_{DDM}	R4
V_{DDM}	R5
V_{DDM}	R6
V_{DDM}	R8

Table 3-1. MSC7115 Signals By Name (Continued)

Signal Name	Ball Designator
V_{DDM}	R10
V_{DDM}	T1
V_{DDM}	T4
V_{DDM}	T5
V_{DDM}	T7
V_{DDM}	T8
V_{DDM}	T10
V_{DDM}	T11
V_{DDM}	U4
V_{DDM}	V1
V_{DDM}	W2
V_{DDM}	Y1
V_{DDPLL}	P20
V_{REF}	N3
V_{SSPLL}	N20
$\overline{WE}$	B8

Notes:
1. This table lists every signal name. Because many signals are multiplexed, an individual ball designator number may be listed several times.
2. Signals listed as NC must not be connected or used as signal junction locations in board designs.
3. Many peripheral signals must be enabled before they can be used. Some signals are reserved after reset if they are not enabled. “Reserved” signals are not included in this list. Refer to **Table 3-2** to determine which signals must be enabled after reset.

Table 3-2. MSC7115 Signals by Ball Designator

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
A1	GND					
A2	GND					
A3	DQM1					
A4	DQS2					
A5	CK					
A6	$\overline{CK}$					
A7	GPIC7			GPOC7	HD15	
A8	GPIC4			GPOC4	HD12	
A9	GPIC2			GPOC2	HD10	
A10	reserved				HD7	
A11	reserved				HD6	
A12	reserved				HD4	
A13	reserved				HD1	
A14	reserved				HD0	
A15	GND					
A16 (1L44X)	NC					
A16 (1M88B)	BM3	GPID8		GPOD7	reserved	
A17	NC					
A18	NC					
A19	NC					
A20	NC					
B1	V_{DDM}					
B2	NC					
B3	$\overline{CS0}$					
B4	DQM2					
B5	DQS3					
B6	DQS0					
B7	CKE					
B8	$\overline{WE}$					
B9	GPIC6			GPOC6	HD14	
B10	GPIC3			GPOC3	HD11	
B11	GPIC0			GPOC0	HD8	
B12	reserved				HD5	
B13	reserved				HD2	
B14	NC					
B15 (1L44X)	NC					
B15 (1M88B)	BM2	GPID7		GPOD7	reserved	
B16	NC					

Table 3-2. MSC7115 Signals by Ball Designator (Continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
B17	NC					
B18	NC					
B19	NC					
B20	NC					
C1	D24					
C2	D30					
C3	D25					
C4	$\overline{CS1}$					
C5	DQM3					
C6	DQM0					
C7	DQS1					
C8	$\overline{RAS}$					
C9	$\overline{CAS}$					
C10	GPIC5			GPOC5	HD13	
C11	GPIC1			GPOC1	HD9	
C12	reserved				HD3	
C13	NC					
C14	NC					
C15	NC					
C16	NC					
C17	NC					
C18	NC					
C19	NC					
C20	NC					
D1	V_{DDM}					
D2	D28					
D3	D27					
D4	GND					
D5	V_{DDM}					
D6	V_{DDM}					
D7	V_{DDM}					
D8	V_{DDM}					
D9	V_{DDM}					
D10	V_{DDM}					
D11	V_{DDIO}					
D12	V_{DDIO}					
D13	V_{DDIO}					
D14	V_{DDIO}					

Table 3-2. MSC7115 Signals by Ball Designator (Continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
D15	V_{DDIO}					
D16	V_{DDIO}					
D17	V_{DDC}					
D18	NC					
D19	NC					
D20	NC					
E1	GND					
E2	D26					
E3	D31					
E4	V_{DDM}					
E5	V_{DDM}					
E6	V_{DDC}					
E7	V_{DDC}					
E8	V_{DDC}					
E9	V_{DDC}					
E10	V_{DDM}					
E11	V_{DDIO}					
E12	V_{DDIO}					
E13	V_{DDIO}					
E14	V_{DDIO}					
E15	V_{DDIO}					
E16	V_{DDC}					
E17	V_{DDC}					
E18	NC					
E19	NC					
E20	NC					
F1	V_{DDM}					
F2	D15					
F3	D29					
F4	V_{DDC}					
F5	V_{DDC}					
F6	V_{DDC}					
F7	GND					
F8	GND					
F9	GND					
F10	V_{DDM}					
F11	V_{DDM}					
F12	GND					

Table 3-2. MSC7115 Signals by Ball Designator (Continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
F13	GND					
F14	GND					
F15	V_{DDIO}					
F16	V_{DDC}					
F17	V_{DDC}					
F18	NC					
F19	NC					
F20	NC					
G1	GND					
G2	D13					
G3	GND					
G4	V_{DDM}					
G5	V_{DDM}					
G6	GND					
G7	GND					
G8	GND					
G9	GND					
G10	GND					
G11	GND					
G12	GND					
G13	GND					
G14	GND					
G15	V_{DDIO}					
G16	V_{DDIO}					
G17	V_{DDC}					
G18	NC					
G19	NC					
G20	NC					
H1	D14					
H2	D12					
H3	D11					
H4	V_{DDM}					
H5	V_{DDM}					
H6	GND					
H7	GND					
H8	GND					
H9	GND					
H10	GND					

Table 3-2. MSC7115 Signals by Ball Designator (Continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
H11	GND					
H12	GND					
H13	GND					
H14	GND					
H15	V_{DDIO}					
H16	V_{DDIO}					
H17	V_{DDC}					
H18	NC					
H19	reserved				HA2	
H20	reserved				HA1	
J1	D10					
J2	V_{DDM}					
J3	D9					
J4	V_{DDM}					
J5	V_{DDM}					
J6	V_{DDM}					
J7	GND					
J8	GND					
J9	GND					
J10	GND					
J11	GND					
J12	GND					
J13	GND					
J14	GND					
J15	GND					
J16	V_{DDIO}					
J17	V_{DDC}					
J18 (1L44X)	reserved				HA3	
J18 (1M88B)	GPIC11			GPOC11	HA3	
J19	reserved				$\overline{\text{HACK}}$/HACK or $\overline{\text{HRRQ}}$/HRRQ	
J20	HDSP	reserved			$\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ	
K1	D0					
K2	GND					
K3	D8					
K4	V_{DDC}					
K5	V_{DDM}					
K6	GND					
K7	GND					

Table 3-2. MSC7115 Signals by Ball Designator (Continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
K8	GND					
K9	GND					
K10	GND					
K11	GND					
K12	GND					
K13	GND					
K14	GND					
K15	V_{DDIO}					
K16	V_{DDIO}					
K17	V_{DDC}					
K18	reserved				HA0	
K19	reserved				HDDS	
K20	reserved				$\overline{\text{HDS}}$/HDS or $\overline{\text{HWR}}$/HWR	
L1	D1					
L2	GND					
L3	D3					
L4	V_{DDC}					
L5	V_{DDM}					
L6	GND					
L7	GND					
L8	GND					
L9	GND					
L10	GND					
L11	GND					
L12	GND					
L13	GND					
L14	V_{DDIO}					
L15	V_{DDIO}					
L16	V_{DDIO}					
L17	V_{DDC}					
L18 (1L44X)	reserved				$\overline{\text{HCS2}}$/HCS2	
L18 (1M88B)	GPIB11			GPOB11	$\overline{\text{HCS2}}$/HCS2	
L19	reserved				$\overline{\text{HCS1}}$/HCS1	
L20	reserved				HRW or $\overline{\text{HRD}}$/HRD	
M1	D2					
M2	V_{DDM}					
M3	D5					
M4	V_{DDM}					

Table 3-2. MSC7115 Signals by Ball Designator (Continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
M5	V_{DDM}					
M6	GND					
M7	GND					
M8	GND					
M9	GND					
M10	GND					
M11	GND					
M12	GND					
M13	GND					
M14	GND					
M15	GND					
M16	V_{DDC}					
M17	V_{DDC}					
M18	GPIA14		$\overline{IRQ15}$		GPOA14	SDA
M19	GPIA12		$\overline{IRQ3}$		GPOA12	UTXD
M20	GPIA13		$\overline{IRQ2}$		GPOA13	URXD
N1	D4					
N2	D6					
N3	V_{REF}					
N4	V_{DDM}					
N5	V_{DDM}					
N6	V_{DDM}					
N7	GND					
N8	GND					
N9	GND					
N10	GND					
N11	GND					
N12	GND					
N13	GND					
N14	GND					
N15	V_{DDIO}					
N16	V_{DDC}					
N17	V_{DDC}					
N18	CLKIN					
N19	GPIA15		$\overline{IRQ14}$		GPOA15	SCL
N20	V_{SSPLL}					
P1	D7					
P2	D17					

Table 3-2. MSC7115 Signals by Ball Designator (Continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
P3	D16					
P4	V_{DDM}					
P5	V_{DDM}					
P6	V_{DDM}					
P7	GND					
P8	GND					
P9	GND					
P10	GND					
P11	GND					
P12	GND					
P13	GND					
P14	GND					
P15	V_{DDIO}					
P16	V_{DDIO}					
P17	V_{DDC}					
P18	$\overline{\text{PORESET}}$					
P19	TPSEL					
P20	V_{DDPLL}					
R1	GND					
R2	D19					
R3	D18					
R4	V_{DDM}					
R5	V_{DDM}					
R6	V_{DDM}					
R7	GND					
R8	V_{DDM}					
R9	GND					
R10	V_{DDM}					
R11	GND					
R12	GND					
R13	V_{DDIO}					
R14	GND					
R15	V_{DDIO}					
R16	V_{DDIO}					
R17	V_{DDC}					
R18	TDO					
R19	reserved				EE0/DBREQ	
R20	TEST0					

Table 3-2. MSC7115 Signals by Ball Designator (Continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
T1	V_{DDM}					
T2	D20					
T3	D22					
T4	V_{DDM}					
T5	V_{DDM}					
T6	V_{DDC}					
T7	V_{DDM}					
T8	V_{DDM}					
T9	V_{DDC}					
T10	V_{DDM}					
T11	V_{DDM}					
T12	V_{DDIO}					
T13	V_{DDIO}					
T14	V_{DDIO}					
T15	V_{DDIO}					
T16	V_{DDC}					
T17	V_{DDC}					
T18	NC					
T19	TMS					
T20	$\overline{\text{HRESET}}$					
U1	GND					
U2	D21					
U3	D23					
U4	V_{DDM}					
U5	V_{DDC}					
U6	V_{DDC}					
U7	V_{DDC}					
U8	V_{DDC}					
U9	V_{DDC}					
U10	V_{DDC}					
U11	V_{DDC}					
U12	V_{DDC}					
U13	V_{DDC}					
U14	V_{DDC}					
U15	V_{DDC}					
U16	V_{DDC}					
U17	V_{DDC}					
U18	NC					

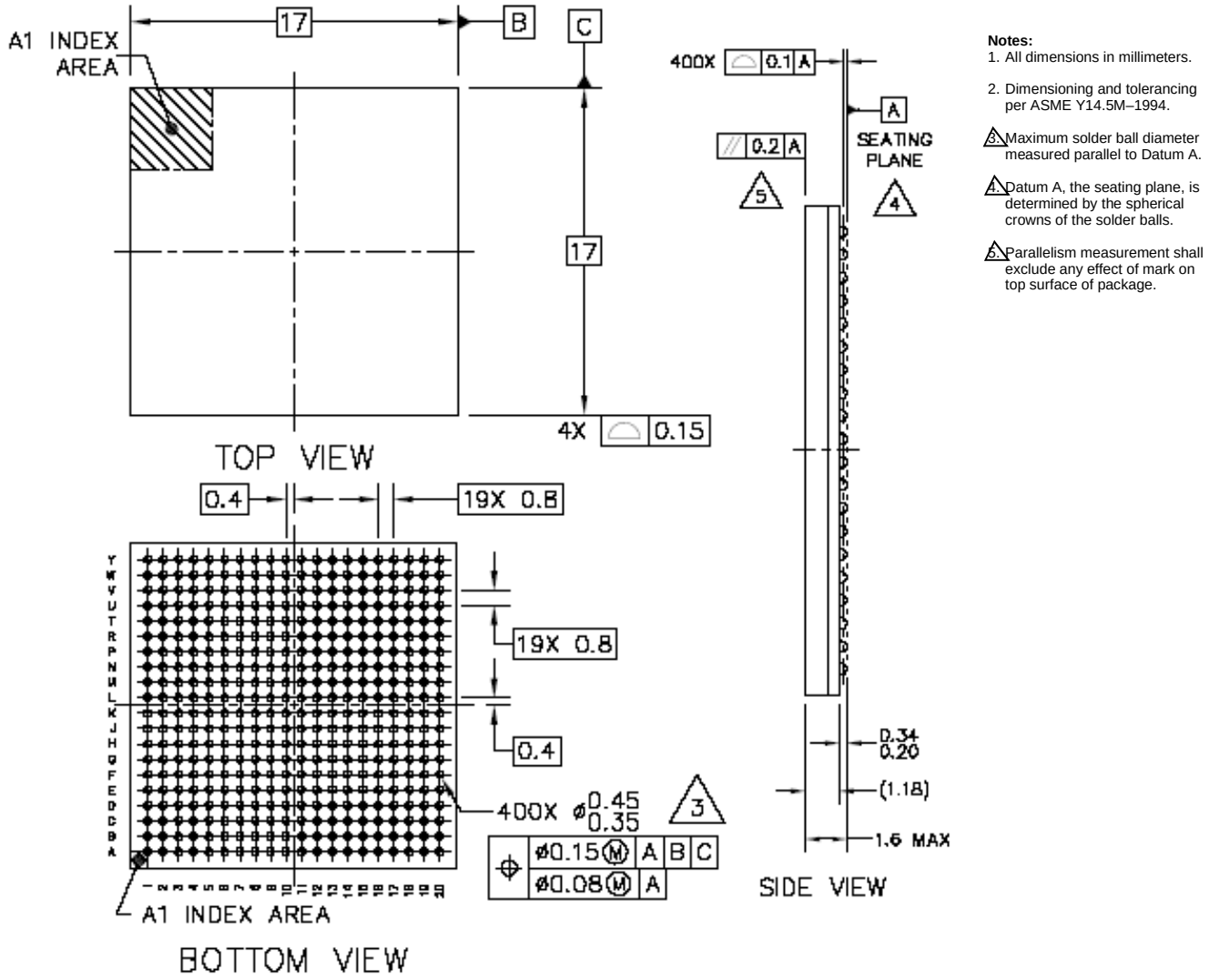
Table 3-2. MSC7115 Signals by Ball Designator (Continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
U19	TCK					
U20	$\overline{\text{TRST}}$					
V1	V_{DDM}					
V2	NC					
V3	A13					
V4	A11					
V5	A10					
V6	A5					
V7	A2					
V8	BA0					
V9	NC					
V10	reserved				EVNT0	
V11	SWTE	GPIA16	$\overline{\text{IRQ12}}$	GPOA16	EVNT4	
V12	GPIA8		$\overline{\text{IRQ6}}$	GPOA8	T0TCK	
V13	GPIA4		$\overline{\text{IRQ1}}$	GPOA4	T1RFS	
V14	GPIA0		$\overline{\text{IRQ11}}$	GPOA0	T1TD	
V15	GPIA28		$\overline{\text{IRQ17}}$	GPOA28	reserved	T2RD
V16	GPID6			GPOD6	reserved	T2TD
V17	GPIA22		$\overline{\text{IRQ22}}$	GPOA22	reserved	
V18	GPIA24		$\overline{\text{IRQ24}}$	GPOA24	reserved	
V19	NC					
V20	TDI					
W1	GND					
W2	V_{DDM}					
W3	A12					
W4	A8					
W5	A7					
W6	A6					
W7	A3					
W8	NC					
W9	GPIA17		$\overline{\text{IRQ13}}$	GPOA17	EVNT1	CLKO
W10	BM0	GPIC14		GPOC14	EVNT2	
W11	GPIA10		$\overline{\text{IRQ5}}$	GPOA10	T0RFS	
W12	GPIA7		$\overline{\text{IRQ7}}$	GPOA7	T0TFS	
W13	GPIA3		$\overline{\text{IRQ8}}$	GPOA3	T1RD	
W14	GPIA1		$\overline{\text{IRQ10}}$	GPOA1	T1TFS	
W15	GPID4			GPOD4	reserved	T2RFS
W16	GPIA27		$\overline{\text{IRQ18}}$	GPOA27	reserved	T2TFS

Table 3-2. MSC7115 Signals by Ball Designator (Continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
W17	GPIA19		$\overline{\text{IRQ19}}$	GPOA19	reserved	
W18	GPIA23		$\overline{\text{IRQ23}}$	GPOA23	reserved	
W19	GPIA26		$\overline{\text{IRQ26}}$	GPOA26	reserved	
W20	H8BIT	reserved				
Y1	V_{DDM}					
Y2	GND					
Y3	A9					
Y4	A1					
Y5	A0					
Y6	A4					
Y7	BA1					
Y8	reserved		$\overline{\text{NMI}}$	reserved		
Y9	BM1	GPIC15		GPOC15	EVNT3	
Y10	GPIA11		$\overline{\text{IRQ4}}$	GPOA11	T0RCK	
Y11	GPIA9			GPOA9	T0RD	
Y12	GPIA6			GPOA6	T0TD	
Y13	GPIA5		$\overline{\text{IRQ0}}$	GPOA5	T1RCK	
Y14	GPIA2		$\overline{\text{IRQ9}}$	GPOA2	T1TCK	
Y15	GPIA29		$\overline{\text{IRQ16}}$	GPOA29	reserved	T2RCK
Y16	GPID5			GPOD5	reserved	T2TCK
Y17	GPIA20		$\overline{\text{IRQ20}}$	GPOA20	reserved	
Y18	GPIA21		$\overline{\text{IRQ21}}$	GPOA21	reserved	
Y19	GND					
Y20	GPIA25		$\overline{\text{IRQ25}}$	GPOA25	reserved	

3.2 MAP-BGA Package Mechanical Drawing



CASE 1568-01

Figure 3-3. MSC7115 Mechanical Information, 400-pin MAP-BGA Package

Design Considerations 4

This section described various areas to consider when incorporating the MSC7115 device into a system design.

4.1 Thermal Design Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textbf{Equation 1}$$

where
T_A = ambient temperature near the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)
$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)
$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC7115 are listed in **Table 2-3**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip.

You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case. Use the following equation to determine T_J:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textbf{Equation 2}$$

where
T_T = thermocouple (or infrared) temperature on top of the package (°C)
Ψ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in the package (W)

4.2 Power Supply Design Considerations

This section outlines the MSC7115 power considerations: power supply, power sequencing, power planes, decoupling, power supply filtering, and power consumption. It also presents a recommended power supply design and options for low-power consumption. For information on AC/DC electrical specifications and thermal characteristics, refer to **Chapter 2**.

- *Power Supply*. The MSC7115 requires four input voltages, as shown in **Table 4-1**.

Table 4-1. MSC7115 Voltages

Voltage	Symbol	Value
Core	V_{DDC}	1.2 V
Memory	V_{DDM}	2.5 V
Reference	V_{REF}	1.25 V
I/O	V_{DDIO}	3.3 V

You should supply the MSC7115 core voltage via a variable switching supply or regulator to allow for compatibility with possible core voltage changes on future silicon revisions. The core voltage is supplied with 1.2 V (+5% and –10%) across V_{DDC} and GND and the I/O section is supplied with 3.3 V (± 10%) across V_{DDIO} and GND. The memory and reference voltages supply the DDR memory controller block. The memory voltage is supplied with 2.5 V across V_{DDM} and GND. The reference voltage is supplied across V_{REF} and GND and must be between $0.49 \times V_{DDM}$ and $0.51 \times V_{DDM}$. Refer to the JEDEC standard JESD8 (*Stub Series Terminated Logic for 2.5 Volts* (STTL_2)) for memory voltage supply requirements.

- *Power sequencing*. One consequence of multiple power supplies is that the voltage rails ramp up at different rates when power is initially applied. The rates depend on the power supply, the type of load on each power supply, and the way different voltages are derived. It is extremely important to observe the power up and power down sequences at the board level to avoid latch-up, forward biasing of ESD devices, and excessive currents, which all lead to severe device damage. The correct power-up sequence is as follows:
  - — Turn on the highest supply first (3.3 V).
  - — Turn on the 2.5 V supply.
  - — Turn on the lowest supply last (1.2 V).

  The correct power-down sequence is as follows:
  - — Turn off the lowest supply first (1.2 V).
  - — Turn off the 2.5 V supply.
  - — Turn off the highest supply last (3.3 V).

  At any instant during power-up and power-down, the 2.5 V supply must maintain a differential of +0.7 V or more below the 3.3 V supply. Also, at any instant, the 1.2 V supply must maintain a differential of +0.7 V or more below the 2.5 V supply, as shown in **Figure 4-1**. The power-down sequence is not as critical as the power-up sequence.

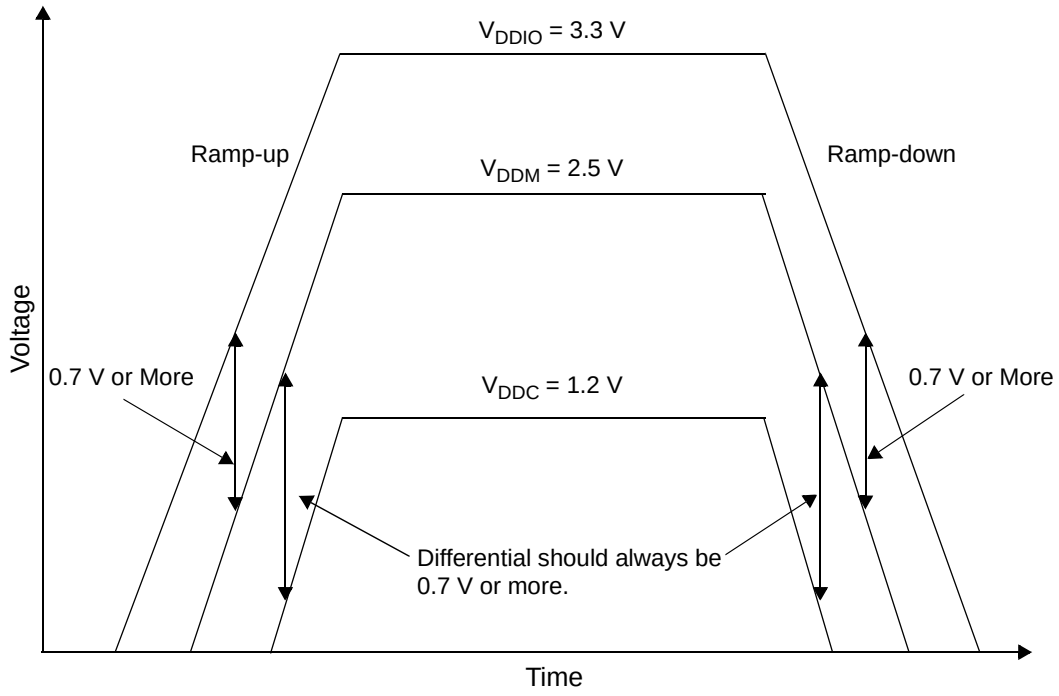


Figure 4-1. Voltage Sequencing

- *Power planes*. Each power supply pin (V_{DDC}, $V_{DDM,}$ and V_{DDIO}) should have a low-impedance path to the board power supply. Each GND pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on the device. The MSC7115 V_{DDC} power supply pins should be bypassed to ground using decoupling capacitors. The capacitor leads and associated printed circuit traces connecting to device power pins and GND should be kept to less than half an inch per capacitor lead. A minimum four-layer board that employs two inner layers as power and GND planes is recommended. See **Section 4.5** for DDR Controller power guidelines.
- *Decoupling.* Both the I/O voltage and core voltage should be decoupled for switching noise. For I/O decoupling, use standard capacitor values of 0.01 µF for every two to three voltage pins. For core voltage decoupling, use two levels of decoupling. The first level should consist of a 0.01 µF high frequency capacitor with low effective series resistance (ESR) and effective series inductance (ESL) for every two to three voltage pins. The second decoupling level should consist of two bulk/tantalum decoupling capacitors, one 10 µF and one 47 µF, (with low ESR and ESL) mounted as closely as possible to the MSC7115 voltage pins. Additionally, the maximum drop between the power supply and the DSP device should be 15 mV at 1 A.
- *PLL power supply filtering*. The MSC7115 V_{DDPLL} power signal provides power to the clock generation PLL. To ensure stability of the internal clock, the power supplied to this pin should be filtered with capacitors that have low and high frequency filtering characteristics. V_{DDPLL} can be connected to V_{DDC} through a 20 Ω resistor. V_{SSPLL} can be tied directly to the GND plane. A circuit similar to the one shown in **Figure 4-2** is recommended. The PLL loop filter should be placed as closely as possible to the V_{DDPLL} pin (which are located on the outside edge of the silicon package) to minimize noise coupled from nearby circuits.The 0.01 µF capacitor should be closest to V_{DDPLL}, followed by the 0.1 µF capacitor, the 10 µF capacitor, and finally the 20-Ω resistor to V_{DDC}. These traces should be kept short. V_{CCSYN} and V_{CCSYN1} should be bypassed to ground by 0.1 µF and 47 µF capacitors located as closely as possible to the device package.

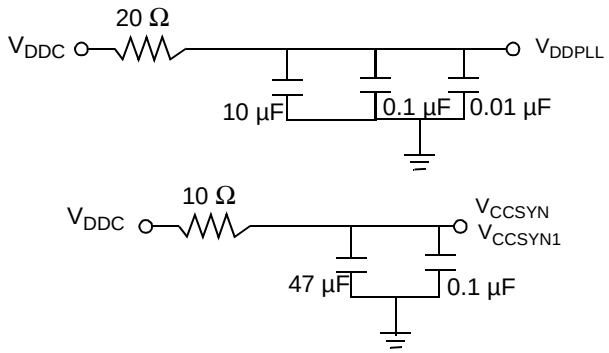


Figure 4-2. PLL Power Supply Filter Circuits

- *Power consumption.* You can reduce power consumption in your design by controlling the power consumption of the following regions of the device:
  - — *Extended core.* Use the SC1400 Stop and Wait modes by issuing a **stop** or **wait** instruction.
  - — *Clock synthesis module.* Disable the PLL, timer, watchdog, or DDR clocks or disable the CLKO pin.
  - — *AHB subsystem.* Freeze or shut down the AHB subsystem using the GPSCTL[XBR_HRQ] bit.
  - — *Peripheral subsystem.* Halt the individual on-device peripherals such as the DDR memory controller, Ethernet MAC, HDI16, TDM, UART, I^2C, and timer modules.

  For details, see the "Clocks and Power Management" chapter of the *MSC711x Reference Manual*.
- *Power supply design*. One of the most common ways to derive power is to use either a simple fixed or adjustable linear regulator. For the system I/O voltage supply, a simple fixed 3.3 V supply can be used. However, a separate adjustable linear regulator supply for the core voltage VDDC should be implemented. For the memory power supply, regulators are available that take care of all DDR power requirements. **Table 4-2** lists the recommended current rating for each supply per device supported.

Table 4-2. Recommended Power Supply Ratings

Supply	Symbol	Nominal Voltage	Current Rating
Core	V_{DDC}	1.2 V	1.5 A per device
Memory	V_{DDM}	2.5 V	0.5 A per device
Reference	V_{REF}	1.25 V	10 µA per device
I/O	V_{DDIO}	3.3 V	1.0 A per device

4.3 Estimated Power Usage Calculations

The following equations permit estimated power usage to be calculated for individual design conditions. Overall power is derived by totaling the power used by each of the major subsystems:

$$P_{TOTAL} = P_{CORE} + P_{PERIPHERALS} + P_{DDRIO} + P_{IO} + P_{LEAKAGE} \quad \textbf{Equation 3}$$

This equation combines dynamic and static power. Dynamic power is determined using the generic equation:

$$C \times V^2 \times F \times 10^{-3}\ mW \quad \textbf{Equation 4}$$

where,

C = load capacitance in pF
V = peak-to-peak voltage swing in V
F = frequency in MHz

4.3.1 Core Power

Estimation of core power is straightforward. It uses the generic dynamic power equation and assumes that the core load capacitance is 750 pF, core voltage swing is 1.2 V, and the core frequency is 200 MHz or 266 MHz. This yields:

$$P_{CORE} = 750\ pF \times (1.2\ V)^2 \times 200\ MHz \times 10^{-3} = 216\ mW \quad \textbf{Equation 5}$$

$$P_{CORE} = 750\ pF \times (1.2\ V)^2 \times 266\ MHz \times 10^{-3} = 287\ mW \quad \textbf{Equation 6}$$

This equation allows for adjustments to voltage and frequency if necessary.

4.3.2 Peripheral Power

Peripherals include the DDR memory controller, DMA controller, HDI16, TDM, UART, timers, GPIOs, and the I^2C module. Basic power consumption by each module is assumed to be the same and is computed by using the following equation which assumes an effective load of 20 pF, core voltage swing of 1.2 V, and a switching frequency of 100 MH or 133 MHz. This yields:

$$P_{PERIPHERAL} = 20\ pF \times (1.2\ V)^2 \times 100\ MHz \times 10^{-3} = 2.88\ mW\ per\ peripheral \quad \textbf{Equation 7}$$

$$P_{PERIPHERAL} = 20\ pF \times (1.2\ V)^2 \times 133\ MHz \times 10^{-3} = 3.83\ mW\ per\ peripheral \quad \textbf{Equation 8}$$

Multiply this value by the number of peripherals used in the application to compute the total peripheral power consumption.

4.3.3 External Memory Power

Estimation of power consumption by the DDR memory system is complex. It varies based on overall system signal line usage, termination and load levels, and switching rates. Because the DDR memory includes terminations external to the MSC7115 device, the 2.5 V power source provides the power for the termination, which is a static value of 16 mA per signal driven high. The dynamic power is computed, however, using a differential voltage swing of ±0.200 V, yielding a peak-to-peak swing of 0.4 V. The equations for computing the DDR power are:

$$P_{DDRIO} = P_{STATIC} + P_{DYNAMIC} \quad \textbf{Equation 9}$$

$$P_{STATIC} = (\text{unused pins} \times \%\ \text{driven high}) \times 16\ mA \times 2.5\ V \quad \textbf{Equation 10}$$

$$P_{DYNAMIC} = (\text{pin activity value}) \times 20\ pF \times (0.4\ V)^2 \times 200\ MHz \times 10^{-3}\ mW \quad \textbf{Equation 11}$$

$$P_{DYNAMIC} = (\text{pin activity value}) \times 20\ pF \times (0.4\ V)^2 \times 266\ MHz \times 10^{-3}\ mW \quad \textbf{Equation 12}$$

$$\text{pin activity value} = (\text{active data lines} \times \%\ \text{activity} \times \%\ \text{data switching}) + (\text{active address lines} \times \%\ \text{activity}) \quad \textbf{Equation 13}$$

As an example, assume the following:

unused pins = 16 (DDR uses 16-pin mode)
% driven high = 50%
active data lines = 16
% activity = 60%
% data switching = 50%
active address lines = 3

In this example, the DDR memory power consumption is:

$$P_{DDRIO} = ((16 \times 0.5) \times 16 \times 2.5) + (((16 \times 0.6 \times 0.5) + (3 \times 0.6)) \times 20 \times (0.4)^2 \times 200 \times 10^{-3}) = 324.2\ mW \quad \textbf{Equation 14}$$

$$P_{DDRIO} = ((16 \times 0.5) \times 16 \times 2.5) + (((16 \times 0.6 \times 0.5) + (3 \times 0.6)) \times 20 \times (0.4)^2 \times 266 \times 10^{-3}) = 326.3\ mW \quad \textbf{Equation 15}$$

4.3.4 External I/O Power

The estimation of the I/O power is similar to the computation of the peripheral power estimates. The power consumption per signal line is computed assuming a maximum load of 20 pF, a voltage swing of 3.3 V, and a switching frequency of 25 MHz or 33 MHz, which yields:

$$P_{IO} = 20\ pF \times (3.3\ V)^2 \times 25\ MHz \times 10^{-3} = 5.44\ mW\ per\ I/O\ line \quad \textbf{Equation 16}$$

$$P_{IO} = 20\ pF \times (3.3\ V)^2 \times 33\ MHz \times 10^{-3} = 7.19\ mW\ per\ I/O\ line \quad \textbf{Equation 17}$$

Multiply this number by the number of I/O signal lines used in the application design to compute the total I/O power.

Note: The signal loading depends on the board routing. For systems using a single DDR device, the load could be as low as 7 pF.

4.3.5 Leakage Power

The leakage power is for all power supplies combined at a specific temperature. The value is temperature dependent. The observed leakage value at room temperature is 64 mW.

4.3.6 Example Total Power Consumption

Using the examples in this section and assuming four peripherals and 10 I/O lines active, a total power consumption value is estimated as the following:

$$P_{TOTAL}\ (200\ MHz\ core) = 216 + (4 \times 2.88) + 324{,}2 + (10 \times 5.44) + 64 = 670.12\ mW \quad \textbf{Equation 18}$$

$$P_{TOTAL}\ (266\ MHz\ core) = 287 + (4 \times 3.83) + 326.3 + (10 \times 7.19) + 64 = 764.52\ mW \quad \textbf{Equation 19}$$

4.4 Reset and Boot

This section describes the recommendations for configuring the MSC7115 at reset and boot.

4.4.1 Reset Circuit

$\overline{\text{HRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. For an open-drain output such as $\overline{\text{HRESET}}$, take care when driving many buffers that implement input bus-hold circuitry. The bus-hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MSC7115 output current, the pull-up value should not be too small (a 1 KΩ pull-up resistor is used in the MSC711xADS reference design).

4.4.2 Reset Configuration Pins

Table 4-3 shows the MSC7115 reset configuration signals. These signals are sampled at the deassertion (rising edge) of $\overline{\text{PORESET}}$. For details, refer to the Reset chapter of the *MSC711x Reference Manual*.

Table 4-3. Reset Configuration Signals

Signal	Description	Settings	
BM[1–0]	Determines boot mode.	0	Boot from HDI16 port.
		01	Boot from I2C.
		1x	Reserved.

Table 4-3. Reset Configuration Signals (Continued)

Signal	Description	Settings
SWTE	Determines watchdog functionality.	0 Watchdog timer disabled. 1 Watchdog timer enabled.
HDSP	Configures HDI16 strobe polarity.	0 Host Data strobes active low. 1 Host Data strobes active high.
H8BIT	Configures HDI16 operation mode.	0 HDI16 port configured for 16-bit operation. 1 HDI16 port configured for 8-bit operation.

4.4.3 Boot

After a power-on reset, the PLL is bypassed and the device is directly clocked from the CLKIN pin. Using this input clock, the system initializes using the boot loader program that resides in the internal ROM. After initialization, the DSP core can enable the PLL and start the device operating at a higher speed. The MSC7115 can boot from an external host through the HDI16 or download a user program through the I^2C port. The boot operating mode is set by configuring the BM[1–0] signals sampled at the rising edge of $\overline{\text{PORESET}}$, as shown in **Table 4-4**.

Table 4-4. Boot Mode Settings

BM1	BM0	Boot Source
0	0	External host via HDI16 with the PLL disabled.
0	1	I^2C.
1	0	External host via the HDI16 with the PLL enabled.
1	1	Reserved.

4.4.3.1 HDI16 Boot

If the MSC7115 device boots from an external host through the HDI16, the port is configured as follows:

- Operate in Non-DMA mode.
- Operate in polled mode on the device side.
- Operate in polled mode on the external host side.
- External host must write four 16-bit values at a time with the first word as the most significant and the fourth word as the least significant.

When booting from a power-on reset, the HDI16 is additionally configurable as follows:

- 8- or 16-bit mode as specified by the H8BIT pin.
- Data strobe as specified by the HDSP and HDDS pins.

These pins are sampled only on the deassertion of power-on reset. During a boot from a hard reset, the configuration of these pins is unaffected.

Note: When the HDI16 is used for booting or other purposes, bit 0 is the least significant bit and not the most significant bit as for other DSP products.

4.4.3.2 I^2C Boot

When the MSC7115 device is configured to boot from the I^2C port, the boot program configures the GPIO pins shared with the I^2C pins as I^2C pins. The I^2C interface is configured as follows:

- I^2C in master mode.

- EPROM in slave mode.

For details on the boot procedure, see the “Boot Program” chapter of the *MSC711x Reference Manual*.

4.5 DDR Memory System Guidelines

MSC7115 devices contain a memory controller that provides a glueless interface to external double data rate (DDR) SDRAM memory modules with Class 2 Series Stub Termination Logic 2.5 V (SSTL_2). There are two termination techniques, as shown in **Figure 4-3**. Technique B is the most popular termination technique.

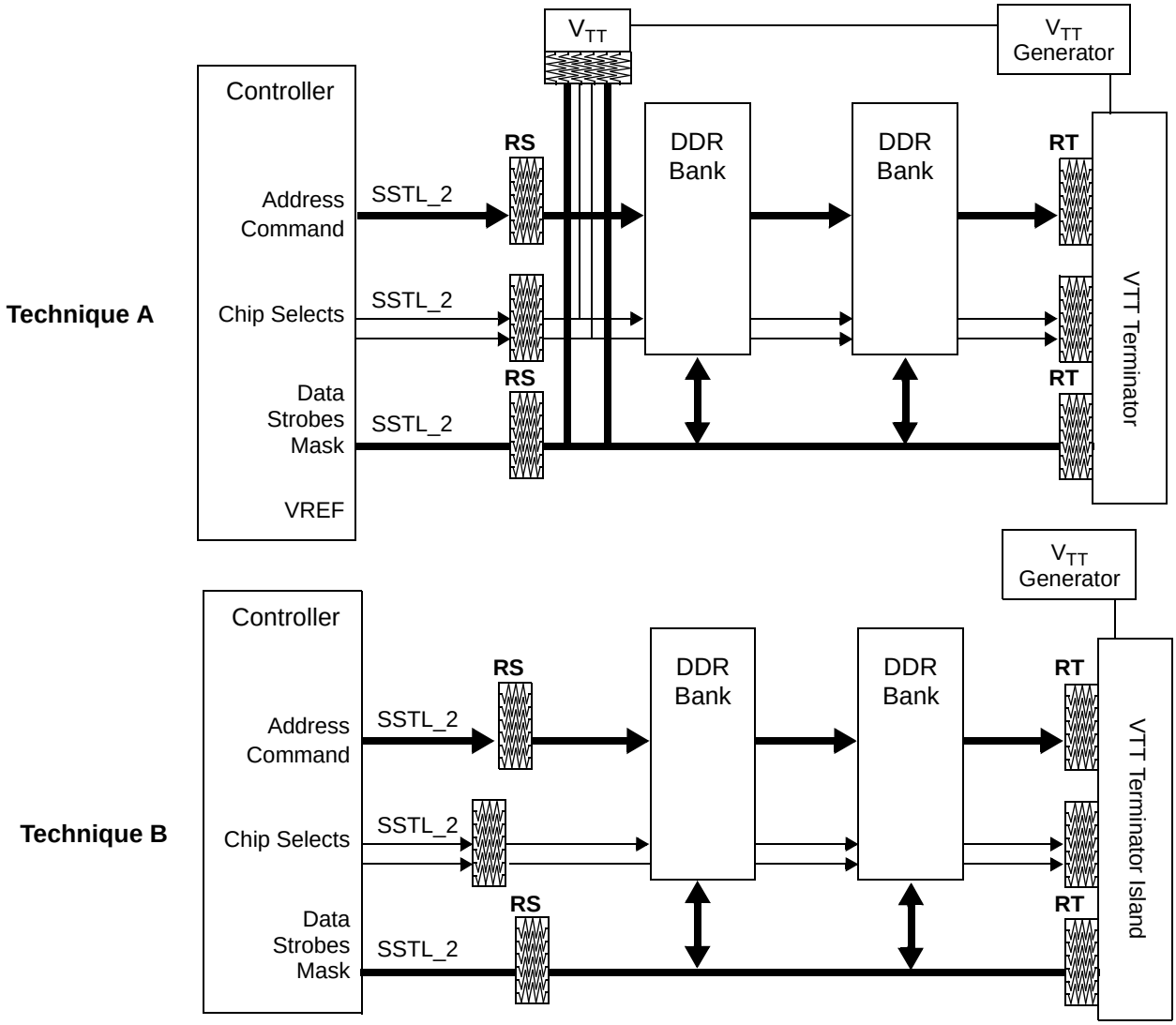


Figure 4-3. SSTL Termination Techniques

Figure 4-4 illustrates the power wattage for the resistors. Typical values for the resistors are as follows:

- RS = 22 Ω
- RT = 24 Ω

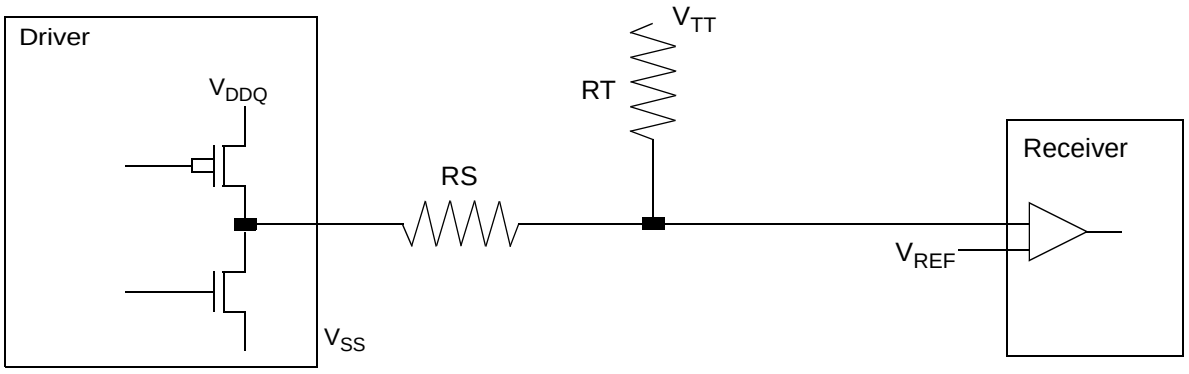


Figure 4-4. SSTL Power Value

4.5.1 V_{REF} and V_{TT} Design Constraints

V_{TT} and V_{REF} are isolated power supplies at the same voltage, with V_{TT} as a high current power source. This section outlines the voltage supply design needs and goals:

- Minimize the noise on both rails.
- V_{TT} must track variation in the V_{REF} DC offsets. Although they are isolated supplies, one possible solution is to use a single IC to generate both signals.
- Both references should have minimal drift over temperature and source supply.
- It is important to minimize the noise from coupling onto V_{REF} as follows:
  - Isolate V_{REF} and shield it with a ground trace.
  - Use 15–20 mm track.
  - Use 20–30 mm clearance between other traces for isolating.
  - Use the outer layer route when possible.
  - Use distributed decoupling to localize transient currents and return path and decouple with an inductance less than 3 nH.
- Max source/sink transient currents of up to 1.8 A for a 32-bit data bus.
- Use a wide island trace on the outer layer:
  - Place the island at the end of the bus.
  - Decouple both ends of the bus.
  - Use distributed decoupling across the island.
  - Place SSTL termination resistors inside the V_{TT} island and ensure a good, solid connection.
- Place the V_{TT} regulator as closely as possible to the termination island.
  - Reduce inductance and return path.
  - Tie current sense pin at the midpoint of the island.

4.5.2 Decoupling

The DDR decoupling considerations are as follows:

- DDR memory requires significantly more burst current than previous SDRAMs.
- In the worst case, up to 64 drivers may be switching states.
- Pay special attention and decouple discrete ICs per manufacturer guidelines.
- Leverage V_{TT} island topology to minimize the number of capacitors required to supply the burst current needs of the termination rail.
- See the Micron DesignLine publication entitled *Decoupling Capacitor Calculation for a DDR Memory Channel* (`http://download.micron.com/pdf/pubs/designline/3Q00dl1-4.pdf`).

4.5.3 General Routing

The general routing considerations for the DDR are as follows:

- All DDR signals must be routed next to a solid reference:
  - For data, next to solid ground planes.
  - For address/command, power planes if necessary.
- All DDR signals must be impedance controlled. This is system dependent, but typical values are 50–60 ohm.
- Minimize other cross-talk opportunities. As possible, maintain at least a four times the trace width spacing between all DDR signals to non-DDR signals.
- Keep the number of vias to a minimum to eliminate additional stubs and capacitance.
- Signal group routing priorities are as follows:
  - DDR clocks.
  - Route MVTT/MVREF.
  - Data group.
  - Command/address.
- Minimize data bit jitter by trace matching.

4.5.4 Routing Clock Distribution

The DDR clock distribution considerations are as follows:

- DDR controller supports six clock pairs:
  - 2 DIMM modules.
  - Up to 36 discrete chips.
- For route traces as for any other differential signals:
  - Maintain proper difference pair spacing.
  - Match pair traces within 25 mm.
- Match all clock traces to within 100 mm.
- Keep all clocks equally loaded in the system.
- Route clocks on inner critical layers.

4.5.5 Data Routing

The DDR data routing considerations are as follows:

- Route each data group (8-bits data + DQS + DM) on the same layer. Avoid switching layers within a byte group.
- Take care to match trace lengths, which is extremely important.
- To make trace matching easier, let adjacent groups be routed on alternate critical layers.
- Pin swap bits within a byte group to facilitate routing (discrete case).
- Tight trace matching is recommended within the DDR data group. Keep each 8-bit datum and its DM signal within ± 25 mm of its respective strobe.
- Minimize lengths across the entire DDR channel:
  - Between all groups maintain a delta of no more than 500 mm.
  - Allows greater flexibility in the design for readjustments as needed.
- DDR data group separation:
  - If stack-up allows, keep DDR data groups away from the address and control nets.
  - Route address and control on separate critical layers.
  - If resistor networks (RNs) are used, attempt to keep data and command lines in separate packages.

4.6 Connectivity Guidelines

This section summarizes the connections and special conditions, such as pull-up or pull-down resistors, for the MSC7115 device. Following are guidelines for signal groups and configuration settings:

- *Clock and reset signals*.
  - SWTE is used to configure the MSC7115 device and is sampled on the deassertion of $\overline{\text{PORESET}}$, so it should be tied to V_{DDC} or GND either directly or through pull-up or pull-down resistors until $\overline{\text{PORESET}}$ is deasserted. After $\overline{\text{PORESET}}$, this signal can be left floating.
  - BM[0–1] configure the MSC7115 device and are sampled until $\overline{\text{PORESET}}$ is deasserted, so they should be tied to V_{DDIO} or GND either directly or through pull-up or pull-down resistors.
  - $\overline{\text{HRESET}}$ should be pulled up.
- *Interrupt signals*. When used, $\overline{\text{IRQ}}$ pins must be pulled up.
- *HDI16 signals*.
  - When they are configured for open-drain, the $\overline{\text{HREQ}}$/HREQ or $\overline{\text{HTRQ}}$/HTRQ signals require a pull-up resistor. However, these pins are also sampled at power-on reset to determine the HDI16 boot mode and may need to be pulled down. When these pins must be pulled down on reset and pulled up otherwise, a buffer can be used with the $\overline{\text{HRESET}}$ signal as the enable.
  - When the device boots through the HDI16, the HDDS, HDSP and H8BIT pins should be pulled up or down, depending on the required boot mode settings.
- *Ethernet MAC/TDM2 signals*. The MDIO signal requires an external pull-up resistor.
- *I^2C signals*. The SCL and SDA signals, when programmed for I^2C, requires an external pull-up resistor.
- *General-purpose I/O (GPIO) signals*. An unused GPIO pin can be disconnected. After boot, program it as an output pin.

- *Other signals.*
  - The $\overline{\text{TEST0}}$ pin must be connected to ground.
  - The $\overline{\text{TPSEL}}$ pin should be pulled up to enable debug access via the EOnCE port and pulled down for boundary scan.
  - Pins labelled NO CONNECT (NC) must not be connected.
  - When a 16-pin double data rate (DDR) interface is used, the 16 unused data pins should be no connects (floating) if the used lines are terminated.
  - Do not connect DBREQ to DONE (as you would for the MSC8101 device). Connect DONE to one of the EVNT pins, and DBREQ to HRRQ.

Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
MSC7115 (mask 1L44X	1.2 V core 2.5 V mem. 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	400	200	Lead-free	MSC7115VM800
					Lead-bearing	MSC7115VF800
MSC7115 (mask 1M88B)	1.2 V core 2.5 V mem 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	400	266	Lead-free	MSC7115VM1000
					Lead-bearing	MSC7115VF1000

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