DSP56F807

Preliminary Technical Data

DSP56F807 16-bit Digital Signal Processor

- Up to 40 MIPS at 80 MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 60K × 16-bit words Program Flash
- 2K × 16-bit words Program RAM
- 8K × 16-bit words Data Flash
- 4K × 16-bit words Data RAM
- 2K × 16-bit words Boot Flash
- Up to 64K × 16- bit words each of external program and data memory
- Two 6 channel PWM Modules
- Four 4 channel, 12-bit ADCs
- Two Quadrature Decoders
- CAN 2.0 B Module
- Two Serial Communication Interfaces (SCIs)
- Serial Peripheral Interface (SPI)
- Up to four General Purpose Quad Timers
- JTAG/OnCE™ port for debugging
- 14 Dedicated and 18 Shared GPIO lines
- 160-pin LQFP or 160 MAPBGA Packages

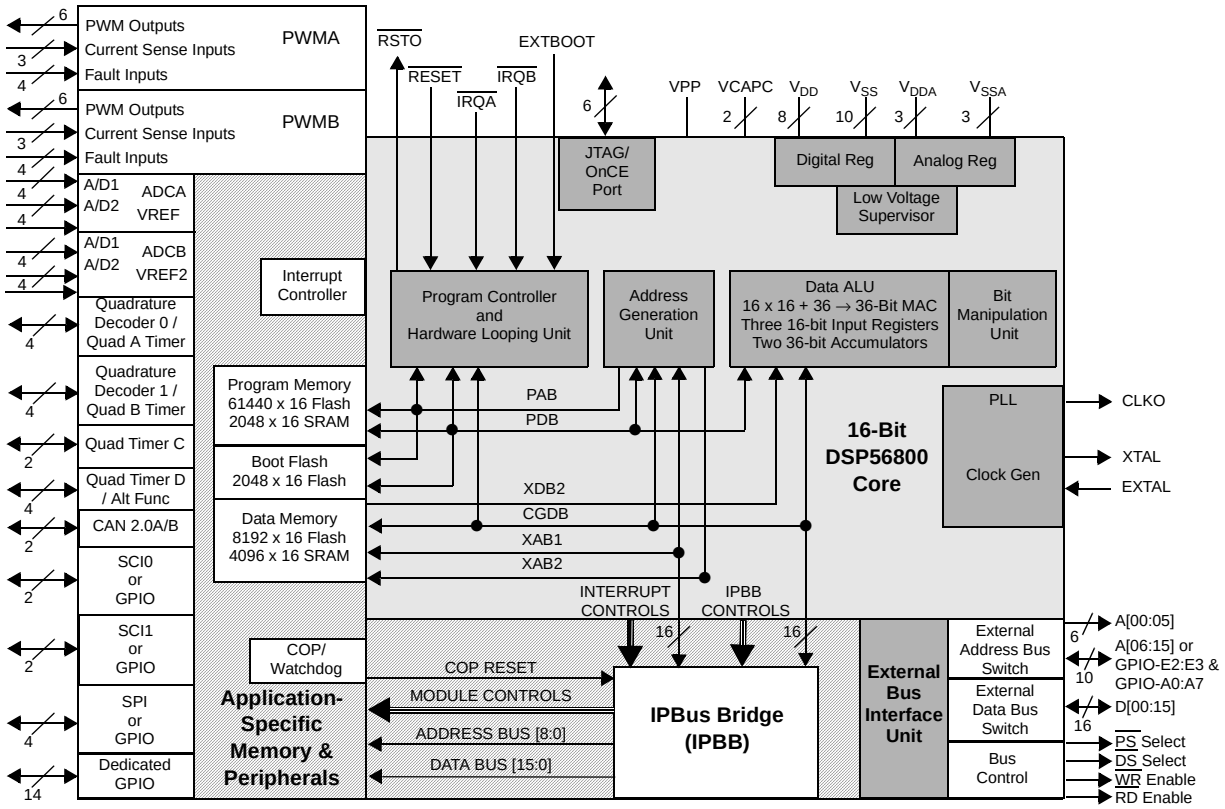


Figure 1. DSP56F807 Block Diagram

Digital DNA™ From Motorola

Part 1 Overview

1.1 DSP56F807 Features

1.1.1 Digital Signal Processing Core

- Efficient 16-bit DSP56800 family DSP engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80 MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory including a low-cost, high-volume flash solution
  - 60K × 16-bit words of Program Flash
  - 2K × 16-bit words of Program RAM
  - 8K × 16-bit words of Data Flash
  - 4K × 16-bit words of Data RAM
  - 2K × 16-bit words of Boot Flash
- Off-chip memory expansion capabilities programmable for 0, 4, 8, or 12 wait states
  - As much as 64K × 16 bits of data memory
  - As much as 64K × 16 bits of program memory

1.1.3 Peripheral Circuits for DSP56F807

- Two Pulse Width Modulator modules each with six PWM outputs, three Current Sense inputs, and four Fault inputs, fault tolerant design with deadtime insertion, supports both center and edge aligned modes
- Four 12-bit, Analog-to-Digital Converters (ADCs), which support four simultaneous conversions with quad, 4-pin multiplexed inputs; ADC and PWM modules can be synchronized
- Two Quadrature Decoders each with four inputs or two additional Quad Timers

- Two dedicated General Purpose Quad Timers totaling six pins: Timer C with two pins and Timer D with four pins
- CAN 2.0 B Module with 2-pin port for transmit and receive
- Two Serial Communication Interfaces each with two pins (or four additional GPIO lines)
- Serial Peripheral Interface (SPI) with configurable 4-pin port (or four additional GPIO lines)
- Computer-Operating Properly (COP) Watchdog timer
- Two dedicated external interrupt pins
- 14 dedicated General Purpose I/O (GPIO) pins, 18 multiplexed GPIO pins
- External reset input pin for hardware reset
- External reset output pin for system reset
- JTAG/On-Chip Emulation (OnCE™) for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase Lock Loop-based frequency synthesizer for the DSP core clock

1.1.4 Energy Information

- Fabricated in high-density CMOS with 5V tolerant, TTL-compatible digital inputs
- Uses a single 3.3V power supply
- On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- Wait and Stop modes available

1.2 DSP56F807 Description

The DSP56F807 is a member of the DSP56800 core-based family of Digital Signal Processors (DSPs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the DSP56F807 is well-suited for many applications. The DSP56F807 includes many peripherals that are especially useful for applications such as motion control, smart appliances, steppers, encoders, tachometers, limit switches, power supply and control, automotive control, engine management, noise suppression, remote utility metering, industrial control for power, lighting, and automation.

The DSP56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C/C++ Compilers to enable rapid development of optimized control applications.

The DSP56F807 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip data RAM per instruction cycle. The DSP56F807 also provides two external dedicated interrupt lines and up to 32 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The DSP56F807 DSP controller includes 60K, 16-bit words of program flash and 8K words of data flash (each programmable through the JTAG port) with 2K words of program RAM and 4K words of data RAM. It also supports program execution from external memory.

A total of 2K words of Boot Flash is incorporated for easy customer-inclusion of field-programmable

software routines that can be used to program the main program and data flash memory areas. Both program and data flash memories can be independently bulk erased or erased in page sizes of 256 words. The Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the DSP56F807 is the inclusion of two Pulse Width Modulator (PWM) modules. These modules each incorporate three complementary, individually programmable PWM signal outputs (each module is also capable of supporting six independent PWM functions for a total of 12 PWM outputs) to enhance motor control functionality. Complementary operation permits programmable dead-time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge and center aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors), both BDC and BLDC (Brush and Brushless DC motors), SRM and VRM (Switched and Variable Reluctance Motors), and stepper motors. The PWMs incorporate fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM modules provide a reference output to synchronize the analog-to-digital converters.

The DSP56F807 incorporates two separate Quadrature Decoders capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast and slow moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a timeout value to alarm when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This DSP controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCI), one Serial Peripheral Interface (SPI), and four Quad Timers. Any of these interfaces can be used as General-Purpose Input/Outputs (GPIO) if that function is not required. A Controller Area Network interface (CAN Version 2.0 A/B compliant), an internal interrupt controller, and 14 dedicated GPIO lines are also included on the DSP56F807.

1.3 “Best in Class” Development Environment

The SDK (Software Development Kit) provides fully debugged peripheral drivers, libraries and interfaces that allow programmers to create their unique C application code independent of component architecture. The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards support concurrent engineering. Together, the SDK, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1** are required for a complete description and proper design with the DSP56F807. Documentation is available from local Motorola distributors, Motorola semiconductor sales offices, Motorola Literature Distribution Centers, or online at http://www.motorola.com/semiconductors/dsp.

Table 1. DSP56F807 Chip Documentation

Topic	Description	Order Number
DSP56800 Family Manual	Detailed description of the DSP56800 family architecture, and 16-bit DSP core processor and the instruction set	DSP56800FM/D
DSP56F801/803/805/807 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56F801, DSP56F803, DSP56F805, and DSP56F807	DSP56F801-7UM/D
DSP56F807 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F807/D
DSP56F807 Product Brief	Summary description and block diagram of the DSP56F807 core, memory, peripherals and interfaces	DSP56F807PB/D

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the DSP56F807 are organized into functional groups, as shown in **Table 2** and as illustrated in **Figure 2**. In **Table 3** through **Table 19**, each table row describes the signal or signals present on a pin.

Table 2. Functional Group Pin Allocations

Functional Group	Number of Pins	Detailed Description
Power (V_{DD} or V_{DDA})	11	Table 3
Ground (V_{SS} or V_{SSA})	13	Table 4
Supply Capacitors & V_{PP}	4	Table 5
PLL and Clock	3	Table 6
Address Bus[1]	16	Table 7
Data Bus	16	Table 8
Bus Control	4	Table 9
Interrupt and Program Control	5	Table 10
Dedicated General Purpose Input/Output	14	Table 11
Pulse Width Modulator (PWM) Ports	26	Table 12
Serial Peripheral Interface (SPI) Port[1]	4	Table 13
Quadrature Decoder Ports[2]	8	Table 14
Serial Communications Interface (SCI) Ports[1]	4	Table 15
CAN Port	2	Table 16
Analog to Digital Converter (ADC) Ports	20	Table 17
Quad Timer Module Ports	6	Table 18
JTAG/On-Chip Emulation (OnCE)	6	Table 19

1. Alternately, GPIO pins
2. Alternately, Quad Timer pins

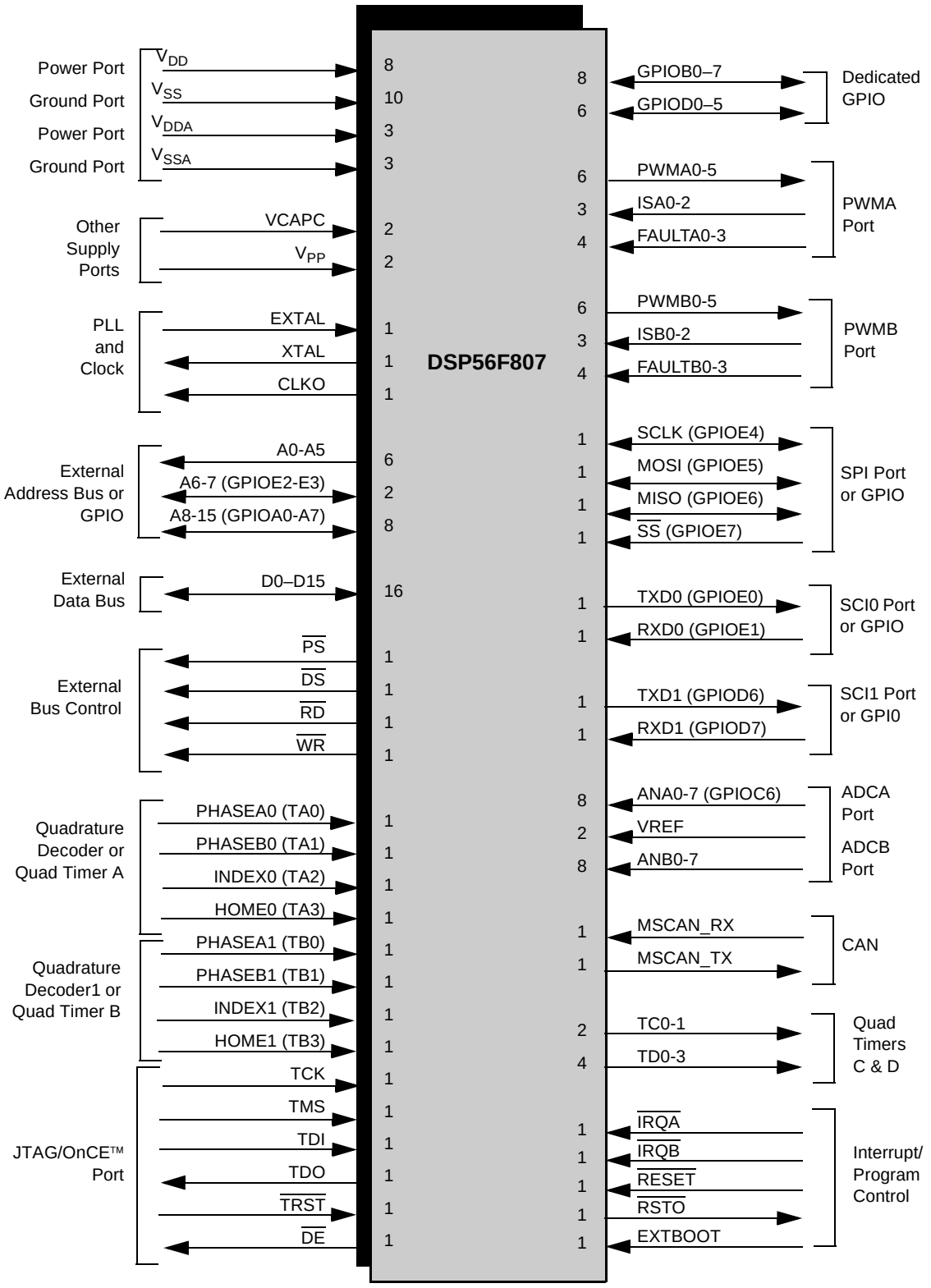


Figure 2. DSP56F807 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

2.2 Power and Ground Signals

Table 3. Power Inputs

No. of Pins	Signal Name	Signal Description
8	V_{DD}	**Power**—These pins provide power to the internal structures of the chip, and should all be attached to V_{DD}.
3	V_{DDA}	**Analog Power**—These pins supply an analog power source.

Table 4. Grounds

No. of Pins	Signal Name	Signal Description
9	V_{SS}	**GND**—These pins provide grounding for the internal structures of the chip and should all be attached to V_{SS}.
3	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.
1	**TCS**	**TCS**—This pin is reserved for factory use and must be tied to V_{SS} for normal use. In block diagrams, this pin is considered an additional V_{SS}.

Table 5. Supply Capacitors and VPP

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**VCAPC**	Supply	Supply	**VCAPC** - Connect each pin to a 2.2uF bypass capacitor in order to bypass the core logic voltage regulator (required for proper chip operation). For more information, please refer to **Section 5.2, Electrical Design Considerations.**
1	**VPP**	Input	Input	**VPP** - This pin should be left unconnected as an open circuit for normal functionality.
1	**VPP_2**	Input	Input	**VPP_2** - This pin should be left unconnected as an open circuit for normal functionality.

2.3 Clock and Phase Lock Loop Signals

Table 6. PLL and Clock

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**EXTAL**	Input	Input	**External Crystal Oscillator Input**—This input can be connected to an 8MHz external crystal. If an 8MHz or less external clock source is used, EXTAL can be used as the input and XTAL must not be connected. For more information, please refer to **Section 3.5.2**. This input can also be connected to an external 8MHz clock. For more information, please refer to **Section 3.5** The input clock can be selected to provide the clock directly to the DSP core. This input clock can also be selected as input clock for the on-chip PLL.
1	**XTAL**	Output	Chip-driven	**Crystal Oscillator Output**—This output connects the internal crystal oscillator output to an external crystal. If an external clock source over 8MHz is used, XTAL must be used as the input and EXTAL connected to GND. For more information, please refer to **Section 3.5.2**.
1	**CLKO**	Output	Chip-driven	**Clock Output**—This pin outputs a buffered clock signal. By programming the CS[1:0] bits in the PLL Control Register (PCR1), the user can select between outputting a version of the signal applied to XTAL and a version of the DSP master clock at the output of the PLL. The clock frequency on this pin can also be disabled by programming the CS[1:0] bits in PCR1.

2.4 Address, Data, and Bus Control Signals

Table 7. Address Bus Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**A0–A5**	Output	Tri-stated	**Address Bus**—A0–A5 specify the address for external program or data memory accesses.
2	**A6–A7** **GPIOE2-GPIOE3**	Output Input/ Output	Tri-stated Input	**Address Bus**—A6–A7 specify the address for external program or data memory accesses. **Port E GPIO**—These two General Purpose I/O (GPIO) pins can individually be programmed as input or output pins. After reset, the default state is Address Bus.
8	**A8–A15** **GPIOA0-GPIOA7**	Output Input/ Output	Tri-stated Input	**Address Bus**—A8–A15 specify the address for external program or data memory accesses. **Port A GPIO**—These eight General Purpose I/O (GPIO) pins can be individually programmed as input or output pins. After reset, the default state is Address Bus.

Table 8. Data Bus Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
16	**D0–D15**	Input/ Output	Tri-stated	**Data Bus**— D0–D15 specify the data for external program or data memory accesses. D0–D15 are tri-stated when the external bus is inactive. Internal pullups may be active.

Table 9. Bus Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**$\overline{\text{PS}}$**	Output	Tri-stated	**Program Memory Select**—$\overline{\text{PS}}$ is asserted low for external program memory access.
1	**$\overline{\text{DS}}$**	Output	Tri-stated	**Data Memory Select**—$\overline{\text{DS}}$ is asserted low for external data memory access.
1	**$\overline{\text{WR}}$**	Output	Tri-stated	**Write Enable**—$\overline{\text{WR}}$ is asserted during external memory write cycles. When $\overline{\text{WR}}$ is asserted low, pins D0–D15 become outputs and the DSP puts data on the bus. When $\overline{\text{WR}}$ is deasserted high, the external data is latched inside the external device. When $\overline{\text{WR}}$ is asserted, it qualifies the A0–A15, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ pins. $\overline{\text{WR}}$ can be connected directly to the $\overline{\text{WE}}$ pin of a Static RAM.
1	**$\overline{\text{RD}}$**	Output	Tri-stated	**Read Enable**—$\overline{\text{RD}}$ is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted low, pins D0–D15 become inputs and an external device is enabled onto the DSP data bus. When $\overline{\text{RD}}$ is deasserted high, the external data is latched inside the DSP. When $\overline{\text{RD}}$ is asserted, it qualifies the A0–A15, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ pins. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a Static RAM or ROM.

2.5 Interrupt and Program Control Signals

Table 10. Interrupt and Program Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**$\overline{\text{IRQA}}$**	Input	Input	**External Interrupt Request A**—The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered.
1	**$\overline{\text{IRQB}}$**	Input	Input	**External Interrupt Request B**—The $\overline{\text{IRQB}}$ input is an external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered.
1	**$\overline{\text{RSTO}}$**	Output	Output	**Reset Output**—This output reflects the internal reset state of the chip.

Table 10. Interrupt and Program Control Signals (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**$\overline{\text{RESET}}$**	Input	Input	**Reset**—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the DSP is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the OnCE/ JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
1	**EXTBOOT**	Input	Input	**External Boot**—This input is tied to VDD to force device to boot from off-chip memory. Otherwise, it is tied to VSS.

2.6 GPIO Signals

Table 11. Dedicated General Purpose Input/Output (GPIO) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
8	**GPIOB0-GPIOB7**	Input or Output	Input	**Port B GPIO**—These eight pins are dedicated General Purpose I/O (GPIO) pins that can individually be programmed as input or output pins. After reset, the default state is GPIO input.
6	**GPIOD0-GPIOD5**	Input or Output	Input	**Port D GPIO**—These six pins are dedicated GPIO pins that can individually be programmed as an input or output pins. After reset, the default state is GPIO input.

2.7 Pulse Width Modulator (PWM) Signals

Table 12. Pulse Width Modulator (PWMA and PWMB) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
6	**PWMA0-5**	Output	Tri-stated	**PWMA0-5**— Six PWMA output pins.
3	**ISA0-2**	Input	Input	**ISA0-2**— These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMA.
4	**FAULTA0-3**	Input	Input	**FAULTA0-3**— These Fault input pins are used for disabling selected PWMA outputs in cases where fault conditions originate off-chip.
6	**PWMB0-5**	Output	Output	**PWMB0-5**— Six PWMB output pins.

Table 12. Pulse Width Modulator (PWMA and PWMB) Signals (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
3	**ISB0-2**	Input	Input	**ISB0-2**— These three input current status pins are used for top/bottom pulse width correction in complementary channel operation for PWMB.
4	**FAULTB0-3**	Input	Input	**FAULTB0-3**— These four Fault input pins are used for disabling selected PWMB outputs in cases where fault conditions originate off-chip.

2.8 Serial Peripheral Interface (SPI) Signals

Table 13. Serial Peripheral Interface (SPI) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MISO**	Input/ Output	Input	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
	GPIOE6	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MISO.
1	**MOSI**	Input/ Output	Input	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
	GPIOE5	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MOSI.
1	**SCLK**	Input/ Output	Input	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
	GPIOE4	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCLK.
1	**$\overline{SS}$**	Input	Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave.
	GPIOE7	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is $\overline{SS}$.

2.9 Quadrature Decoder Signals

Table 14. Quadrature Decoder (Quad Dec0 and Quad Dec1) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**PHASEA0**	Input	Input	**Phase A**—Quadrature Decoder #0 PHASEA input
	TA0	Input/Output	Input	**TA0**—Timer A Channel 0
1	**PHASEB0**	Input	Input	**Phase B**—Quadrature Decoder #0 PHASEB input
	TA1	Input/Output	Input	**TA1**—Timer A Channel 1
1	**INDEX0**	Input	Input	**Index**—Quadrature Decoder #0 INDEX input
	TA2	Input/Output	Input	**TA2**—Timer A Channel 2
1	**HOME0**	Input	Input	**Home**—Quadrature Decoder #0 HOME input
	TA3	Input/Output	Input	**TA3**—Timer A Channel 3
1	**PHASEA1**	Input	Input	**Phase A**—Quadrature Decoder #1 PHASEA input
	TB0	Input/Output	Input	**TB0**—Timer B Channel 0
1	**PHASEB1**	Input	Input	**Phase B**—Quadrature Decoder #1 PHASEB input
	TB1	Input/Output	Input	**TB1**—Timer B Channel 1
1	**INDEX1**	Input	Input	**Index**—Quadrature Decoder #1 INDEX input
	TB2	Input/Output	Input	**TB2**—Timer B Channel 2
1	**HOME1**	Input	Input	**Home**—Quadrature Decoder #1 HOME input
	TB3	Input/Output	Input	**TB3**—Timer B Channel 3

2.10 Serial Communications Interface (SCI) Signals

Table 15. Serial Communications Interface (SCI0 and SCI1) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TXD0**	Output	Input	**Transmit Data (TXD0)**—transmit data output
	GPIOE0	Input/ Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI output.

Table 15. Serial Communications Interface (SCI0 and SCI1) Signals (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**RXD0** **GPIOE1**	Input Input/ Output	Input Input	**Receive Data (RXD0)**— receive data input **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI input.
1	**TXD1** **GPIOD6**	Output Input/ Output	Input Input	**Transmit Data (TXD1)**—transmit data output **Port D GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI output.
1	**RXD1** **GPIOD7**	Input Input/ Output	Input Input	**Receive Data (RXD1)**— receive data input **Port D GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI input.

2.11 CAN Signals

Table 16. CAN Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MSCAN_ RX**	Input	Input	**MSCAN Receive Data**—MSCAN input. This pin has an internal pull-up resistor.
1	**MSCAN_ TX**	Output	Output	**MSCAN Transmit Data**—MSCAN output. CAN output is open-drain output and pull-up resistor is needed.

2.12 Analog-to-Digital Converter (ADC) Signals

Table 17. Analog to Digital Converter Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
4	**ANA0-3**	Input	Input	**ANA0-3**—Analog inputs to ADCA channel 1
4	**ANA4-7**	Input	Input	**ANA4-7**—Analog inputs to ADCA channel 2
1	**VREF**	Input	Input	**VREF**—Analog reference voltage
4	**ANB0-3**	Input	Input	**ANB0-3**—Analog inputs to ADCB, channel 1

Table 17. Analog to Digital Converter Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
4	**ANB4-7**	Input	Input	**ANB4-7**—Analog inputs to ADCB, channel 2
1	**$VREF_2$**	Input	Input	**$VREF_2$**—Analog reference voltage

2.13 Quad Timer Module Signals

Table 18. Quad Timer Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**TC0-1**	Input/Output	Input	**TC0-1**—Timer C Channels 0 and 1
4	**TD0-3**	Input/Output	Input	**TD0-3**—Timer D Channels 0, 1, 2, and 3

2.14 JTAG/OnCE

Table 19. JTAG/On-Chip Emulation (OnCE) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TCK**	Input	Input, pulled low internally	**Test Clock Input**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
1	**TMS**	Input	Input, pulled high internally	**Test Mode Select Input**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
1	**TDI**	Input	Input, pulled high internally	**Test Data Input**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
1	**TDO**	Output	Tri-stated	**Test Data Output**—This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
1	**$\overline{\text{TRST}}$**	Input	Input, pulled high internally	**Test Reset**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
1	**$\overline{\text{DE}}$**	Output	Output	**Debug Event**—$\overline{\text{DE}}$ provides a low pulse on recognized debug events.

Part 3 Specifications

3.1 General Characteristics

The DSP56F807 is fabricated in high-density CMOS with 5-volt tolerant TTL-compatible digital inputs. The term “5-volt tolerant” refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such sytems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 20** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The DSP56F807 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either or V_{DD} or V_{SS}).

Table 20. Absolute Maximum Ratings (V_{SS}, V_{SSA}= 0 V)

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3	4.0	V
All other input voltages, excluding Analog inputs	V_{IN}	V_{SS} – 0.3	5.5V	V
Analog inputs, ANA0-7 and VREF	V_{IN}	V_{SSA}	V_{DDA}	V
Current drain per pin excluding V_{DD}, V_{SS}, PWM outputs, TCS, VPP, VDDA, VSSA	I	—	10	mA
Current drain per pin for PWM outputs	I	—	20	mA

Table 20. Absolute Maximum Ratings (V_{SS}, V_{SSA}= 0 V) (Continued)

Characteristic	Symbol	Min	Max	Unit
Junction temperature	T_J	—	150	°C
Storage temperature range	T_{STG}	-55	150	°C

Table 21. Recommended Operating Conditions (V_{SS}, V_{SSA} = 0 V)

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD},V_{DDA}	3.0	3.6	V
Ambient operating temperature	T_A	-40	85	°C
Flash program/erase temperature	T_F	0	85	°C

Table 22. Thermal Characteristics[1]

Characteristic	160-pin LQFP		
	Symbol	Value	Unit
Thermal resistance junction-to-ambient (estimated)	θ_{JA}	40	°C/W
I/O pin power dissipation	$P_{I/O}$	User Determined	W
Power dissipation	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O}$	W
Maximum allowed P_D	P_{DMAX}	$(T_J - T_A) / \theta_{JA}$	°C

1. See **Section 5.1** for more detail.

3.2 DC Electrical Characteristics

Table 23. DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{op} = 80$ MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	2.5	2.75	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	-0.3	—	0.5	V
Input high voltage (all other inputs, EXTAL when using external clock)	V_{IH}	2.0	—	5.5	V
Input low voltage (all other inputs, EXTAL when using external clock)	V_{IL}	-0.3	—	0.8	V
Input current low (pullups disabled)	I_{IL}	-1	—	1	µA
Input current high (pullups disabled)	I_{IH}	-1	—	1	µA
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA
Output Voltage High (at IOH)	V_{OH}	$V_{DD} – 0.7$	—	—	V
Output Voltage Low (at IOL)	V_{OL}	—	—	0.4	V
Output High Current	I_{OH}	-300	—	—	µA
Output Low Current	I_{OL}	—		2	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
PWM pin output source current[1]	I_{OHP}	—	—	-10	mA
PWM pin output sink current[2]	I_{OLP}	—	—	16	mA
V_{DD} supply current Run [3] Wait[4] Stop	I_{DD}	 — — —	 180 170 120	 200 180 130	 mA mA mA
Low Voltage Interrupt[5]	V_{EI}	—	2.7	TBD	V
Low Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	5.0	—	mV
Power on Reset[6]	POR	—	1.5	2.0	V

1. PWM pin output source current measured with 50% duty cycle.
2. PWM pin output sink current measured with 50% duty cycle.

3. Run (operating) I_{DD} measured using external square wave clock source (f_{osc} = 8 MHz) into XTAL. All inputs 0.2 V from rail; no dc loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 80MHz out.

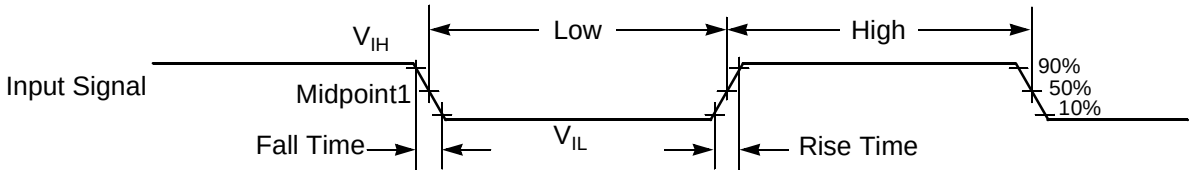
4. Wait I_{DD} measured using external square wave clock source (f_{osc} = 8 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs. C_L = 20 pF on OSC2; all ports configured as inputs; OSC2 capacitance linearly affects wait I_{DD}; measured with PLL and LVI enabled.

5. When V_{DD} drops below V_{EI} max value, an interrupt is generated.

6. Power on reset occurs whenever the internally regulated 2.5 volts digital supply drops below 1.8 volts. While power is ramping up, this signal remains active for as long as the internal 2.5 volts is below 1.8 volts no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5 volts is reached, at which time it self regulates.

3.3 AC Electrical Characteristics

Timing waveforms in **Section 3.3, AC Electrical Characteristics,** are tested with a V_{IL} maximum of 0.8 V and a V_{IH} minimum of 2.0 V for all pins except XTAL, which is tested using the input levels in **Section 3.2, DC Electrical Characteristics.** . In **Figure 3** the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 3. Input Signal Measurement References

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state.
- Tri-stated, when a bus or signal is placed in a high impedance state.
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}.
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}.

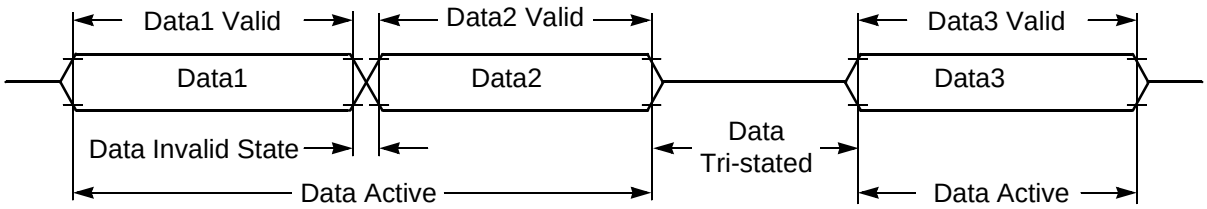


Figure 4. Signal States

3.4 Flash Memory Characteristics

Table 24. Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE=0
2. Y address enable, YMUX is disabled when YE=0
3. Sense amplifier enable
4. Output enable, tri-state flash data out bus when OE=0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 25. IFREN Truth Table

Mode	IFREN=1	IFREN=0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both block	Erase main memory block

Table 26. Timing Symbols

Characteristic	Symbol	See Figure(s)
X address access time	T_{xa}	-
Y address access time	T_{ya}	-
OE access time	T_{oa}	-
PROG/ERASE to NVSTR set up time	T_{nvs*}	Figure 5, Figure 6, Figure 7
NVSTR hold time	T_{nvh*}	Figure 5, Figure 6
NVSTR hold time(mass erase)	T_{nvh1*}	Figure 7
NVSTR to program set up time	T_{pgs*}	Figure 5

Table 26. Timing Symbols (Continued)

Program hold time	T_{pgh}	Figure 5
Address/data set up time	T_{ads}	Figure 5
Address/data hold time	T_{adh}	Figure 5
Recovery time	T_{rcv}*	Figure 5, Figure 6, Figure 7
Cumulative program HV period	T_{hv}	Figure 5
Program time	T_{prog}*	Figure 5
Erase time	T_{erase}*	Figure 6
Mass erase time	T_{me}*	Figure 7

*The flash interface unit provides registers for the control of these parameters.

Table 27. Flash Timing Parameters

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to +85°C, $C_L \leq 50$ pF

Characteristic	Symbol	Min	Typ	Max	Unit
Program time[1]	T_{prog}	20	-	-	us
Erase time[2]	T_{erase}	20	-	-	ms
Mass erase time[3]	T_{me}	100	-	-	ms
Endurance[4]	E_{CYC}	10,000	-	-	cycles
Data Retention	D_{RET}	10	-	-	years
PROG/ERASE to NVSTR set up time	T_{nvs}	-	5	-	us
NVSTR hold time	T_{nvh}	-	5	-	us
NVSTR hold time(mass erase)	T_{nvh1}	-	100	-	us
NVSTR to program set up time	T_{pgs}	-	10	-	us
Recovery time	T_{rcv}	-	1	-	us
Cumulative program HV period[5]	T_{hv}	-	3	-	ms

1. Program specification guaranteed from TA = 0° C to 85° C.
2. Erase specification guaranteed from TA = 0° C to 85° C.
3. Mass erase specification guaranteed from TA = 0° C to 85° C.
4. One cycle is equal to an erase, program, and read.
5. Thv is the cumulative high voltage programming time to the same row before next erase. The same address can not be programmed twice before next erase.

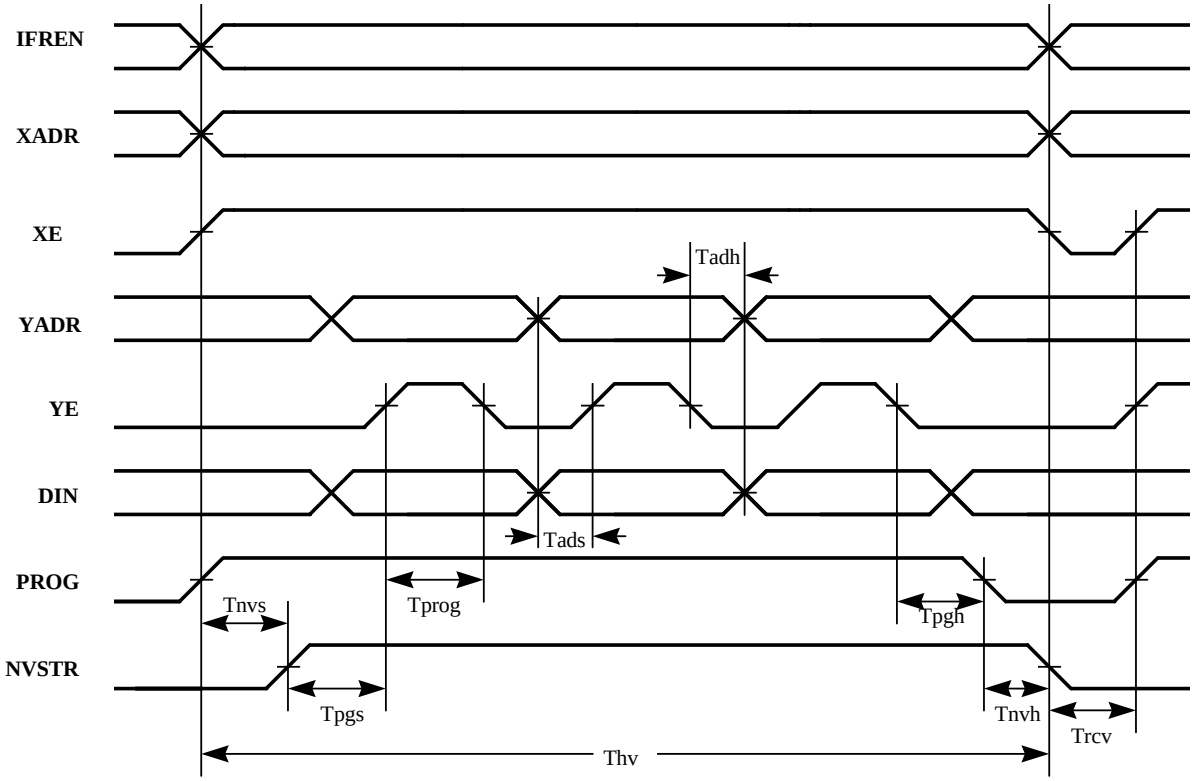


Figure 5. Flash Program Cycle

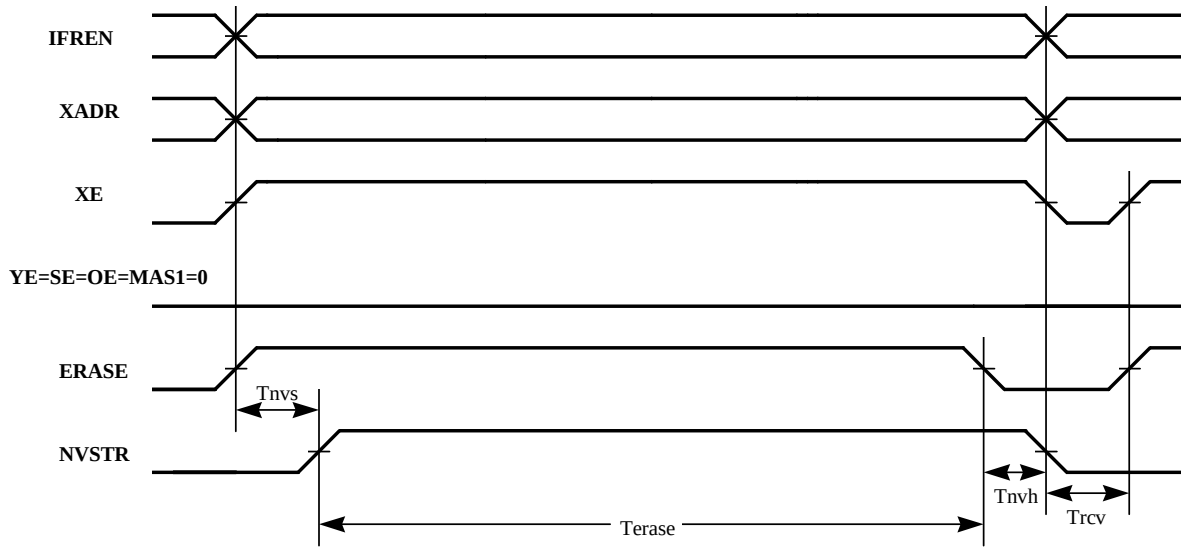


Figure 6. Flash Erase Cycle

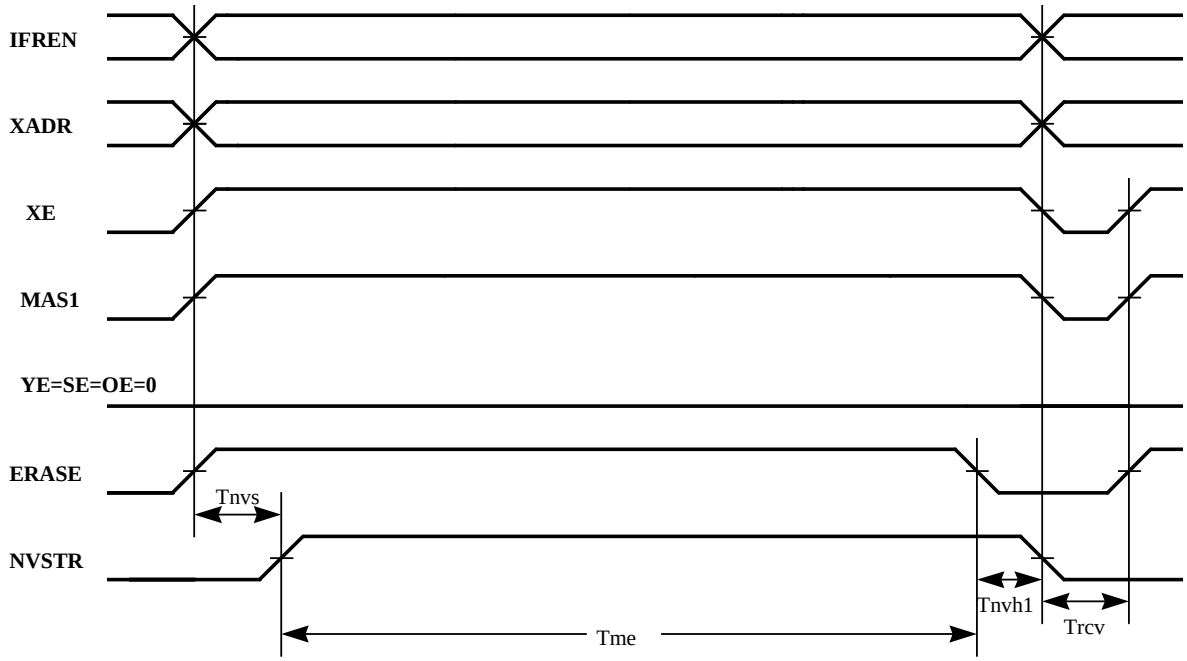


Figure 7. Flash Mass Erase Cycle

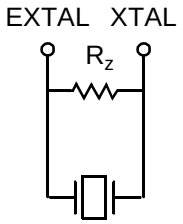
3.5 External Clock Operation

The DSP56F807 system clock can be derived from an external crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

3.5.1 Crystal Oscillator

The internal oscillator is also designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 29**. In **Figure 8** a typical crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, since crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

Crystal Frequency = 4–8 MHz (optimized for 8 MHz)



Sample External Crystal Parameters:
R_Z = 10 MΩ

Figure 8. Crystal Oscillator

3.5.2 External Clock Source

The recommended method of connecting an external clock is given in **Figure 9**. The external clock source is connected to XTAL and the EXTAL pin is grounded.

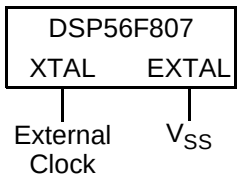


Figure 9. Connecting an External Clock Signal using XTAL

It is possible to instead drive EXTAL with an external clock, though this is not the recommended method. If you elect to drive EXTAL with an external clock source the following conditions must be met:

1. XTAL must be completely un-loaded,
2. the maximum frequency of the applied clock must be less than 8 MHz.

Figure 10 illustrates how to connect an external clock circuit with a external clock source using EXTAL as the input.

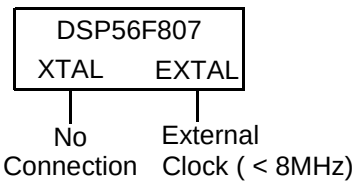


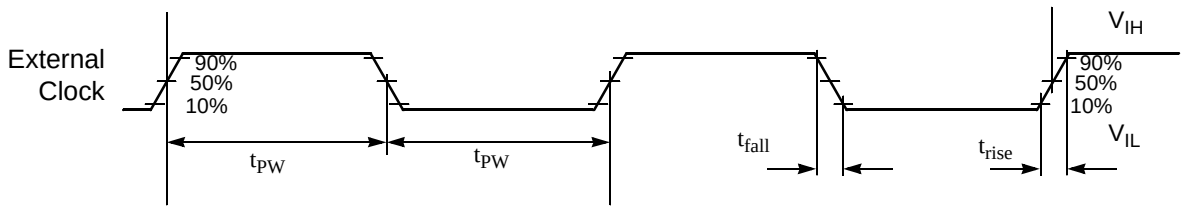
Figure 10. Connecting an External Clock Signal using EXTAL

Table 28. External Clock Operation Timing Requirements[5]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	-	80	MHz
Clock Pulse Width[2]	t_{PW}	6.25	—	—	ns
External clock input rise time[3]	t_{rise}	—	—	3	ns
External clock input fall time[4]	t_{fall}	—	—	3	ns

1. See Figure 9 for details on using the recommended connection of an external clock driver.
2. The high or low pulse width must be no smaller than 6.25 ns or the chip will not function.
3. External clock input rise time is measured from 10% to 90%.
4. External clock input fall time is measured from 90% to 10%.
5. Parameters listed are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 11. External Clock Timing

Table 29. PLL Timing

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	4	8	8	MHz
PLL output frequency	f_{op}	40	—	80	MHz
PLL stabilization time [2]	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input crystal.
2. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

3.6 External Bus Asynchronous Timing

Table 30. External Bus Asynchronous Timing[1,2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{op} = 80$ MHz

Characteristic	Symbol	Typical Min	Typical Max	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	6.5	—	ns
$\overline{WR}$ Width Asserted Wait states = 0 Wait states > 0	t_{WR}	 7.5 (T*WS)+7.5	 — —	 ns ns
$\overline{WR}$ Asserted to D0–D15 Out Valid	t_{WRD}	—	T + 4.2	ns
Data Out Hold Time from $\overline{WR}$ Deasserted	t_{DOH}	4.8	—	ns
Data Out Set Up Time to $\overline{WR}$ Deasserted Wait states = 0 Wait states > 0	t_{DOS}	 6.4 (T*WS)+6.4	 — —	 ns ns
$\overline{RD}$ Deasserted to Address Not Valid	t_{RDA}	0	—	ns
Address Valid to $\overline{RD}$ Deasserted Wait states = 0 Wait states > 0	t_{ARDD}	 18.7 (T*WS) + 18.7	— 	 ns ns
Input Data Hold to $\overline{RD}$ Deasserted	t_{DRD}	0	—	ns
$\overline{RD}$ Assertion Width Wait states = 0 Wait states > 0	t_{RD}	 19 (T*WS)+19	 — —	 ns ns
Address Valid to Input Data Valid Wait states = 0 Wait states > 0	t_{AD}	 — —	 1 (T*WS)+1	 ns ns
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}	-4.4	—	ns
$\overline{RD}$ Asserted to Input Data Valid Wait states = 0 Wait states > 0	t_{RDD}	 — —	 2.4 (T*WS) + 2.4	 ns ns
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}	6.8	—	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}	0	—	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	14.1	—	ns
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}	12.8	—	ns

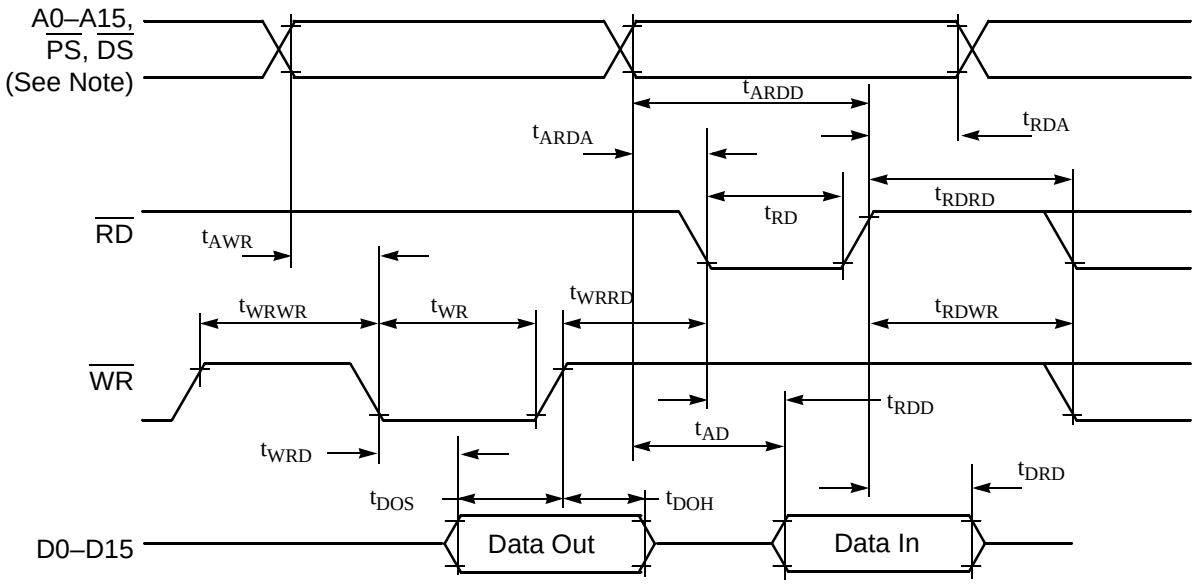
1. Timing is both wait state and frequency dependent. In the formulas listed, WS = the number of wait states and T = Clock Period. For 80 MHz operation, T = 12.5ns.
2. Parameters listed are guaranteed by design.

To calculate the required access time for an external memory for any frequency < 80 Mhz, use this formula:

Top = Clock period @ desired operating frequency

WS = Number of wait states

Memory Access Time = (Top*WS) + (Top- 11.5)



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 12. External Bus Asynchronous Timing

3.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 31. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,5]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	21	ns	Figure 13
Minimum $\overline{\text{RESET}}$ Assertion Duration[2] OMR Bit 6 = 0 OMR Bit 6 = 1	t_{RA}	 275,000T 128T	 — —	 ns ns	Figure 13
$\overline{\text{RESET}}$ De-assertion to First External Address Output	t_{RDA}	33T	34T	ns	Figure 13
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	Figure 14
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	—	15T	ns	Figure 15
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	—	16T	ns	Figure 15
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[3]	t_{IRI}	—	13T	ns	Figure 16

Table 31. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,5] (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[4]	t_{IW}	—	2T	ns	Figure 17
Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IF}	 — —	 275,000T 12T	 ns ns	Figure 17
Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Cause the Fetch of First $\overline{\text{IRQA}}$ Interrupt Instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IRQ}	 — —	 275,000T 12T	 ns ns	Figure 18
Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to First Interrupt Vector Address Out Valid (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{II}	 — —	 275,000T 12T	 ns ns	Figure 18

1. In the formulas, T = clock cycle. For an operating frequency of 80 MHz, T = 12.5 ns.
2. Circuit stabilization delay is required during reset when using an external clock or crystal oscillator in two cases:
   - After power-on reset
   - When recovering from Stop state
3. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
4. The interrupt instruction fetch is visible on the pins only in Mode 3.
5. Parameters listed are guaranteed by design.

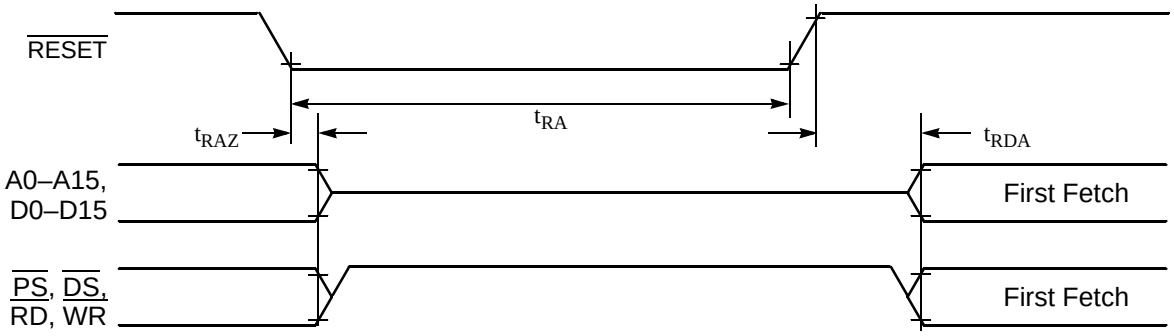


Figure 13. Asynchronous Reset Timing

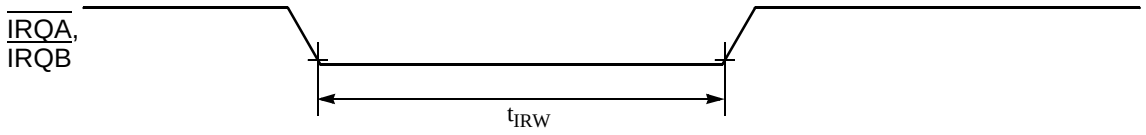


Figure 14. External Interrupt Timing (Negative-Edge-Sensitive)

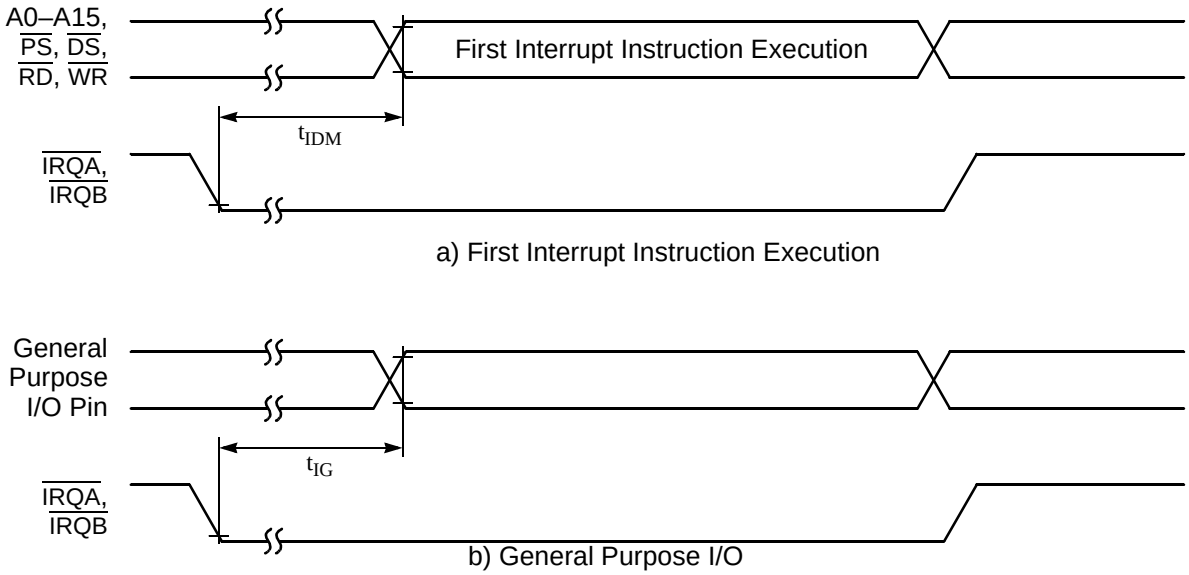


Figure 15. External Level-Sensitive Interrupt Timing

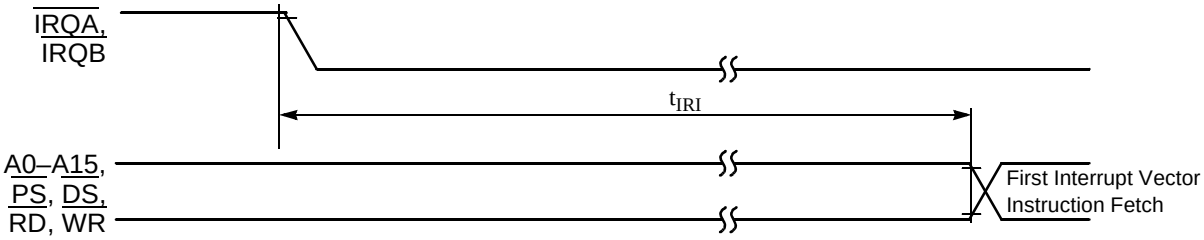


Figure 16. Interrupt from Wait State Timing

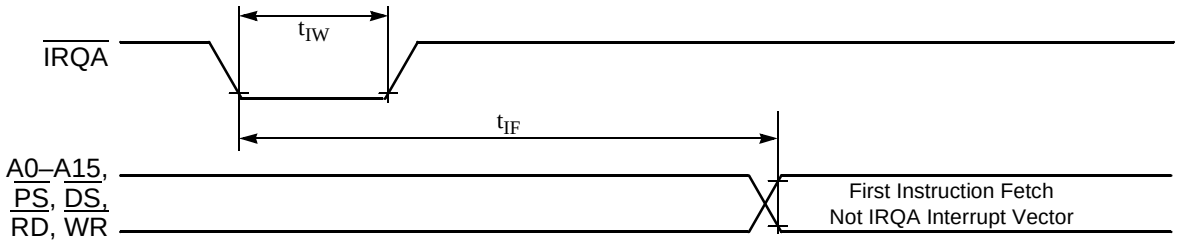


Figure 17. Recovery from Stop State Using Asynchronous Interrupt Timing

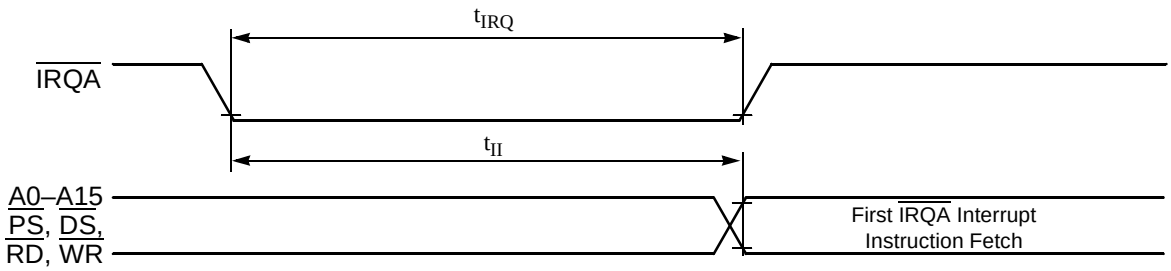


Figure 18. Recovery from Stop State Using IRQA Interrupt Service

3.8 Serial Peripheral Interface (SPI) Timing

Table 32. SPI Timing[1]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 50	 — —	 ns ns	Figures 19-22
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure 22
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure 22
Clock (SCK) high time Master Slave	t_{CH}	 17.6 25	 — —	 ns ns	Figures 19, 20, 21, 22
Clock (SCK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	Figure 22
Data setup time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures 19, 20, 21, 22
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures 19, 20, 21, 22
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	Figure 22
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	Figure 22
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures 19, 20, 21, 22

Table 32. SPI Timing[1] (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$MHz

Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures 19, 20, 21, 22
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures 19, 20, 21, 22
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures 19, 20, 21, 22

1. Parameters listed are guaranteed by design.

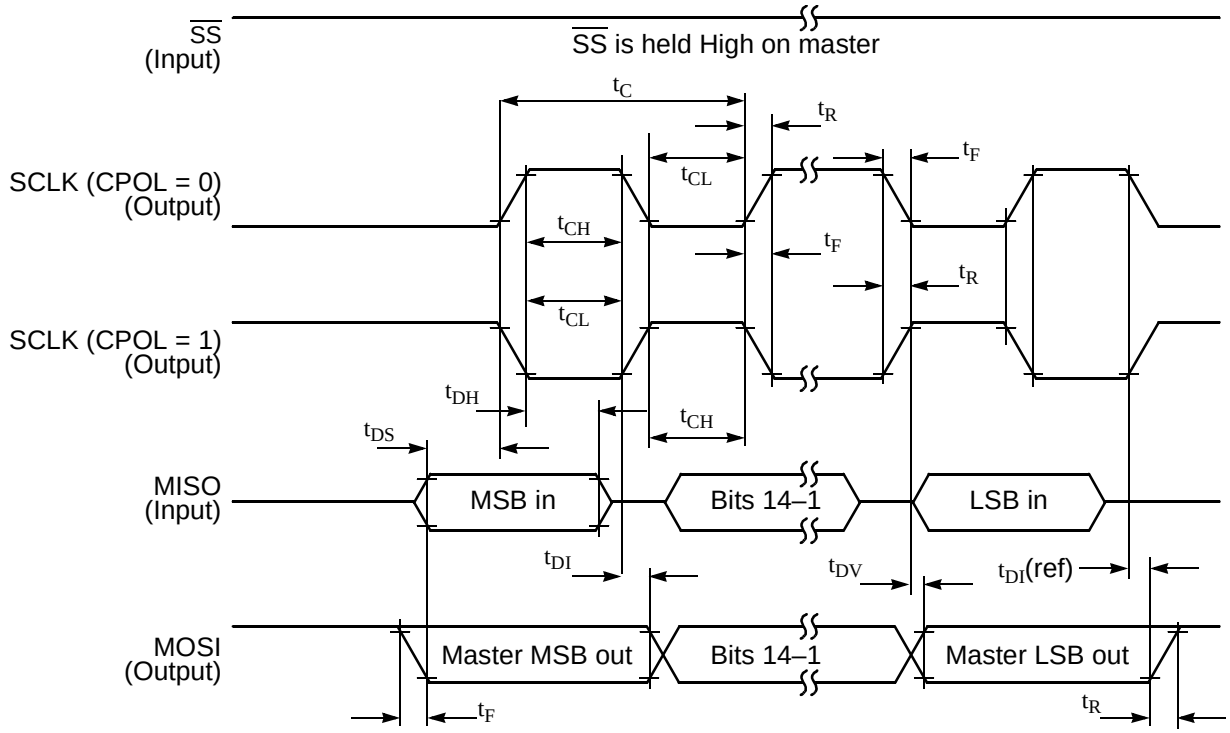


Figure 19. SPI Master Timing (CPHA = 0)

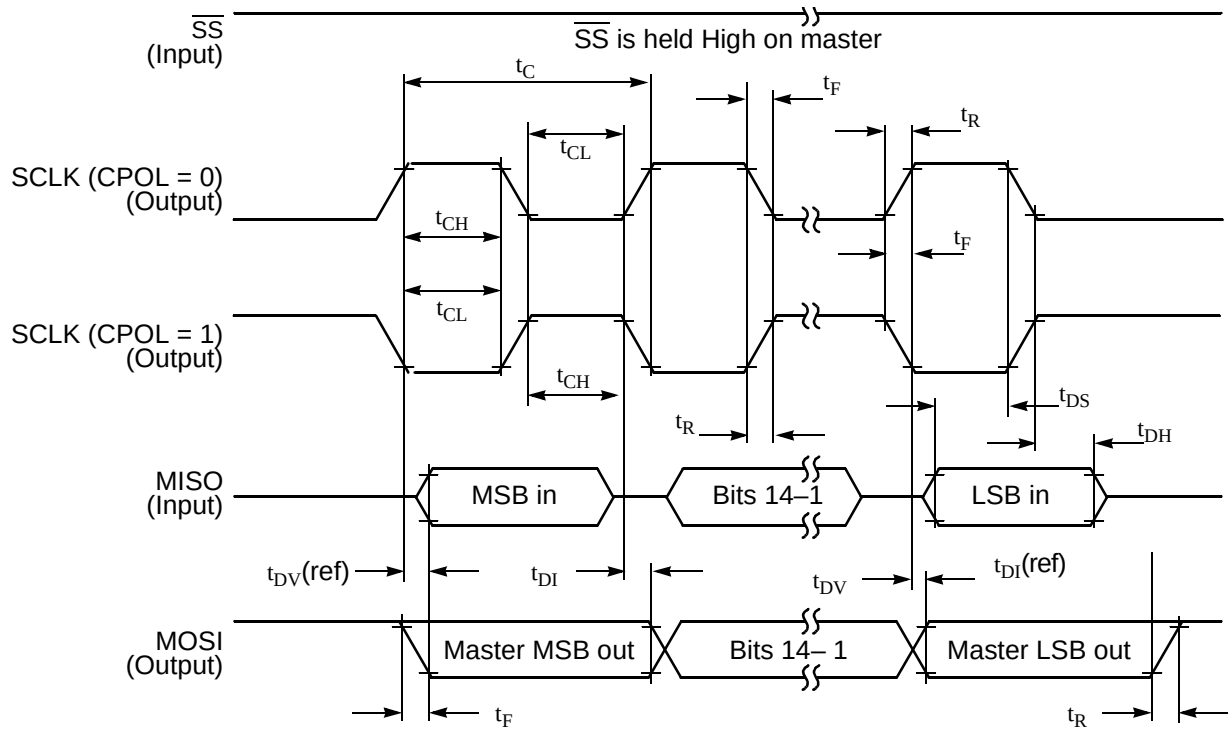


Figure 20. SPI Master Timing (CPHA = 1)

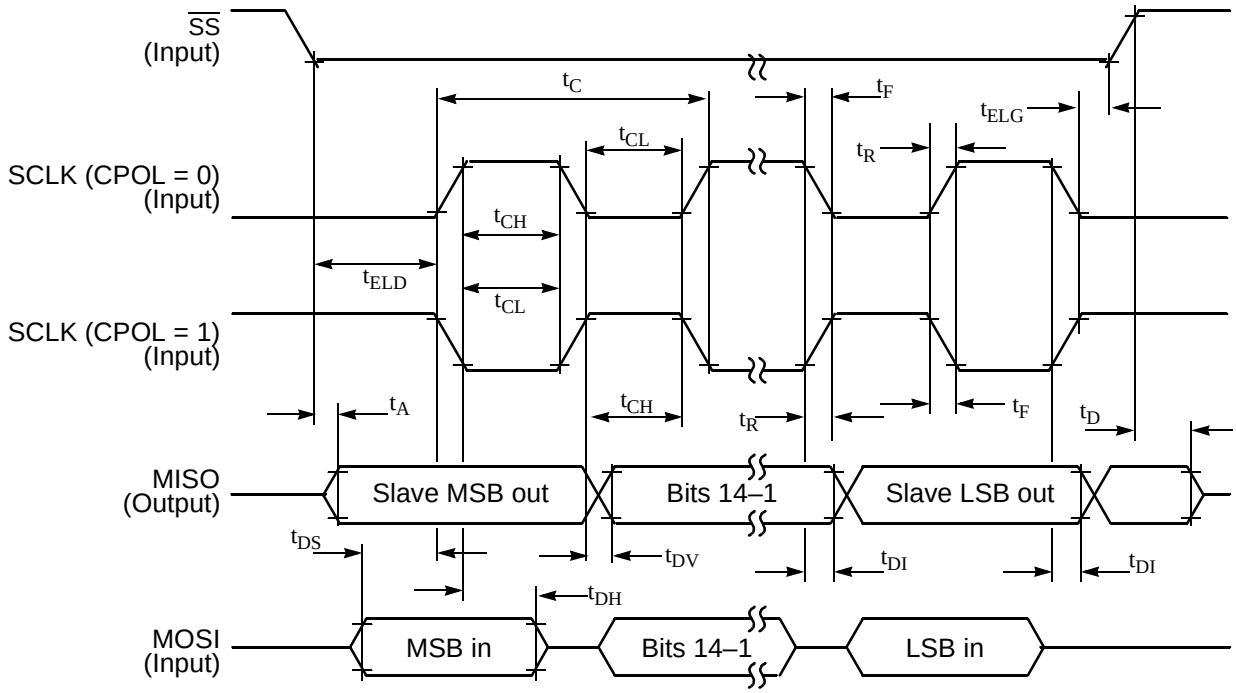


Figure 21. SPI Slave Timing (CPHA = 0)

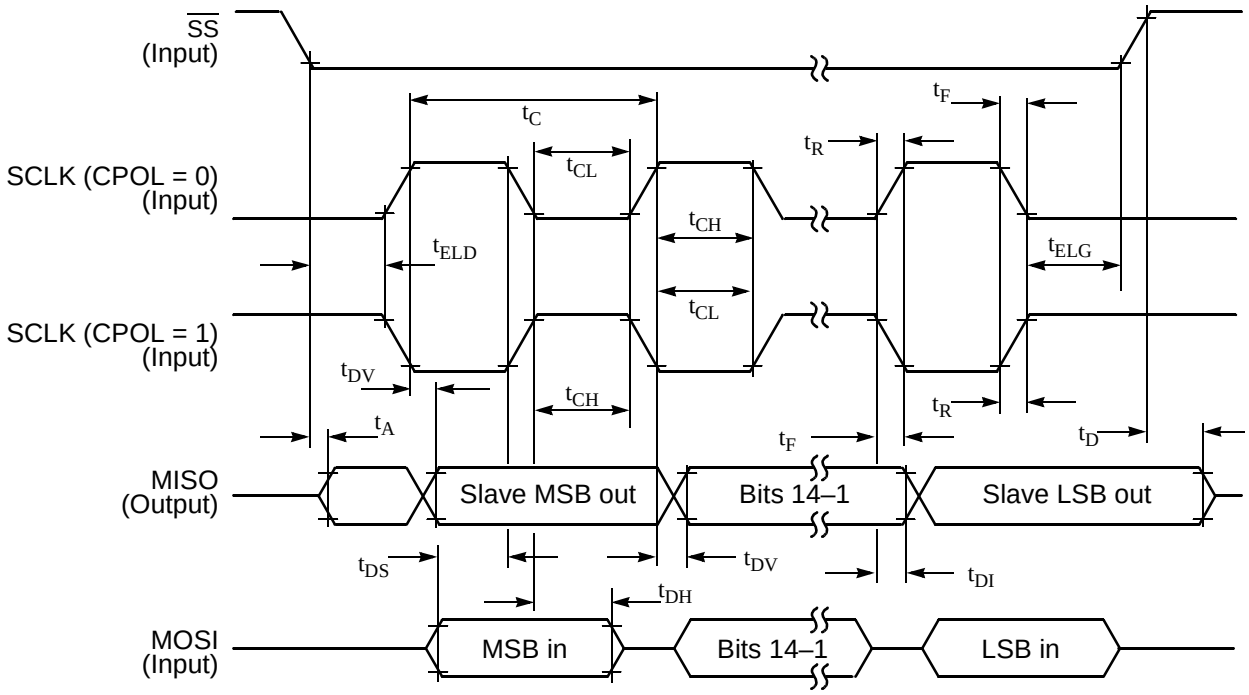


Figure 22. SPI Slave Timing (CPHA = 1)

3.9 Quad Timer Timing

Table 33. Timer Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	4T + 6	—	ns
Timer input high/low period	P_{INHL}	2T + 3	—	ns
Timer output period	P_{OUT}	2T - 3	—	ns
Timer output high/low period	P_{OUTHL}	1T - 3	—	ns

1. In the formulas listed, T = the clock cycle. For 80 MHz operation, T = 12.5 ns.
2. Parameters listed are guaranteed by design.

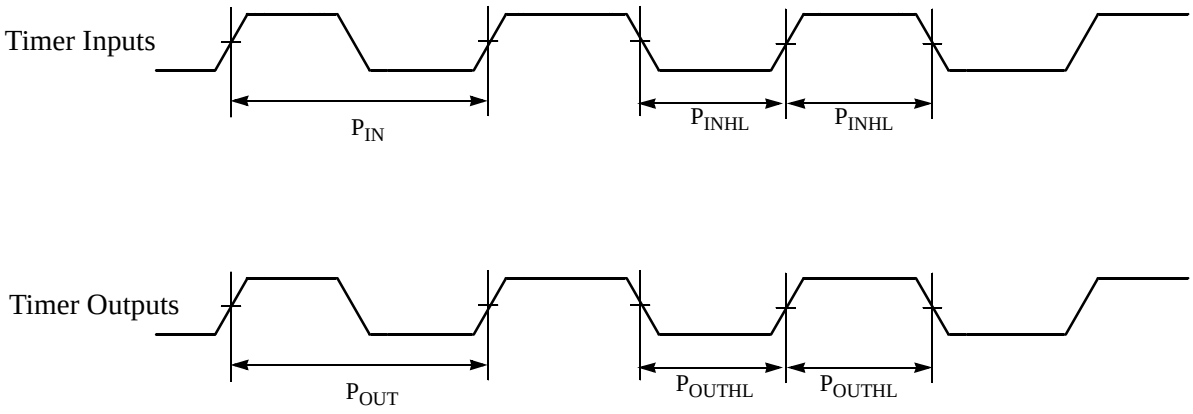


Figure 23. Timer Timing

3.10 Quadrature Decoder Timing

Table 34. Quadrature Decoder Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Quadrature input period	P_{IN}	8T + 12	—	ns
Quadrature input high/low period	P_{HL}	4T + 6	—	ns
Quadrature phase period	P_{PH}	2T + 3	—	ns

1. In the formulas listed, T = the clock cycle. For 80 MHz operation, T=12.5 ns. $V_{SS} = 0$ V, $V_{DD} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF.
2. Parameters listed are guaranteed by design.

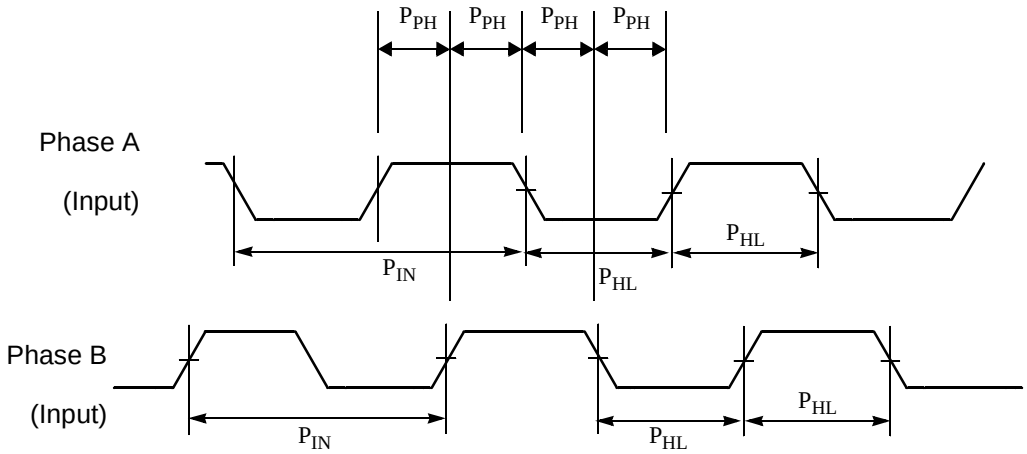


Figure 24. Quadrature Decoder Timing

3.11 Serial Communication Interface (SCI) Timing

Table 35. SCI Timing[4]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	$(f_{MAX}*2.5)/(80)$	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

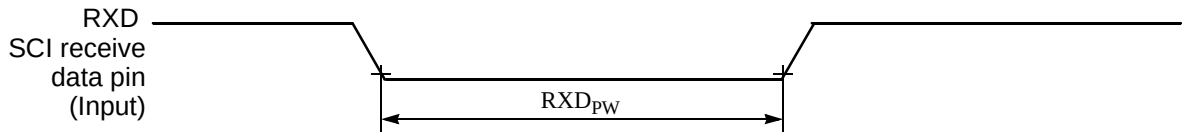


Figure 25. RXD Pulse Width

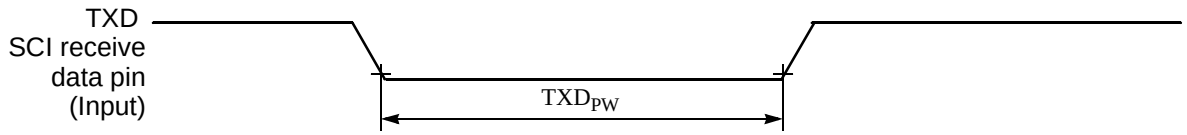


Figure 26. TXD Pulse Width

3.12 Analog-to-Digital Converter (ADC) Timing

Table 36. ADC Timing

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$ MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input voltages	V_{ADIN}	0	—	V_{REFH}	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity	INL	—	+/- 3	TBD	LSB[1]
Differential Non-Linearity	DNL	—	+/- .8	TBD	LSB[1]
Monotonicity	GUARANTEED				
ADC internal clock	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{SSA}	—	V_{DDA}	V

Table 36. ADC Timing (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to +85°C, $C_L \leq 50$ pF, $f_{OP} = 80$ MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Power-up time	t_{ADPU}	—	16	—	t_{AIC} cycles[2]
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[2]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[2]
Input capacitance	C_{ADI}	—	5	—	pF[3]
V_{REF} current	I_{VREF}	—	—	11.85	mA
Gain Error (transfer gain)	E_{GAIN}	—	TBD	—	—
Offset Voltage	V_{OFFSET}	—	TBD	TBD	mV
SINAD	SINAD	—	59	—	—
ENOB	ENOB	—	9.5	—	bit
SFDR	SFDR	—	64	—	db

1. LSB = Least Significant Bit.
2. $t_{AIC} = 1/f_{ADIC}$.
3. See Figure 27

NOTE:

I_{ADC} quiescent current (both ADCs) is 39.3 mA

I_{VREF} quiescent current (both ADCs) is 11.85 mA

Typical values measured at $V_{DD} = 3.3$, $V_{REF} = 3.0$

V_{REF} must be equal to or less than V_{DD}

V_{REF} can go as low as 2.7V.

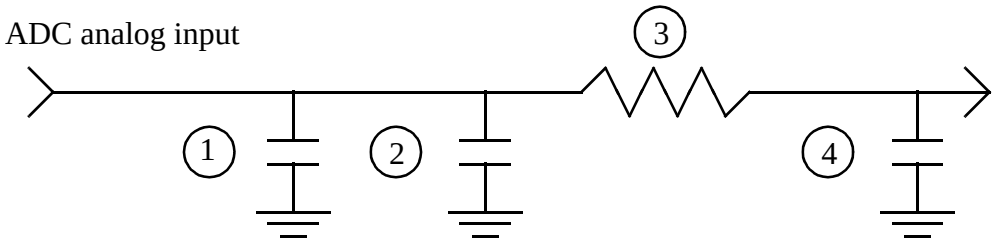


Figure 27. Equivalent Analog Input Circuit

1. Parasitic capacitance due to package, pin to pin, and pin to package base coupling. 1.8pf
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing. 2.04pf
3. Equivalent resistance for the ESD isolation resistor and the channel select mux. 500 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor 4 is normally disconnected from the input and is only connected to it at sampling time. 1pf

3.13 Controller Area Network (CAN) Timing

Table 37. CAN Timing[2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, MSCAN Clock = 30 MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
Bus Wakeup detection [1]	T_{WAKEUP}	5	—	us

1. If Wakeup glitch filter is enabled during the design initialization and also CAN is put into SLEEP mode then, any bus event (on MSCAN_RX pin) whose duration is less than 5 microseconds is filtered away. However, a valid CAN bus wakeup detection takes place for a wakeup pulse equal to or greater than 5 microseconds. The number 5 microseconds originates from the fact that the CAN wakeup message consists of 5 dominant bits at the highest possible baud rate of 1 Mbps.
2. Parameters listed are guaranteed by design

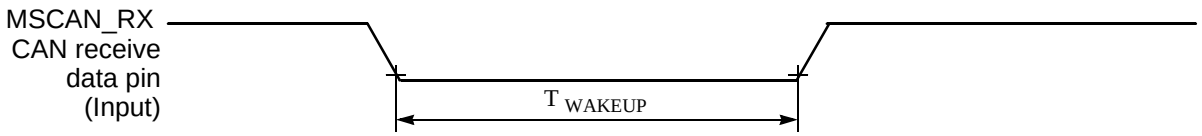


Figure 28. Bus Wakeup Detection

3.14 JTAG Timing

Table 38. JTAG Timing[1, 3]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$ pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	10	MHz
TCK cycle time	t_{CY}	100	—	ns
TCK clock pulse width	t_{PW}	50	—	ns
TMS, TDI data setup time	t_{DS}	0.4	—	ns
TMS, TDI data hold time	t_{DH}	1.2	—	ns
TCK low to TDO data valid	t_{DV}	—	26.6	ns
TCK low to TDO tri-state	t_{TS}	—	23.5	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	50	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 80 MHz operation, T = 12.5 ns.
2. TCK frequency of operation must be less than 1/8 the processor rate.
3. Parameters listed are guaranteed by design.

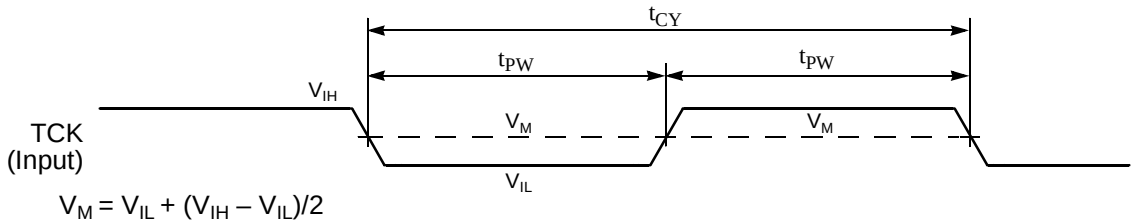


Figure 29. Test Clock Input Timing Diagram

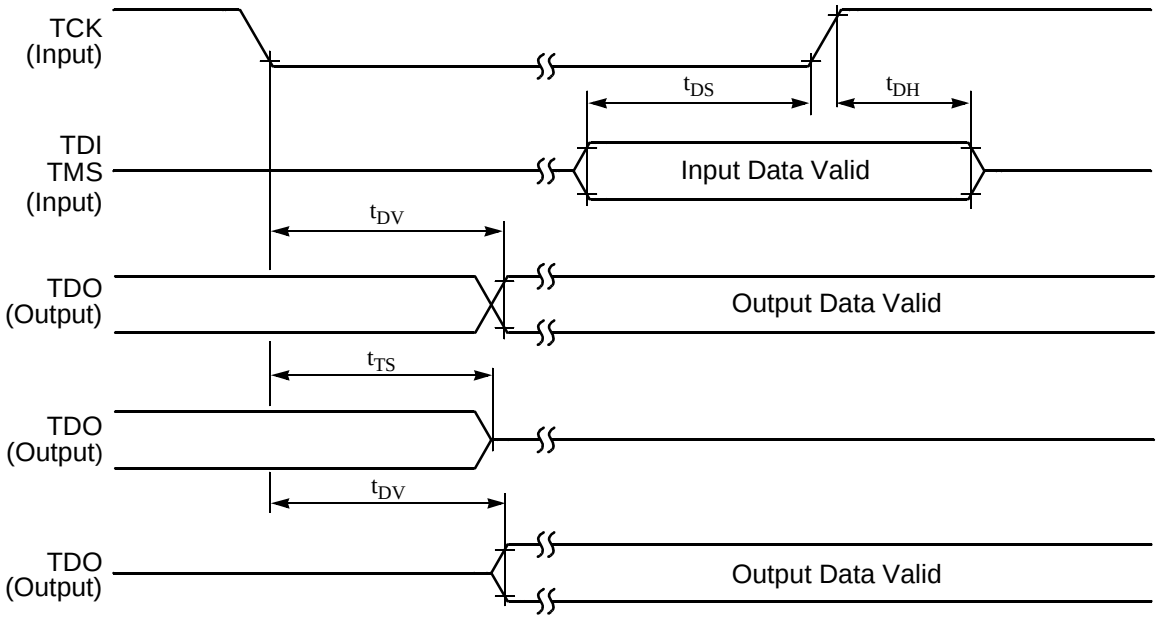


Figure 30. Test Access Port Timing Diagram

Figure 31. $\overline{\text{TRST}}$ Timing Diagram

Figure 32. OnCE—Debug Event

Part 4 Packaging

4.1 Package and Pin-Out Information DSP56F807

This section contains package and pin-out information for the DSP56F807. This device comes in two case types: low-profile quad flat pack (LQFP) or mold array process ball grid assembly (MAPBGA). **Figure 33** shows the package outline for the LQFP case, **Figure 34** shows the mechanical parameters for the LQFP case, and **Table 39** lists the pinout for the LQFP case. **Figure 35** shows the mechanical parameters for the MAPBGA case, and **Table 40** lists the pinout for the MAPBGA package.

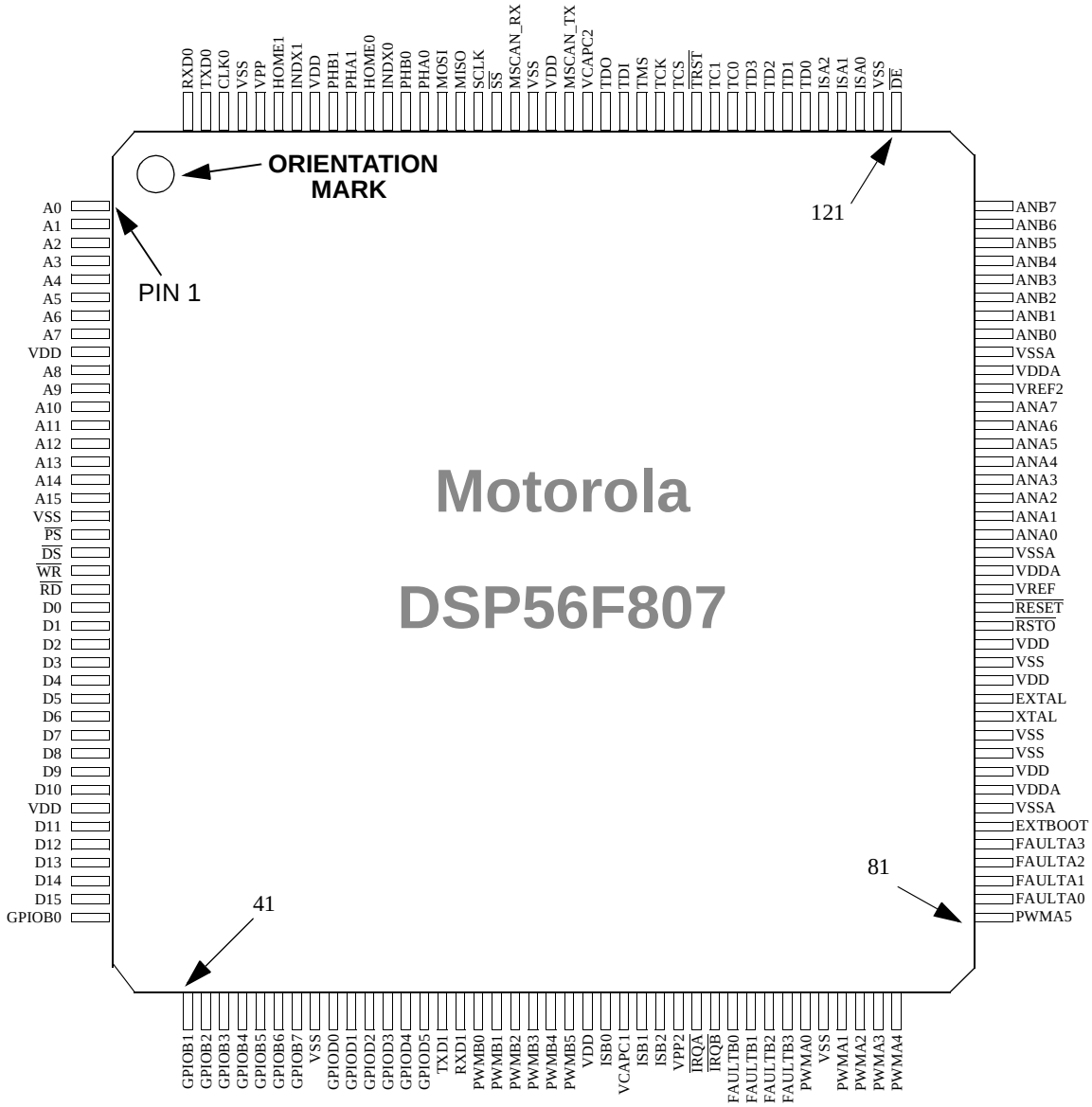
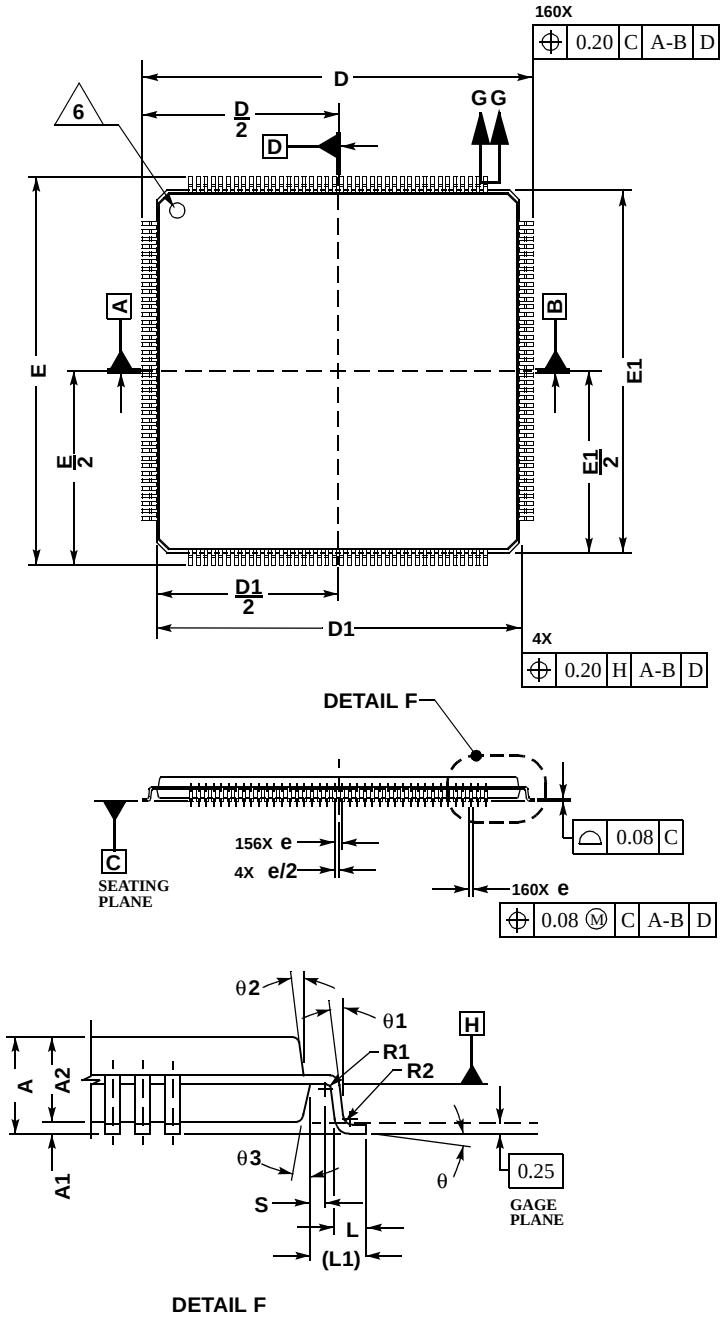
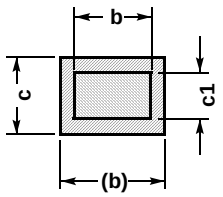


Figure 33. Top View, DSP56F807 160-pin LQFP Package





SECTION G-G

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. EXACT SHAPE OF CORNERS MAY VARY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	26.00 BSC	
D1	24.00 BSC	
e	0.50 BSC	
E	26.00 BSC	
E1	24.00 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	---
R2	0.08	0.20
S	0.20	---
θ	0°	7°
θ1	0°	---
θ2	11°	13°
θ3	11°	13°

CASE 1259-01
ISSUE O

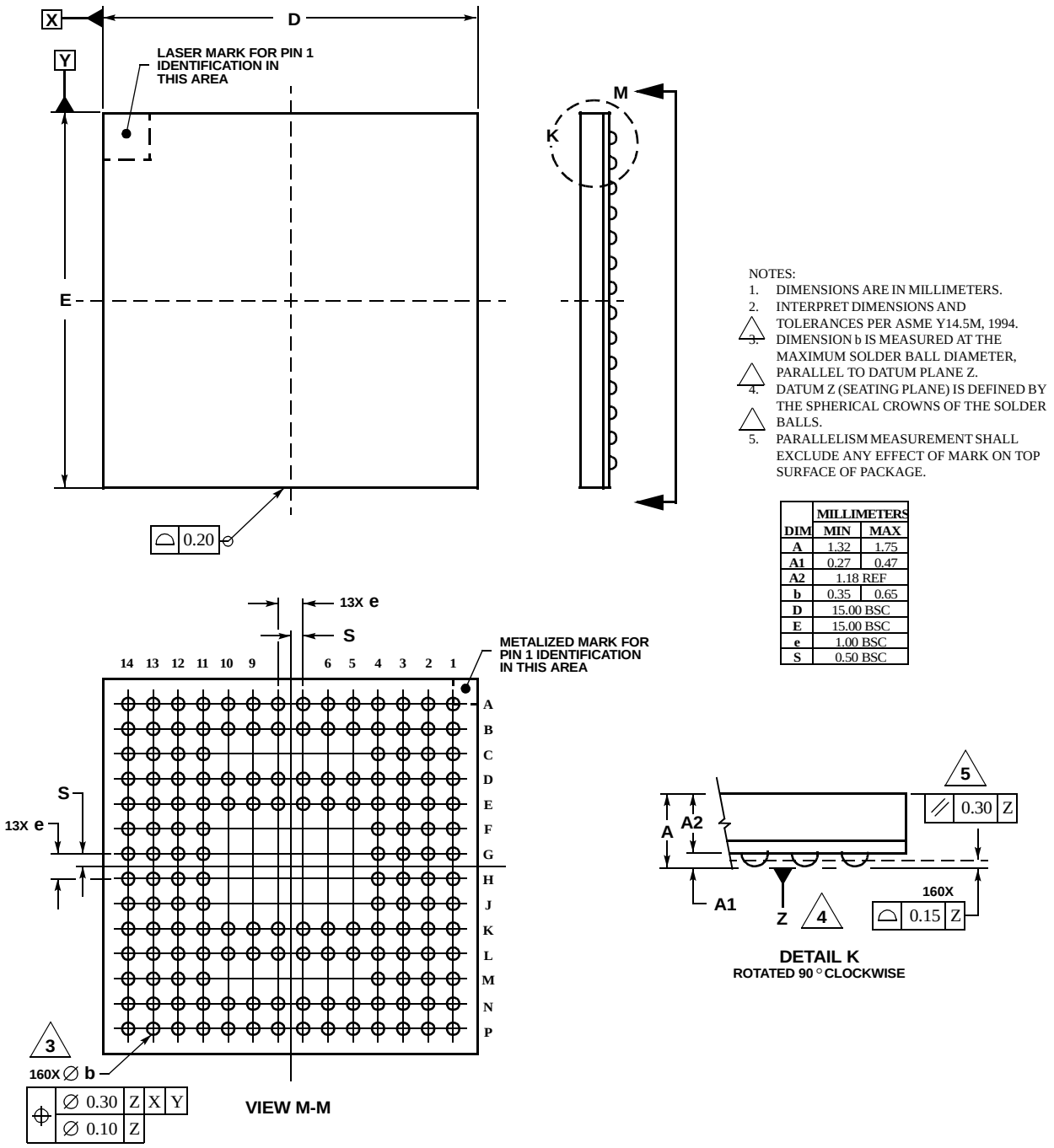
Figure 34. 160-pin LQFP Mechanical Information

Table 39. DSP56F807 LQFP Package Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	A0	41	GPIOB1	81	PWMA5	121	$\overline{DE}$
2	A1	42	GPIOB2	82	FAULTA0	122	V_{SS}
3	A2	43	GPIOB3	83	FAULTA1	123	ISA0
4	A3	44	GPIOB4	84	FAULTA2	124	ISA1
5	A4	45	GPIOB5	85	FAULTA3	125	ISA2
6	A5	46	GPIOB6	86	EXTBOOT	126	TD0
7	A6	47	GPIOB7	87	V_{SSA}	127	TD1
8	A7	48	V_{SS}	88	V_{DDA}	128	TD2
9	V_{DD}	49	GPIOD0	89	V_{DD}	129	TD3
10	A8	50	GPIOD1	90	V_{SS}	130	TC0
11	A9	51	GPIOD2	91	V_{SS}	131	TC1
12	A10	52	GPIOD3	92	XTAL	132	$\overline{TRST}$
13	A11	53	GPIOD4	93	EXTAL	133	TCS
14	A12	54	GPIOD5	94	V_{DD}	134	TCK
15	A13	55	TXD1	95	V_{SS}	135	TMS
16	A14	56	RXD1	96	V_{DD}	136	TDI
17	A15	57	PWMB0	97	$\overline{RSTO}$	137	TDO
18	V_{SS}	58	PWMB1	98	$\overline{RESET}$	138	VCAPC2
19	$\overline{PS}$	59	PWMB2	99	VREF	139	MSCAN_TX
20	$\overline{DS}$	60	PWMB3	100	V_{DDA}	140	V_{DD}
21	$\overline{WR}$	61	PWMB4	101	V_{SSA}	141	V_{SS}
22	$\overline{RD}$	62	PWMB5	102	ANA0	142	MSCAN_RX
23	D0	63	V_{DD}	103	ANA1	143	$\overline{SS}$
24	D1	64	ISB0	104	ANA2	144	SCLK
25	D2	65	VCAPC1	105	ANA3	145	MISO
26	D3	66	ISB1	106	ANA4	146	MOSI
27	D4	67	ISB2	107	ANA5	147	PHA0

Table 39. DSP56F807 LQFP Package Pin Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
28	D5	68	VPP2	108	ANA6	148	PHB0
29	D6	69	$\overline{\text{IRQA}}$	109	ANA7	149	INDX0
30	D7	70	$\overline{\text{IRQB}}$	110	VREF2	150	HOME0
31	D8	71	FAULTB0	111	V_{DDA}	151	PHA1
32	D9	72	FAULTB1	112	V_{SSA}	152	PHB1
33	D10	73	FAULTB2	113	ANB0	153	V_{DD}
34	V_{DD}	74	FAULTB3	114	ANB1	154	INDX1
35	D11	75	PWMA0	115	ANB2	155	HOME1
36	D12	76	V_{SS}	116	ANB3	156	VPP
37	D13	77	PWMA1	117	ANB4	157	V_{SS}
38	D14	78	PWMA2	118	ANB5	158	CLKO
39	D15	79	PWMA3	119	ANB6	159	TXD0
40	GPIOB0	80	PWMA4	120	ANB7	160	RXD0



CASE 1268-01
ISSUE O

DATE 04/06/98

Figure 35. 160 MAPBGA Mechanical Information

Table 40. 160 MAPBGA Package Pin Identification by Pin Number

Solder Ball	Signal Name	Solder Ball	Signal Name	Solder Ball	Signal Name	Solder Ball	Signal Name
C3	A0	N4	GPIOB5	K12	V_{SSA}	E10	TC1
B2	A1	P4	GPIOB6	K13	V_{DDA}	D9	$\overline{TRST}$
D3	A2	M4	GPIOB7	L14	V_{DD}	B9	TCS
C2	A3	L5	V_{SS}	K11	V_{SS}	E9	TCK
B1	A4	N5	GPIOD0	K14	V_{SS}	A9	TMS
D2	A5	P5	GPIOD1	J13	XTAL	D8	TDI
C1	A6	K5	GPIOD2	J12	EXTAL	B8	TDO
D1	A7	N6	GPIOD3	J14	V_{DD}	A8	VCAPC2
E3	V_{DD}	L6	GPIOD4	J11	V_{SS}	E8	MSCAN_TX
E2	A8	K6	GPIOD5	H13	VDD	D7	V_{DD}
E1	A9	P6	TXD1	H12	$\overline{RSTO}$	E7	V_{SS}
F3	A10	N7	RXD1	H14	$\overline{RESET}$	D6	MSCAN_RX
F2	A11	L7	PWMB0	H11	VREF	H1	D1
F1	A12	P7	PWMB1	G12	V_{DDA}	H2	D2
G3	A13	K7	PWMB2	G11	V_{SSA}	J3	D3
G2	A14	L8	PWMB3	G14	ANA0	J1	D4
G1	A15	K8	PWMB4	B13	$\overline{DE}$	J2	D5
F4	V_{SS}	P8	PWMB5	A14	V_{SS}	K3	D6
G4	$\overline{PS}$	L9	V_{DD}	B12	ISA0	K1	D7
H4	$\overline{DS}$	N8	ISB0	A13	ISA1	L1	D8
J4	$\overline{WR}$	P14	PWMA5	A12	ISA2	K2	D9
K4	$\overline{RD}$	M13	FAULTA0	B11	TD0	L3	D10
P1	GPIOB1	L12	FAULTA1	A11	TD1	M1	V_{DD}
N3	GPIOB2	N14	FAULTA2	D10	TD2	L2	D11
P2	GPIOB3	L13	FAULTA3	B10	TD3	N1	D12
P3	GPIOB4	M14	EXTBOOT	A10	TC0	M2	D13

Table 40. 160 MAPBGA Package Pin Identification by Pin Number (Continued)

Solder Ball	Signal Name	Solder Ball	Signal Name	Solder Ball	Signal Name	Solder Ball	Signal Name
N2	D14	N11	V_{SS}	D14	V_{SSA}	D5	PHB0
M3	D15	P13	PWMA1	D11	ANA8	B6	INDX0
L4	GPIOB0	N12	PWMA2	D12	ANA9	A5	HOME0
K10	VCAPC1	N13	PWMA3	D13	ANA10	E4	PHA1
K9	ISB1	M12	PWMA4	C14	ANA11	B5	PHB1
P9	ISB2	F11	ANA1	C13	ANA12	A4	V_{DD}
L10	VPP2	G13	ANA2	C11	ANA13	D4	INDX1
N9	$\overline{\text{IRQA}}$	F12	ANA3	B14	ANA14	C4	HOME1
P10	$\overline{\text{IRQB}}$	F14	ANA4	C12	ANA15	B4	VPP
P11	FAULTB0	E11	ANA5	A7	$\overline{\text{SS}}$	A2	CLKO
N10	FAULTB1	F13	ANA6	E5	SCLK	B3	TXD0
L11	FAULTB2	E12	ANA7	B7	MISO	A1	RXD0
M11	FAULTB3	E14	VREF2	A6	MOSI	A3	V_{SS}
P12	PWMA0	E13	V_{DDA}	E6	PHA0	H3	D0

Part 5 Design Considerations

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

Definitions:

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

The junction-to-case thermal resistances quoted in this data sheet are determined using the first definition on page 46. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

5.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{DD} or V_{SS}).

Use the following list of considerations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the DSP, and from the board ground to each V_{SS} pin.
- The minimum bypass requirement is to place six 0.01–0.1 µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the ten V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and V_{SS}.
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100 µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS}circuits.

- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the VREF, V_{DDA} and V_{SSA} pins.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. Designs that do not require debugging functionality, such as consumer products, should tie these pins together.
- Because the Flash memory is programmed through the JTAG/OnCE port, designers should provide an interface to this port to allow in-circuit Flash programming.

Part 6 Ordering Information

Table 41 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 41. DSP56F807 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56F807	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	80	DSP56F807PY80
DSP56F807	3.0–3.6 V	Mold Array Process Ball Grid Array (MAPBGA)	160	80	DSP56F807VF80

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