EPC2107 – Enhancement-Mode GaN Power Transistor Half Bridge With Integrated Synchronous Bootstrap Preliminary Specification Sheet

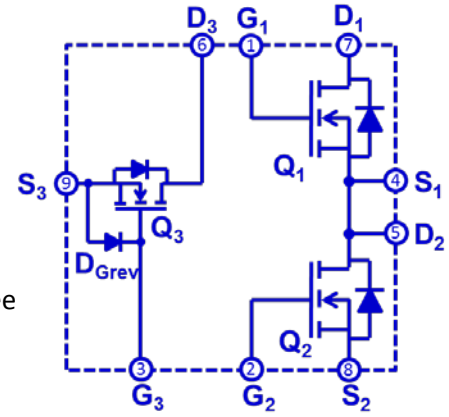
Status: Engineering

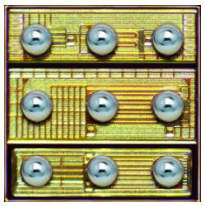
Features:

- V_{DS}, 100 V
- High Frequency Operation
- High Density Footprint
- Low Inductance Package
- Pb-Free (RoHS Compliant), Halogen Free

Applications:

- High Frequency DC-DC Conversion
- Class-D Audio
- Wireless Power (Highly Resonant and Inductive)

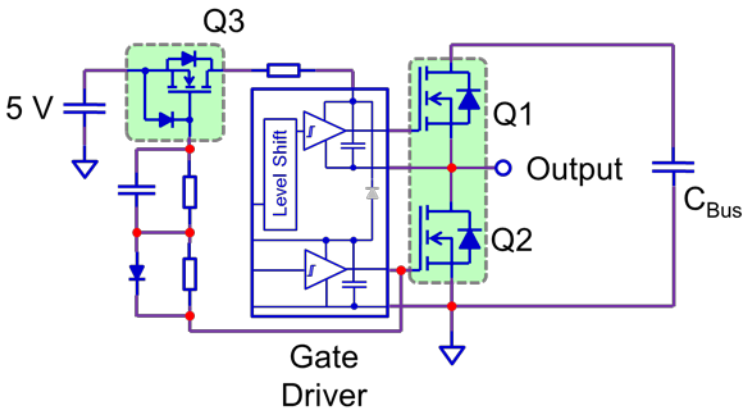




EPC2107 devices are supplied only in passivated die form with solder balls

Die Size: 1.35 mm x 1.35 mm

Typical Circuit



MAXIMUM RATINGS

Parameter	Device	Value
Maximum Drain – Source Voltage	Q1 & Q2	100 V
	Q3	100 V
Maximum Gate – Source Voltage Range	Q1 & Q2	-4 V < V_{GS} < 6 V
	Q3	-2 V < V_{GS} < 6 V
Continuous Drain Current, 25 °C	Q1 & Q2 , $R_{\theta JA}$ = 74 °C/W	1.7 A
	Q3 , $R_{\theta JA}$ = 95 °C/W	0.5 A
Maximum Pulsed Drain Current, 25 °C, T_{pulse} = 300 µs	Q1 & Q2	3.8 A
	Q3	0.5 A
Operating Temperature Range	-40 °C < T_J < 150 °C	

STATIC CHARACTERISTICS

Parameter	Conditions	Q1 & Q2	Q3
Maximum Drain – Source Voltage (BV_{DSS})	V_{GS} = 0 V, I_D = 0.3 mA	100 V	100 V
Maximum Drain – Source Leakage	V_{DS} = 80 V, V_{GS} = 0 V	0.25 mA	0.1 mA
Maximum $R_{DS(on)}$	Q1/Q2: V_{GS} = 5 V, I_D = 2 A Q3: V_{GS} = 5 V, I_D = 0.05 A	320 mΩ	2.8 Ω
Typical $R_{DS(on)}$		240 mΩ	2.1 Ω
Gate – Source Threshold Voltage	Q1/Q2: I_D = 0.1 mA, V_{DS} = V_{GS} Q3: I_D = 0.02 mA, V_{DS} = V_{GS}	0.8 V < $V_{GS(TH)}$ < 2.5 V	
Gate – Source Maximum Positive Leakage	V_{GS} = 5 V	1 mA	1 mA
Gate – Source Maximum Negative Leakage	Q1/Q2: V_{GS} = -4 V Q3: V_{GS} = -1 V	-0.25 mA	-0.1 mA
Source-Gate Maximum Forward Voltage	Q3: I_{SG} = 0.2 mA, V_{DS} = 0 V		-2 V

T_J = 25 °C unless otherwise stated

DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value			
		Q1	Q2	Q3	Unit
C_{ISS} (Input Capacitance)	V_{DS} = 50 V, V_{GS} = 0 V	16		7	pF
C_{OSS} (Output Capacitance)		10	17	1.7	
C_{RSS} (Reverse Transfer Capacitance)		0.3		0.02	
Q_G (Total Gate Charge)	Q1 & Q2: V_{DS} = 50 V, V_{GS} = 5 V, I_D = 2 A	160			pC
	Q3: V_{DS} = 50 V, V_{GS} = 5 V, I_D = 0.05 A			44	
Q_{GS} (Gate to Source Charge)	V_{DS} = 50 V Q1 & Q2: I_D = 2 A Q3: I_D = 0.05 A	65		16	
Q_{GD} (Gate to Drain Charge)		40		5	
$Q_{G(TH)}$ (Gate Charge at Threshold)		38		14	
Q_{OSS} (Output Charge)	V_{DS} = 50 V, V_{GS} = 0 V	800	1400	140	
Q_{RR} (Source-Drain Recovery Charge)		0			

T_J = 25 °C unless otherwise stated

THERMAL CHARACTERISTICS

		TYPICAL	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	6	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board (Note 2)	33	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	81	°C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Thermal models for EPC devices available at http://epc-co.com/epc/DesignSupport/DeviceModels.aspx

Figure 1a: EPC2107-Q1&Q2: Typical Output Characteristics at 25°C

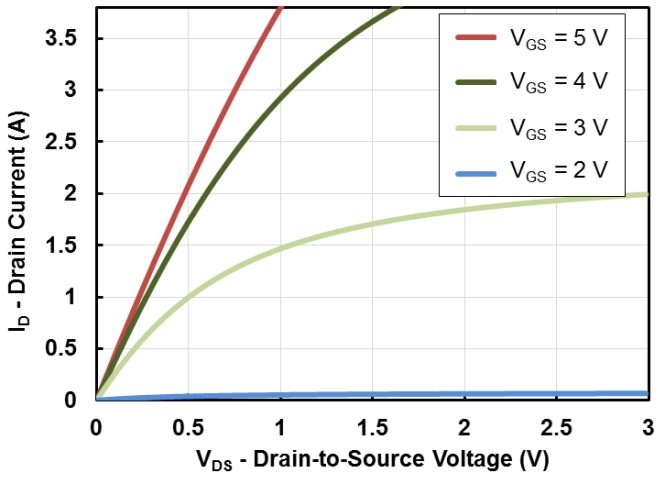


Figure 1b: EPC2107-Q3: Typical Output Characteristics at 25°C

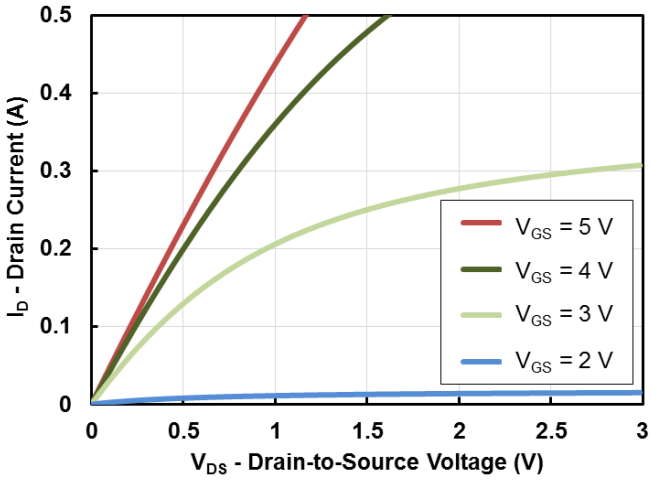


Figure 2a: EPC2107-Q1&Q2: Transfer Characteristics

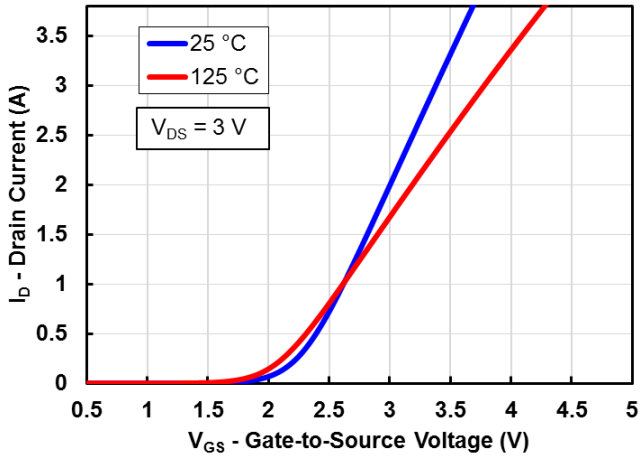


Figure 2b: EPC2107-Q3: Transfer Characteristics

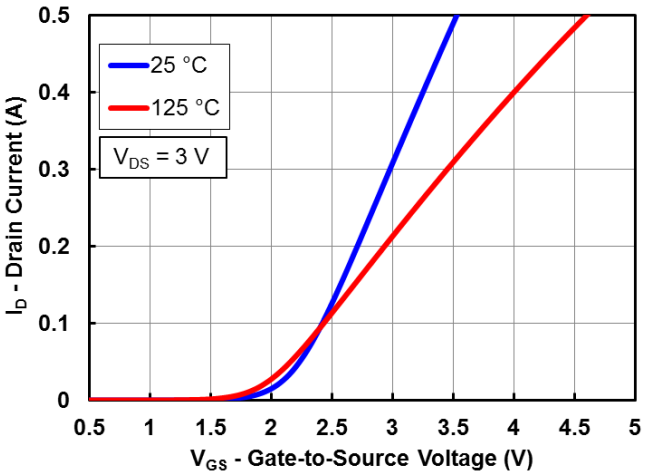


Figure 3a: EPC2107-Q1&Q2: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

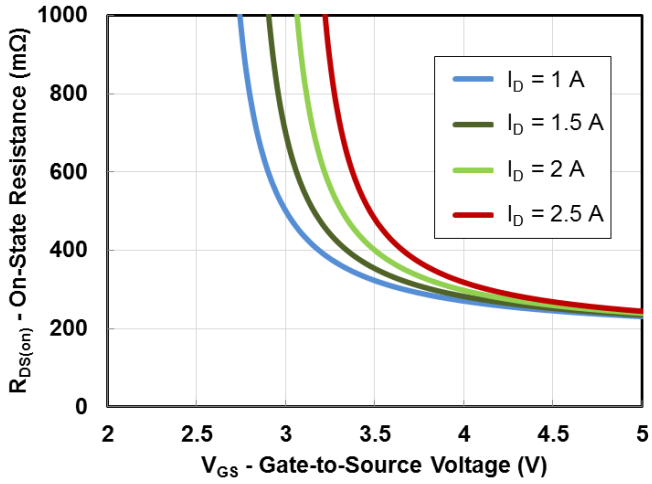


Figure 3b: EPC2107-Q3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

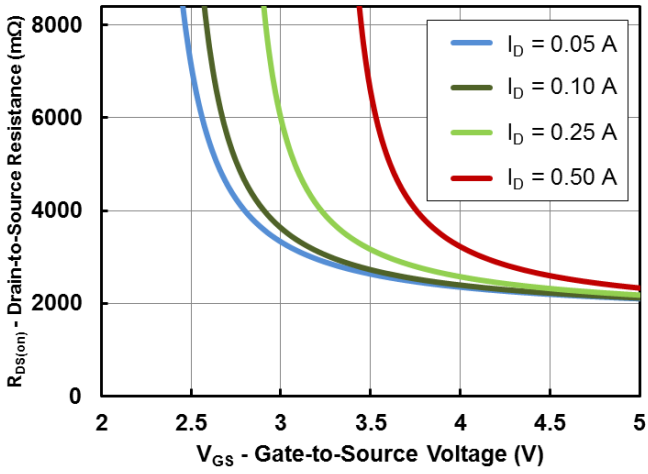


Figure 4a: EPC2107-Q1&Q2: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

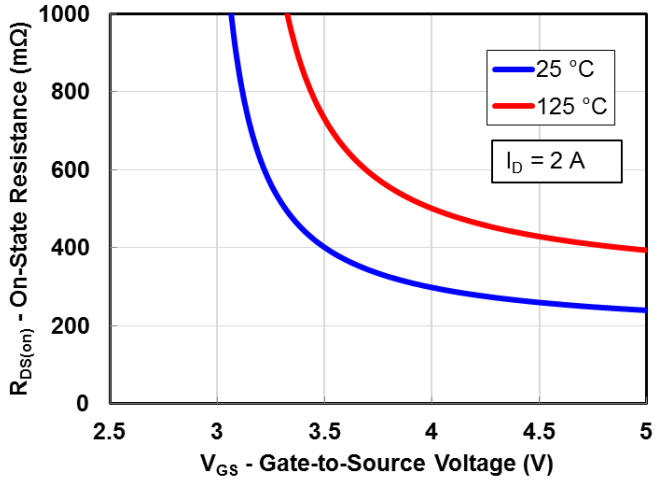


Figure 4b: EPC2107-Q3: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

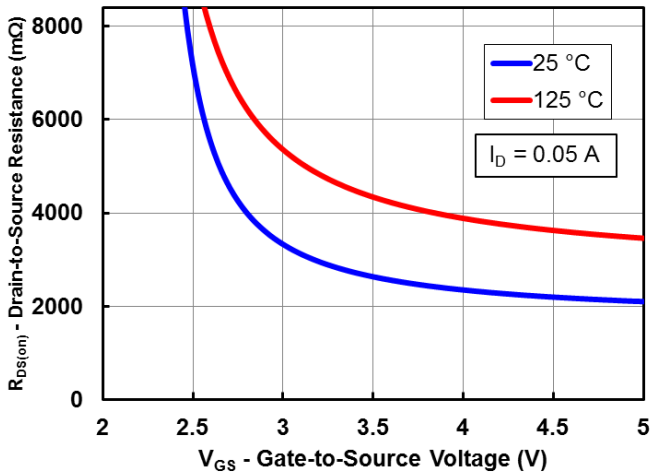


Figure 5a: EPC2107-Q1&Q2: Capacitance (Linear Scale)

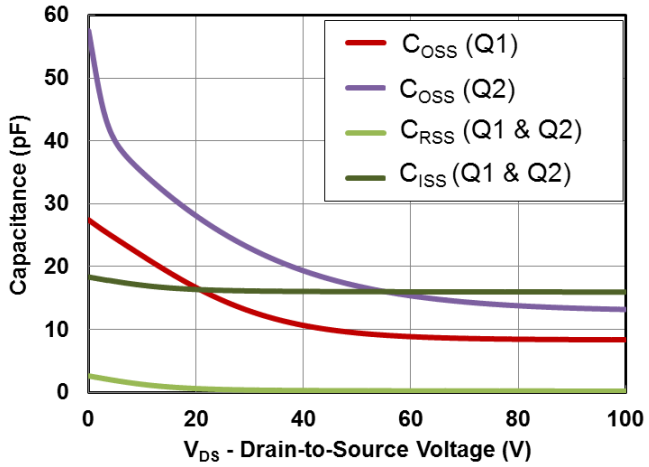


Figure 5b: EPC2107-Q3: Capacitance (Linear Scale)

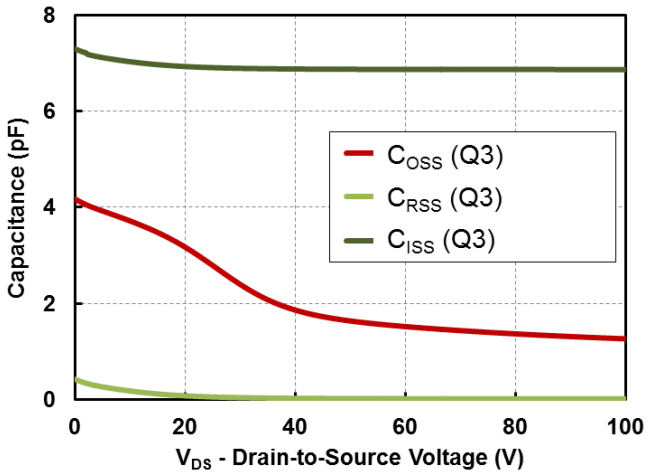


Figure 5c: EPC2107-Q1&Q2: Capacitance (Log Scale)

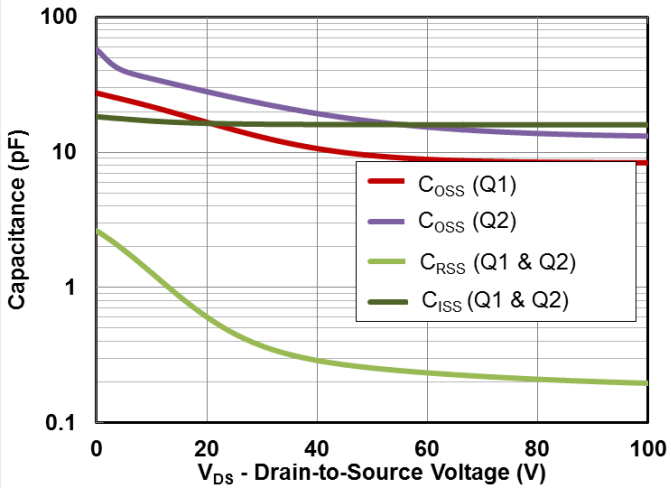


Figure 5d: EPC2107-Q3: Capacitance (Log Scale)

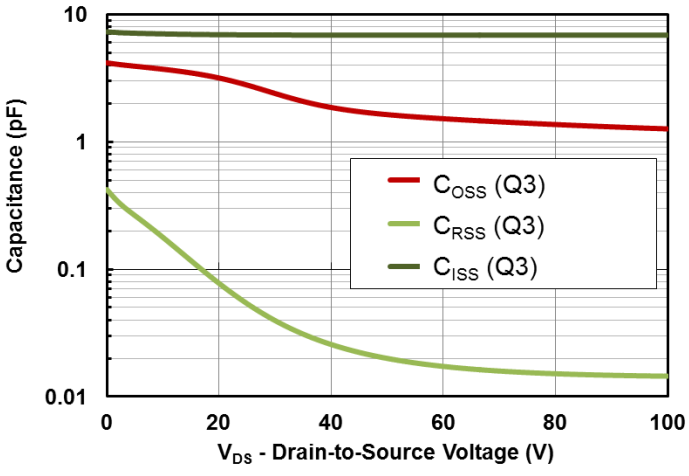


Figure 6a: EPC2107-Q1&Q2: Gate Charge

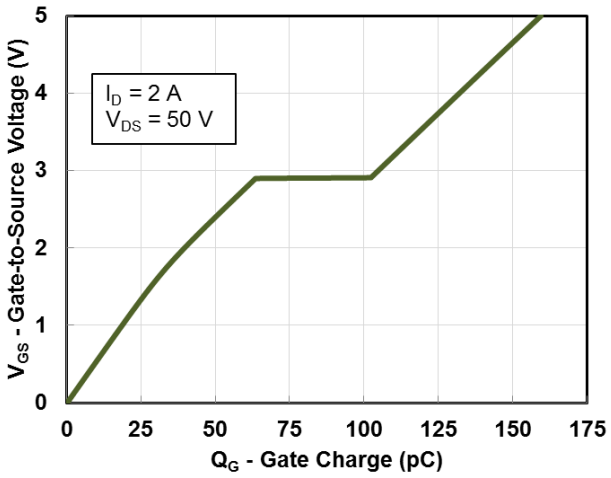


Figure 6b: EPC2107-Q3: Gate Charge

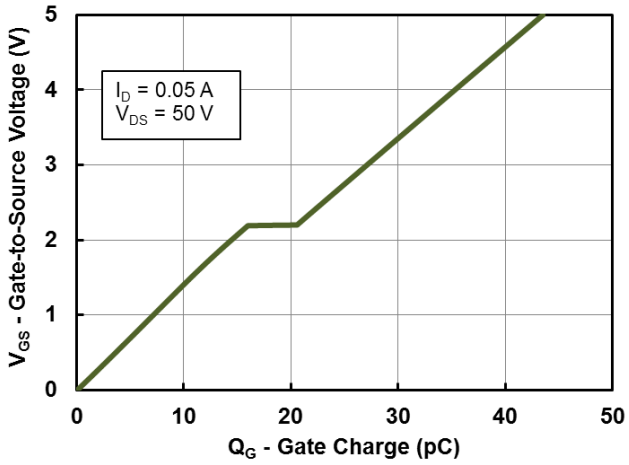


Figure 7a: EPC2107-Q1&Q2: Reverse Drain-Source Characteristics

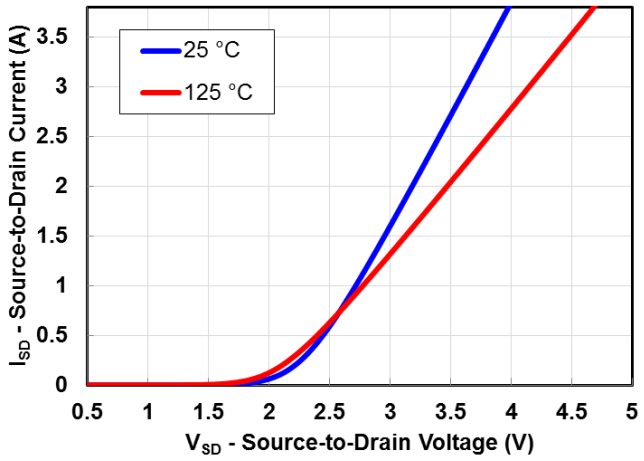


Figure 7b: EPC2107-Q3: Reverse Drain-Source Characteristics

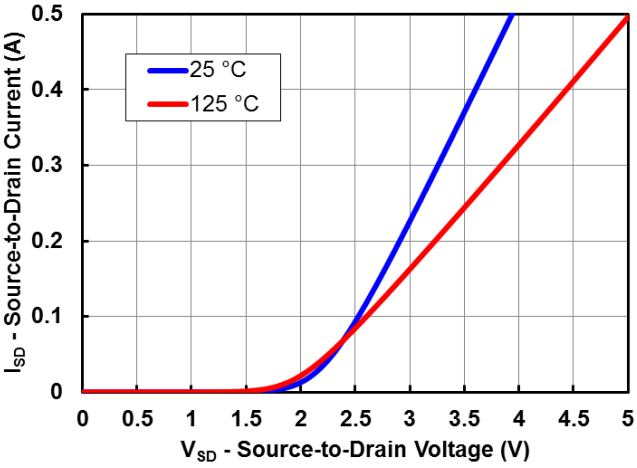


Figure 8a: EPC2107-Q1&Q2: Normalized On Resistance vs. Temperature

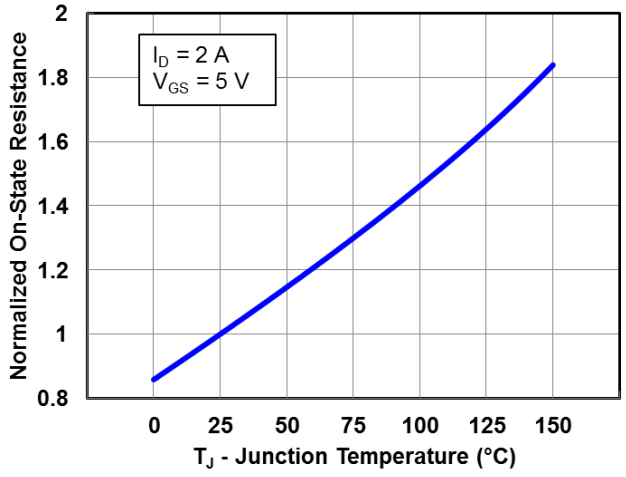


Figure 8b: EPC2107-Q3: Normalized On Resistance vs. Temperature

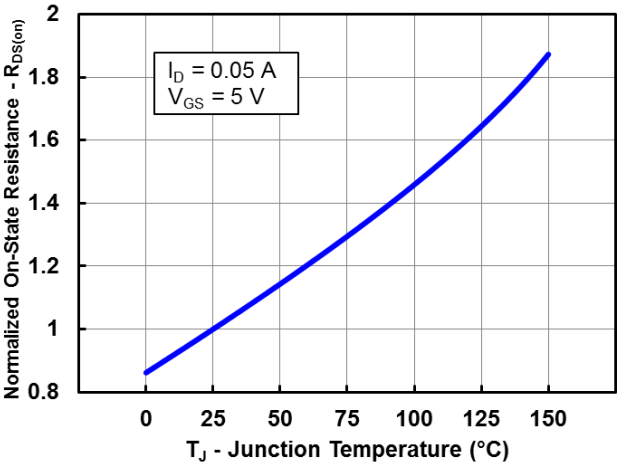


Figure 9a:
EPC2107-Q1&Q2: Normalized Threshold Voltage vs. Temperature

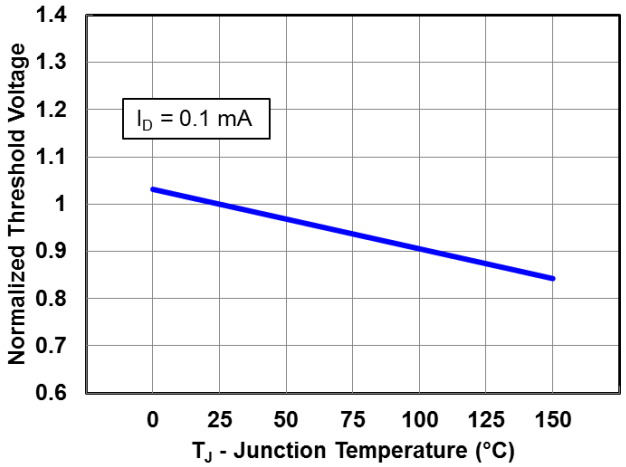
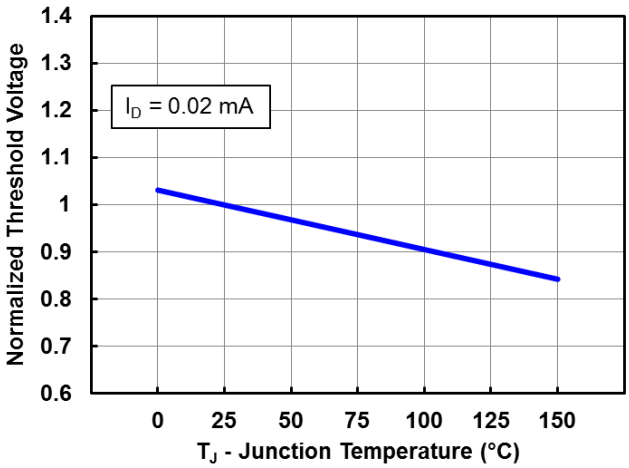
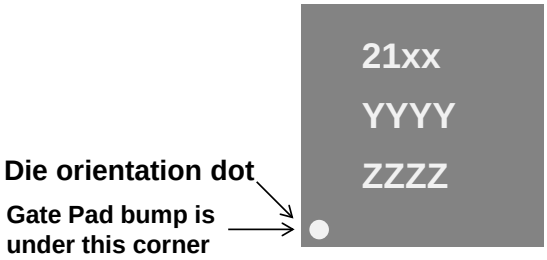


Figure 9b:
EPC2107-Q3: Normalized Threshold Voltage vs. Temperature



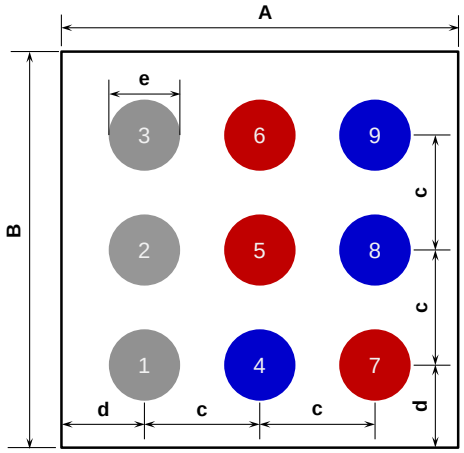
DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2107ENGR	21XX	YYYY	ZZZZ

DIE OUTLINE

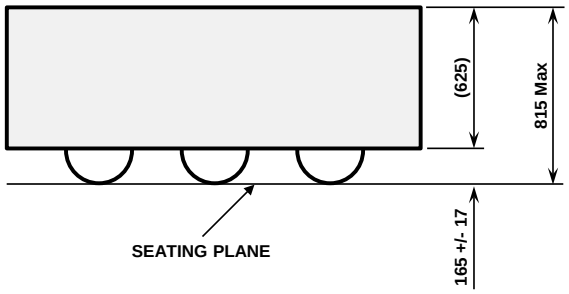
Solder Bar View



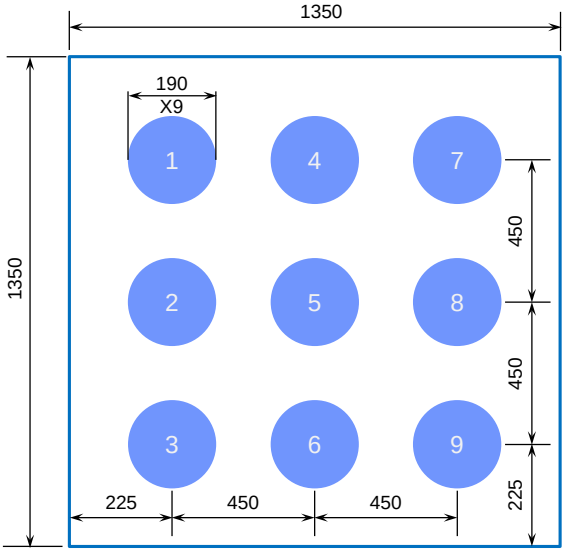
Pad 1 is Gate1 (Q1)
Pad 2 is Gate2 (Q2)
Pad 3 is Gate 3 (Q3)
Pad 7 is Drain1 (Q1)
Pad 5 is Drain2 (Q2)
Pad 6 is Drain3 (Q3)
Pad 4 is Source1 (Q1)
Pad 8 is Source2 (Q2)
Pad 9 is Source3 (Q3)

DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1320	1350	1380
B	1320	1350	1380
c	450	450	450
d	210	225	240
e	187	208	229

Side View



RECOMMENDED LAND PATTERN
(Units in µm)



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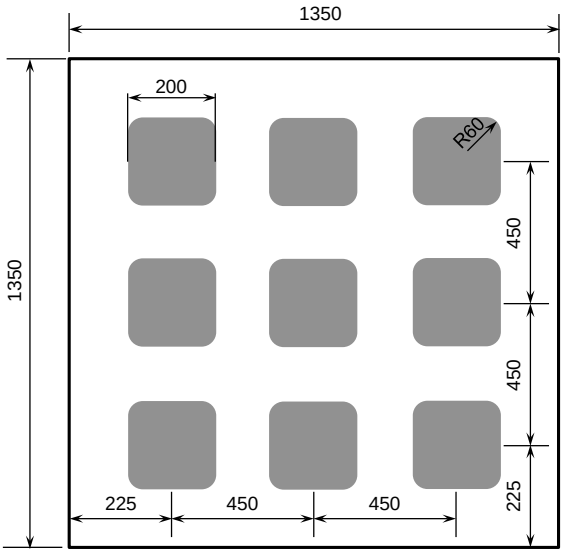
Pad 7 is Drain1 (Q1)
Pad 5 is Drain2 (Q2)
Pad 6 is Drain3 (Q3)
Pad 4 is Source1 (Q1)
Pad 8 is Source2 (Q2)
Pad 9 is Source3 (Q3)

RECOMMENDED STENCIL DESIGN
(Units in µm)



Recommended stencil should be 4mil (100µm) thick, must be laser cut, openings per drawing.
Intended for use with SAC305 Type 4 solder, reference 88.5% metals content
Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012 Revised December, 2015