

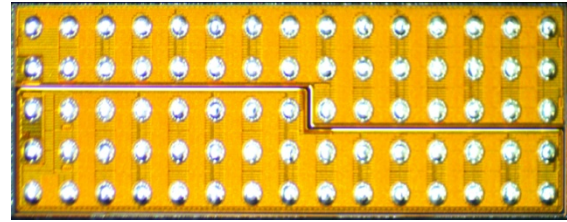
EPC2102 – Enhancement-Mode GaN Power Transistor Half Bridge Preliminary Specification Sheet



Status: Engineering

Features:

- 98% System Efficiency at 18 A
 - 42 V_{IN} to 14 V_{OUT}, 500 kHz
 - Includes driver, inductor, and output filter
- High Frequency Operation
- High Density Footprint
- Low Inductance Package



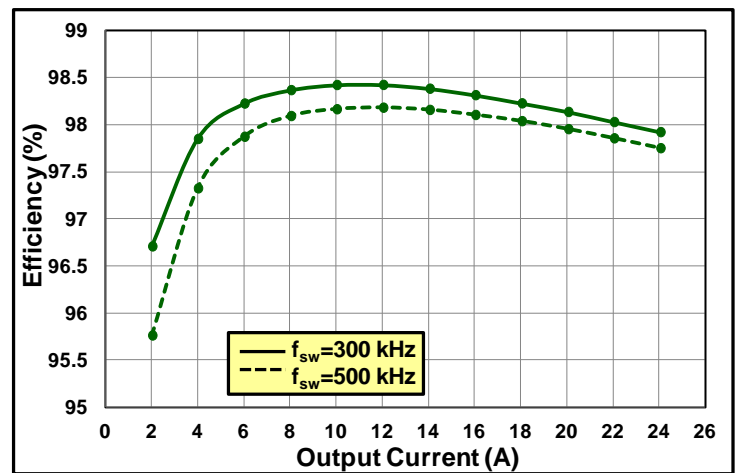
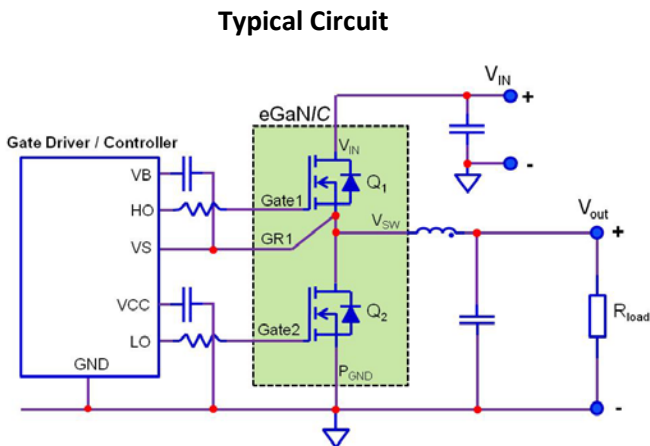
EPC2102 devices are supplied only in passivated die form with solder balls
Die Size: 6.05 mm x 2.3 mm

Pb-Free (RoHS Compliant), Halogen Free

Applications:

- High Frequency DC-DC Conversion

Typical System Efficiency



V_{IN} = 42 V, V_{OUT} = 14 V

MAXIMUM RATINGS

Parameter	Value	
Maximum Drain – Source Voltage (V _{SW} to P _{GND} , V _{IN} to V _{SW})	60 V	
Maximum Gate – Source Voltage Range (Gate 1 to V _{SW} , Gate 2 to P _{GND})	-4 V < V _{GS} < 6 V	
Continuous Drain Current, 25 °C, R _{θJA} = 28 (Q1), 28 (Q2)	Q1 Control FET	23 A
	Q2 Sync FET	23 A
Maximum Pulsed Drain Current, 25 °C, T _{pulse} = 300 μs	Q1 Control FET	215 A
	Q2 Sync FET	215 A
Optimum Temperature Range	-40 °C < T _J < 150 °C	

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STATIC CHARACTERISTICS

Parameter	Conditions	Q1 Control FET	Q2 Sync FET
Maximum Drain – Source Voltage (BV_{DSS})	Q1: $V_{GS} = 0\text{ V}$, $I_D = 430\ \mu\text{A}$	60 V	
	Q2: $V_{GS} = 0\text{ V}$, $I_D = 430\ \mu\text{A}$		
Maximum Drain – Source Leakage	$V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$	360 μA	360 μA
Maximum $R_{DS(on)}$	$V_{GS} = 5\text{ V}$, $I_D = 20\text{ A}$	4.4 m Ω	4.4 m Ω
Typical $R_{DS(on)}$	$V_{GS} = 5\text{ V}$, $I_D = 20\text{ A}$	3.2 m Ω	3.2 m Ω
Gate – Source Threshold Voltage	Q1: $I_D = 7\text{ mA}$, $V_{DS} = V_{GS}$	0.8 V < $V_{GS(TH)}$ < 2.5 V	
	Q2: $I_D = 7\text{ mA}$, $V_{DS} = V_{GS}$		
Gate – Source Maximum Positive Leakage	$V_{GS} = 5\text{ V}$	7 mA	7 mA
Gate – Source Maximum Negative Leakage	$V_{GS} = -4\text{ V}$	-360 μA	-360 μA

$T_J = 25\text{ }^\circ\text{C}$ unless otherwise stated

DYNAMIC CHARACTERISTICS

Parameter	Conditions	Typical Value		
		Q1 Control FET	Q2 Sync FET	Unit
C_{ISS} (Input Capacitance)	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$	0.83	0.83	nF
C_{OSS} (Output Capacitance)		0.51	0.71	
C_{RSS} (Reverse Transfer Capacitance)		0.014	0.014	
Q_G (Total Gate Charge)	$V_{DS} = 30\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 5\text{ V}$	6.8	6.8	nC
Q_{GS} (Gate to Source Charge)	$V_{DS} = 30\text{ V}$, $I_D = 20\text{ A}$	2.3	2.3	
Q_{GD} (Gate to Drain Charge)		1.4	1.4	
$Q_{G(TH)}$ (Gate Charge at Threshold)		1.8	1.8	
Q_{OSS} (Output Charge)	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$	23	31	
Q_{RR} (Source-Drain Recovery Charge)		0	0	

$T_J = 25\text{ }^\circ\text{C}$ unless otherwise stated

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THERMAL CHARACTERISTICS

		TYP		
		Q1 Control FET	Q2 Sync FET	
R _{θJC}	Thermal Resistance, Junction to Case	0.4		°C/W
R _{θJB}	Thermal Resistance, Junction to Board (Note 2)	1.8	1.9	°C/W
R _{θ12}	Thermal Resistance, Cross-Coupling	1.3		°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1)	42		°C/W

Note 1: R_{θJA} is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Note 2: ΔT is determined by the following matrix equation:

$$\begin{pmatrix} \Delta T_{Q1} \\ \Delta T_{Q2} \end{pmatrix} = \begin{bmatrix} 1.8 & 1.3 \\ 1.3 & 1.9 \end{bmatrix} \cdot \begin{pmatrix} P_{Q1} \\ P_{Q2} \end{pmatrix}$$

This matrix equation lets you calculate the temperature rise of each FET, given the power dissipated in each FET.

Thermal models for EPC devices available at <http://epc-co.com/epc/DesignSupport/DeviceModels.aspx>

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Figure 1a: EPC2102-Q1 Typical Output Characteristics at 25°C

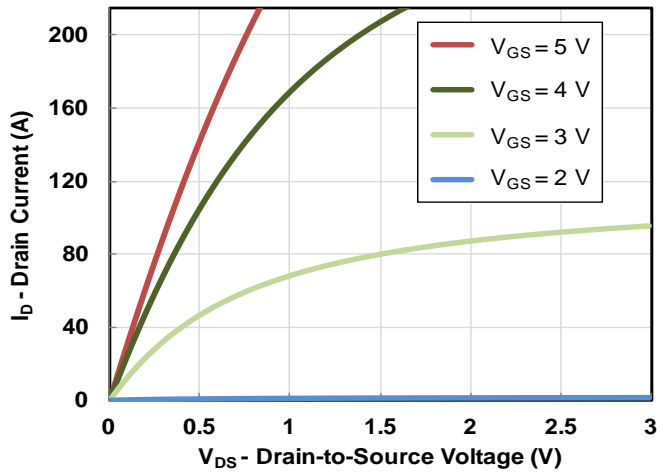


Figure 1b: EPC2102-Q2 Typical Output Characteristics at 25°C

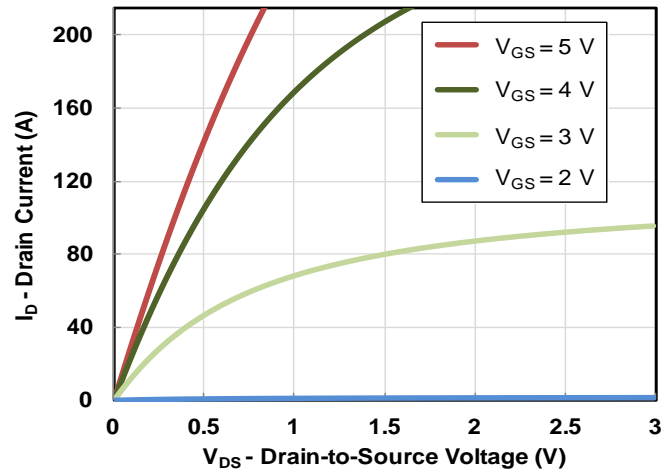


Figure 2a: EPC2102-Q1 Transfer Characteristics

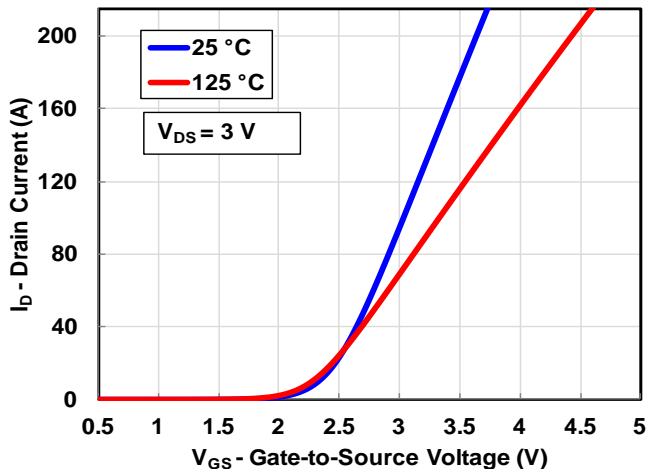


Figure 2b: EPC2102-Q2 Transfer Characteristics

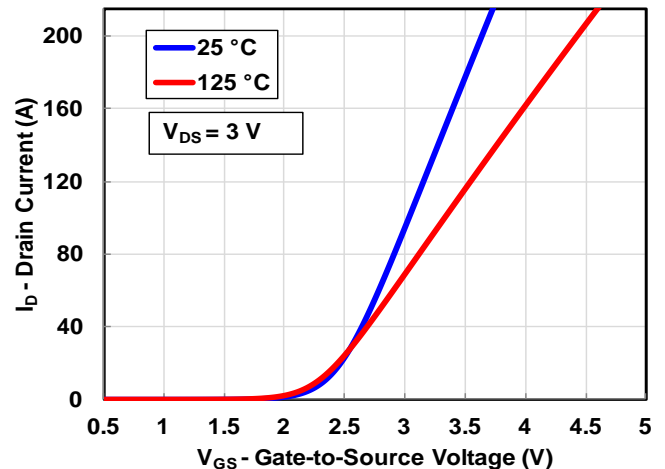


Figure 3a: EPC2102-Q1: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

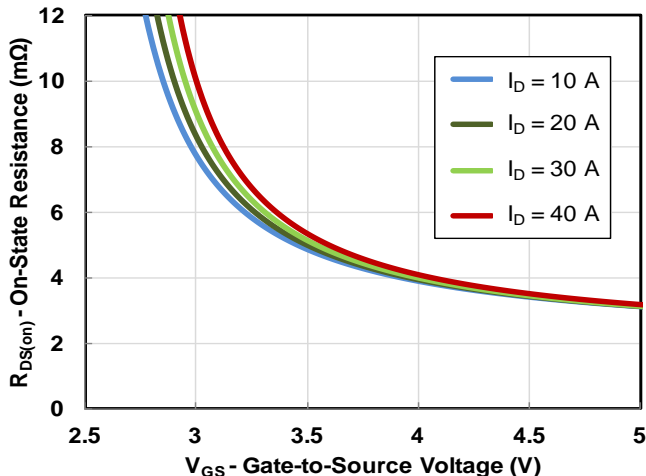
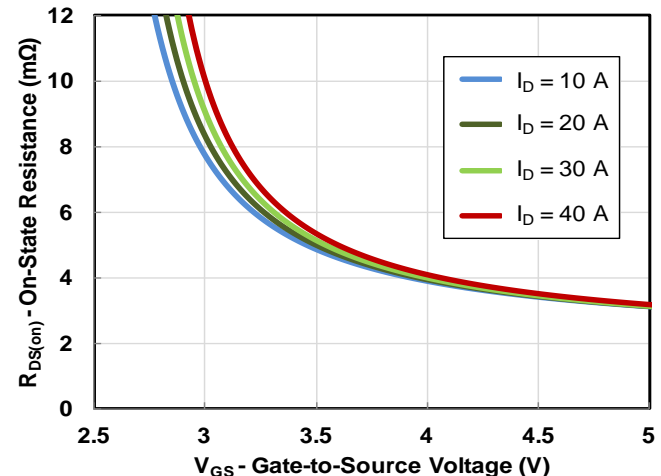


Figure 3b: EPC2102-Q2: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents



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Figure 4a: EPC2102-Q1: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

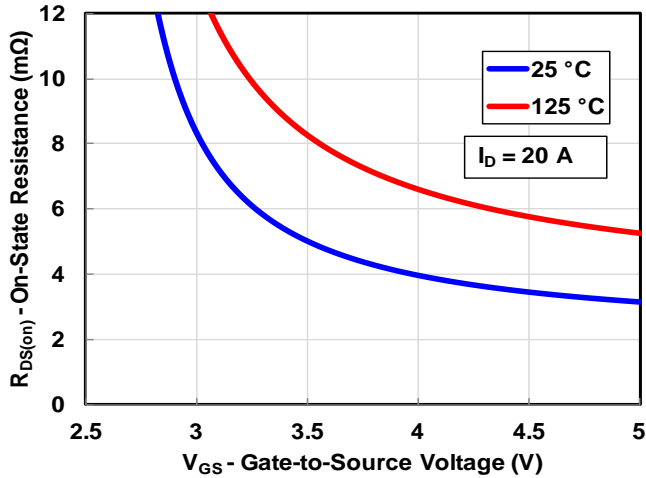


Figure 4b: EPC2102-Q2: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

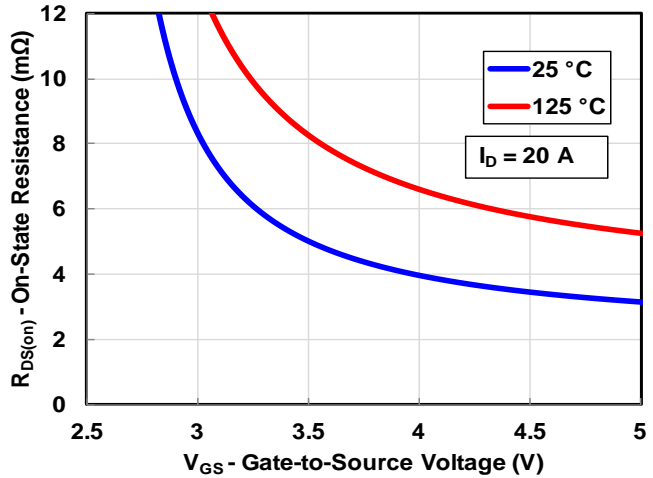


Figure 5a: EPC2102-Q1: Capacitance (Linear Scale)

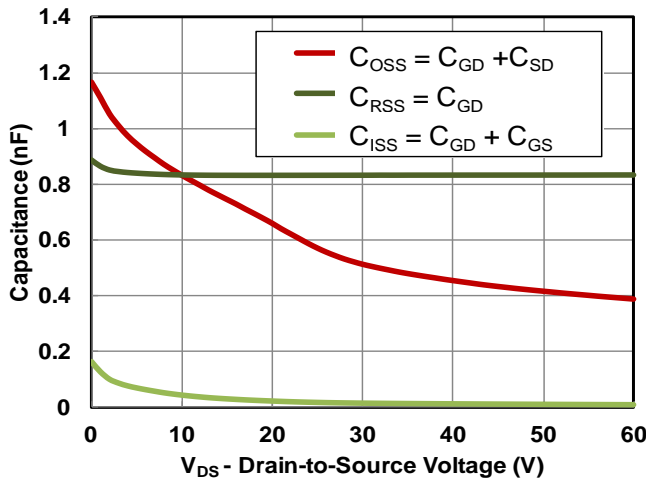


Figure 5b: EPC2102-Q2: Capacitance (Linear Scale)

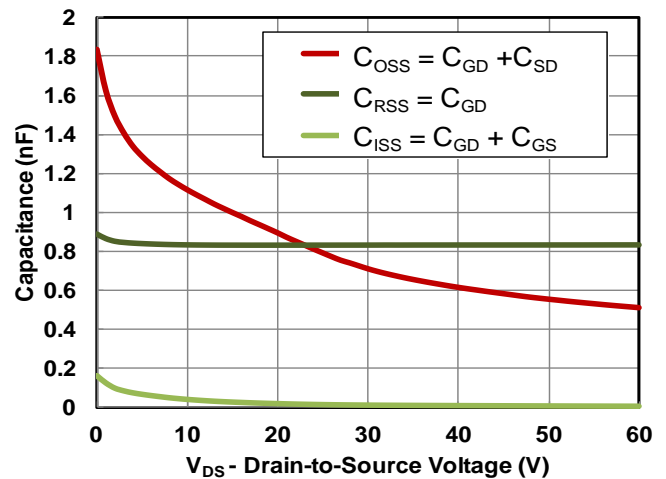


Figure 5c: EPC2102-Q1: Capacitance (Log Scale)

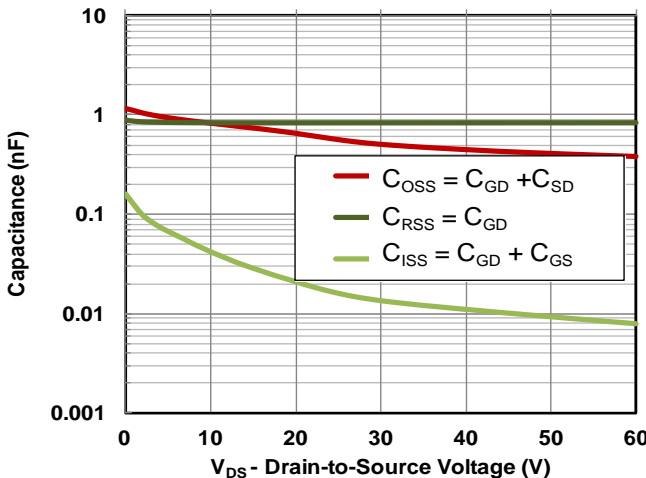
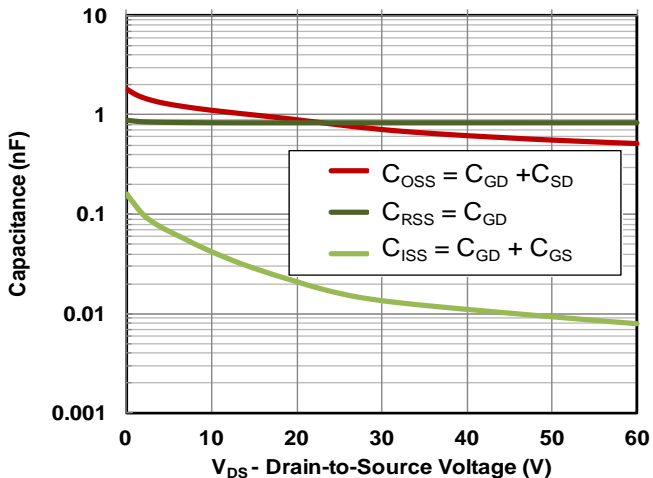


Figure 5d: EPC2102-Q2: Capacitance (Log Scale)



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Figure 6a: EPC2102-Q1: Gate Charge

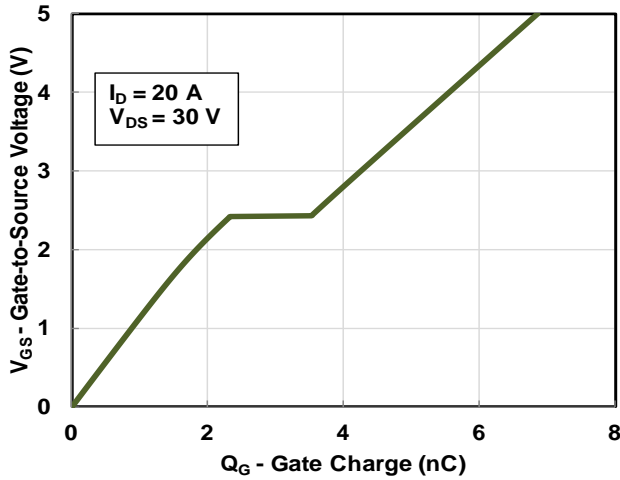


Figure 6b: EPC2102-Q2: Gate Charge

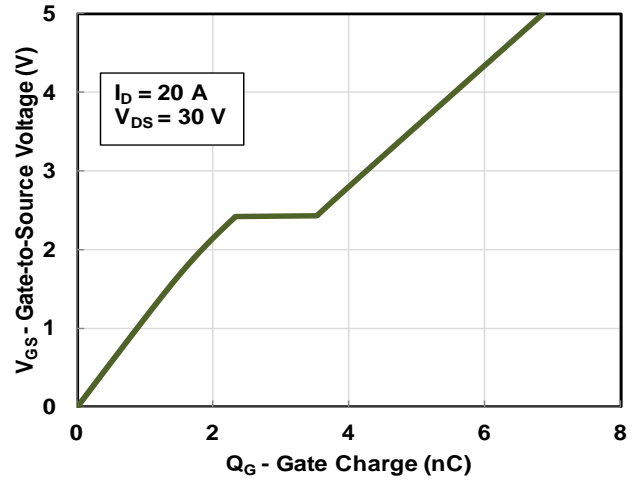


Figure 7a: EPC2102-Q1: Reverse Drain-Source Characteristics

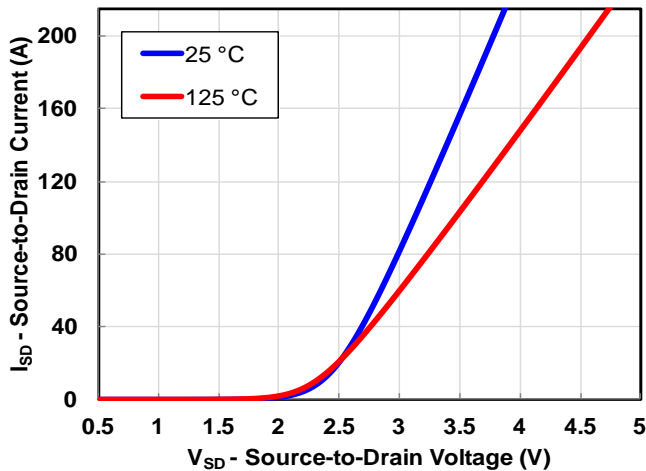


Figure 7b: EPC2102-Q2: Reverse Drain-Source Characteristics

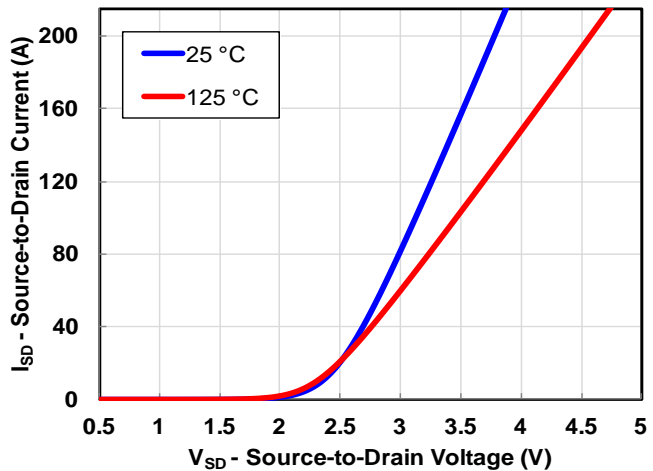


Figure 8a: EPC2102-Q1: Normalized On Resistance vs. Temperature

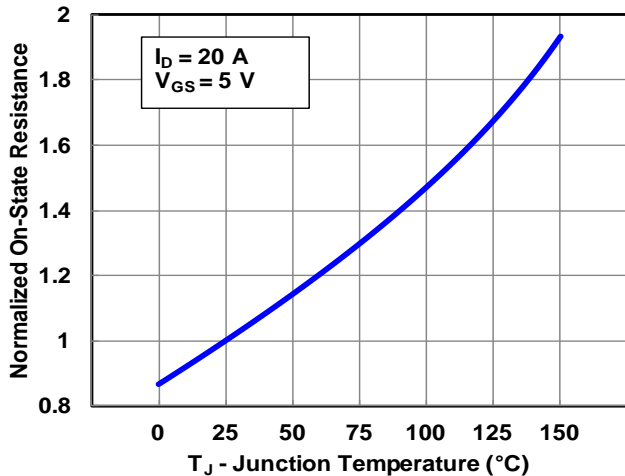
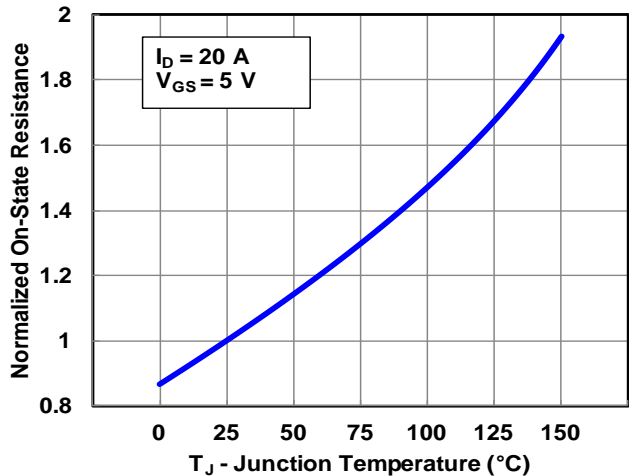


Figure 8b: EPC2102-Q2: Normalized On Resistance vs. Temperature



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Figure 9a:
EPC2102-Q1: Normalized Threshold Voltage vs. Temperature

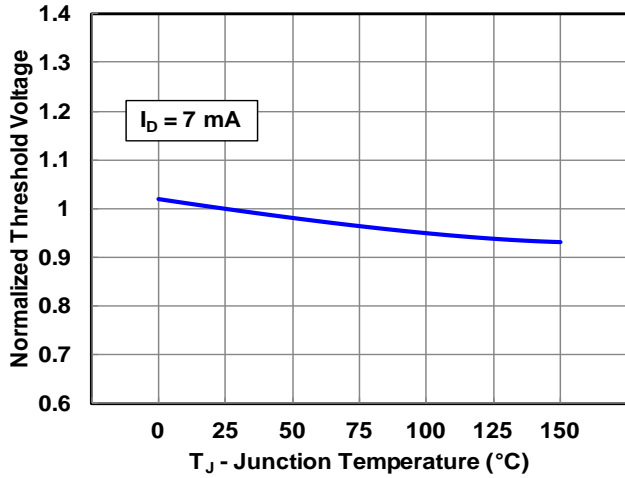
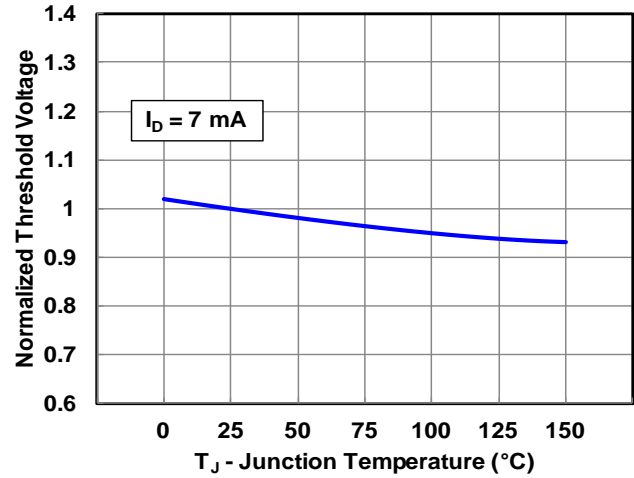


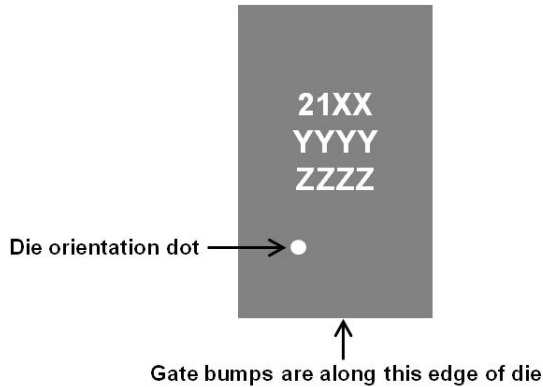
Figure 9b:
EPC2102-Q2: Normalized Threshold Voltage vs. Temperature



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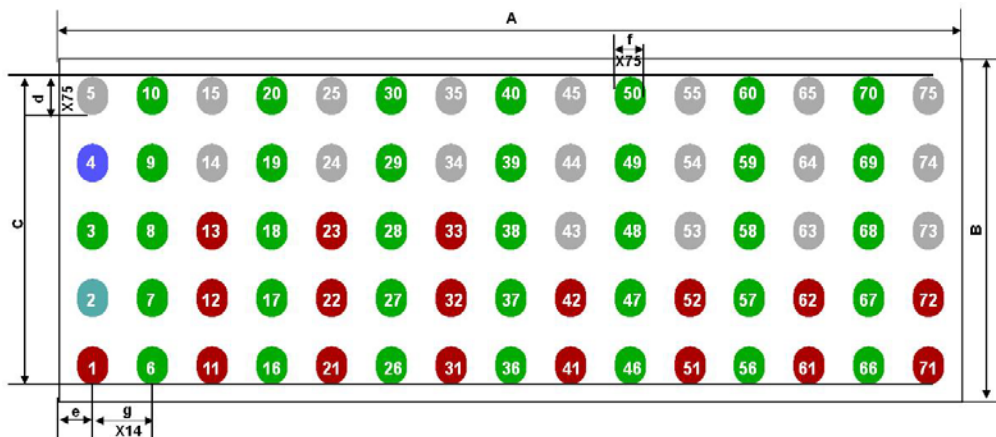
DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2102ENGR	21XX	YYYY	ZZZZ

DIE OUTLINE

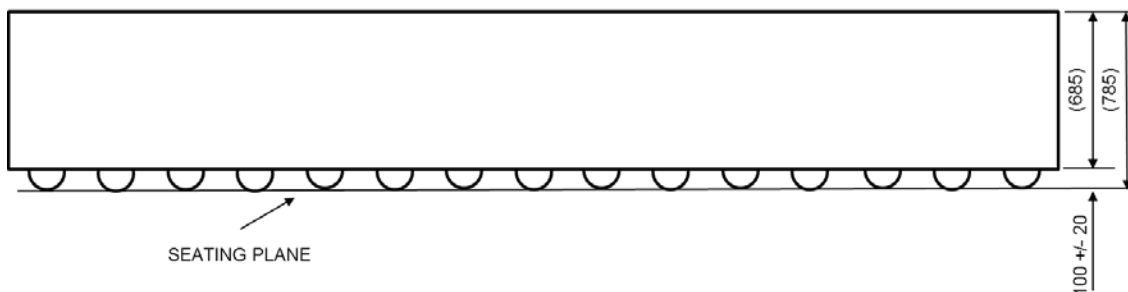
Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c	2047	2050	2053
d	247	250	253
e	210	225	240
f	195	200	205
g	400	400	400

Pads 5, 14, 15, 24, 25, 34, 35, 43, 44, 35, 53, 54, 44, 63, 64, 65, 73, 74, 75 are Ground
 Pads 1, 11, 12, 13, 21, 22, 23, 31, 32, 33, 41, 42, 51, 52, 61, 62, 71, 72 are V_{IN}
 Pads 3, 6, 7, 8, 9, 10, 16, 17, 18, 19, 20, 26, 27, 28, 29, 30, 36, 37, 38, 39, 40, 46, 47, 48, 49, 50, 56, 57, 58, 59, 60, 66, 67, 68, 69, 70 are switch node.

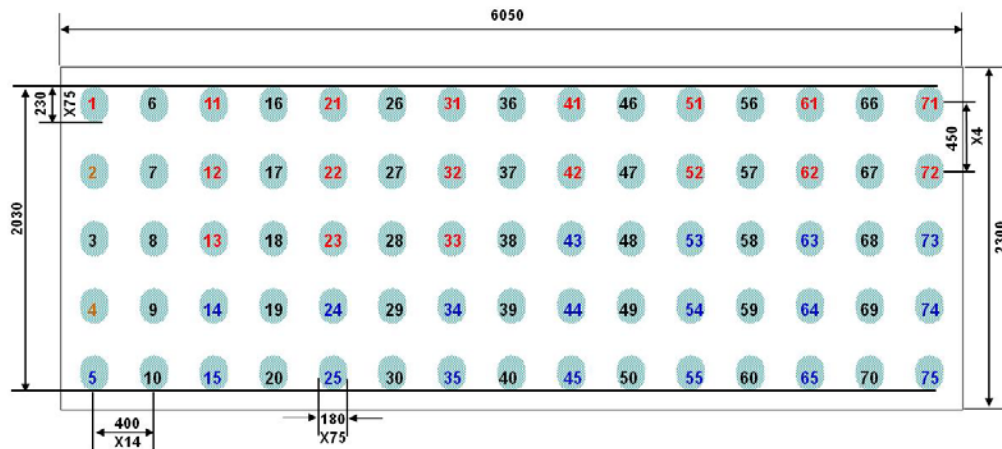
Side View



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RECOMMENDED LAND PATTERN

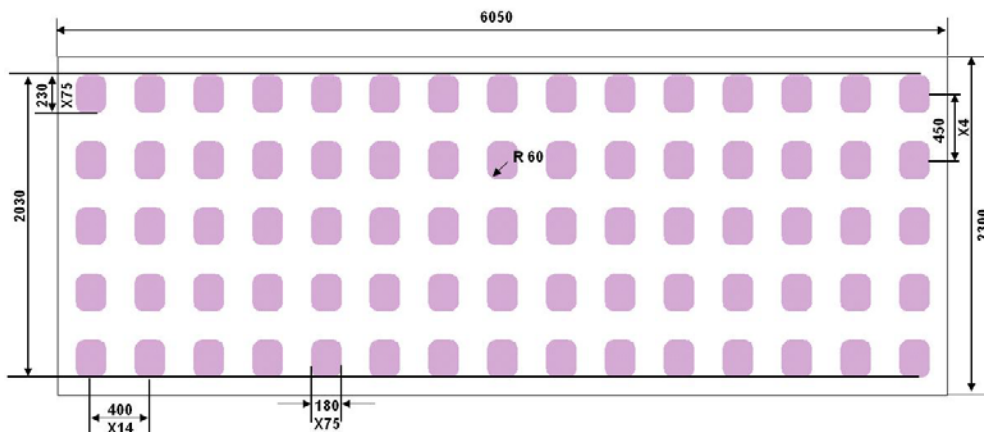
(Units in μm)



Pad 2 is Gate1 (high side); Pad 4 is Gate2 (low side); Pad 3 is HS Gate Return;
 Pads 5, 14, 15, 24, 25, 34, 35, 43, 44, 35, 53, 54, 44, 63, 64, 65, 73, 74, 75 are Ground
 Pads 1, 11, 12, 13, 21, 22, 23, 31, 32, 33, 41, 42, 51, 52, 61, 62, 71, 72 are V_{IN}
 Pads 3, 6, 7, 8, 9, 10, 16, 17, 18, 19, 20, 26, 27, 28, 29, 30, 36, 37, 38, 39, 40, 46, 47, 48, 49, 50, 56, 57, 58, 59, 60, 66, 67, 68, 69, 70 are switch node.

RECOMMENDED STENCIL DESIGN

(Units in μm)



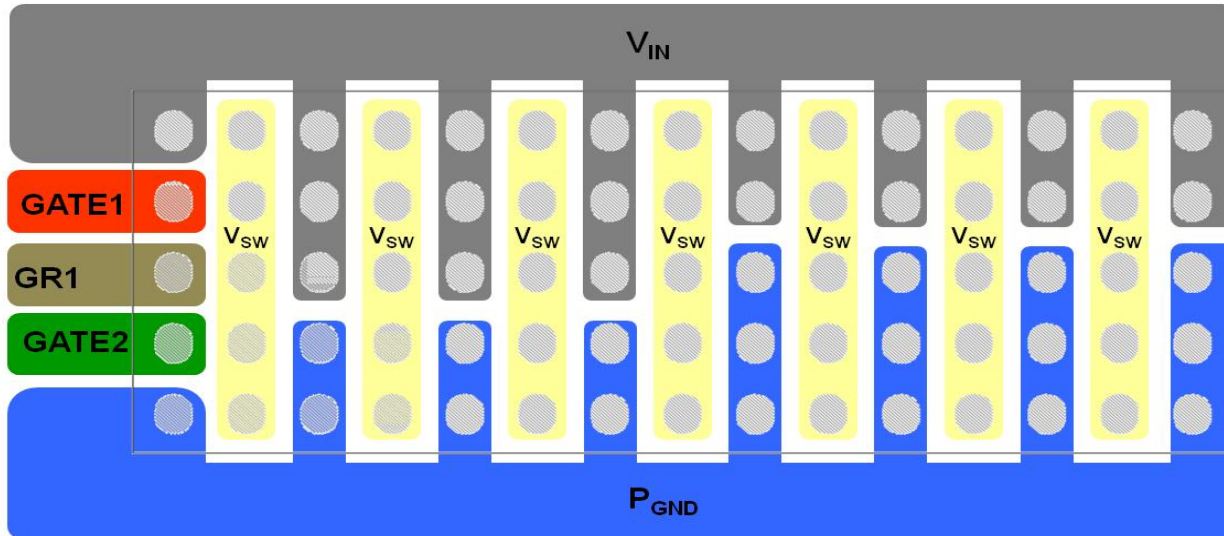
Recommended stencil should be 4mil (100 μm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional assembly resources available at <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

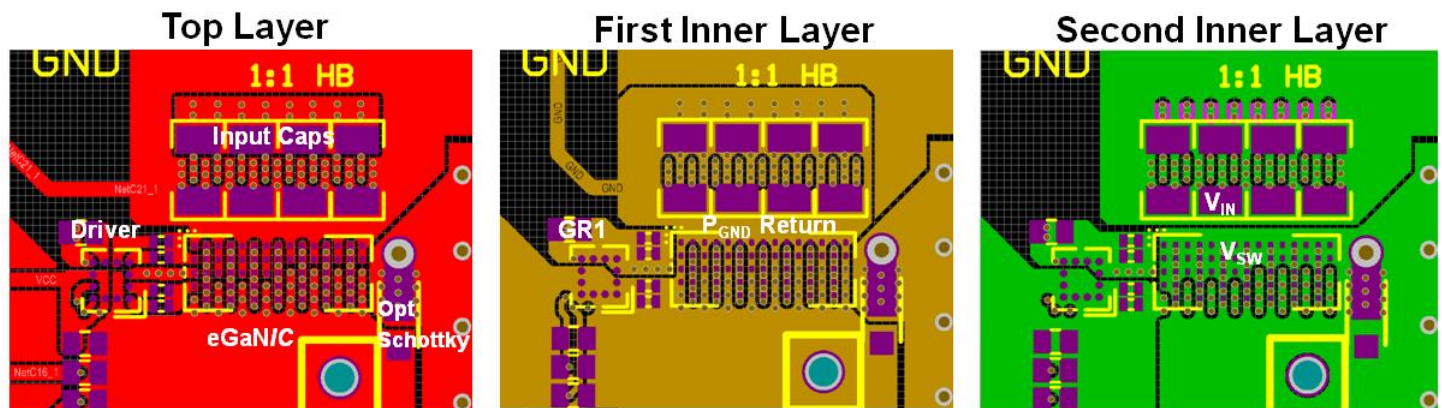
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RECOMMENDED PCB LAYOUT



Land pattern is solder mask defined.

PCB LAYOUT EXAMPLE



Recommended PCB Layout

Gerber Files available at:

<http://epc-co.com/epc/documents/gerber-files/EPC9038%20Development%20Board%20Gerbers.zip>

Assembly Resources at: <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

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