A Low Power, 10 mΩ, 2 A, 0.82 mm^2 WLCSP Integrated Power Switch with Multiple Protection Features

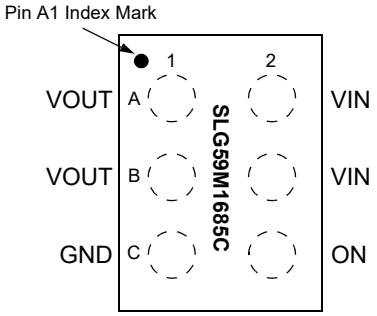
General Description

The SLG59M1685C is a self-powered, high-performance, 2 A capable, single-channel integrated power switch designed for high-side power control applications up to 2 A. This feature-rich nFET IPS has been performance-optimized for all small form-factor, battery-powered applications including smartphones, tablet/notebook PCs, and GPS devices.

Operating from 1.3 V to 3.6 V supplies, the SLG59M1685C's RDS_{ON} is 10 mΩ and its protection-feature set includes V_{IN} undervoltage lockout, two-level current-limit, thermal shutdown, and fast V_{OUT} discharge. With a fixed V_{OUT} slew rate of 2.7 V/ms (adjustable via metal mask from 0.3 V/ms to 10 V/ms), inrush currents at V_{IN} are predictable and the IPS is designed to drive C_{LOAD}s up to 500 µF.

Using Dialog's proprietary MOSFET IP, the SLG59M1685C achieves a stable RDS_{ON} across a wide input voltage range. Fully specified over the -40 °C to 85 °C temperature range, this advanced nFET IPS is available in a 6-ball WLCSP measuring 0.71 mm x 1.16 mm x 0.5 mm with 0.35mm pitch.

Pin Configuration



6L WLCSP
(Laser Marking View)

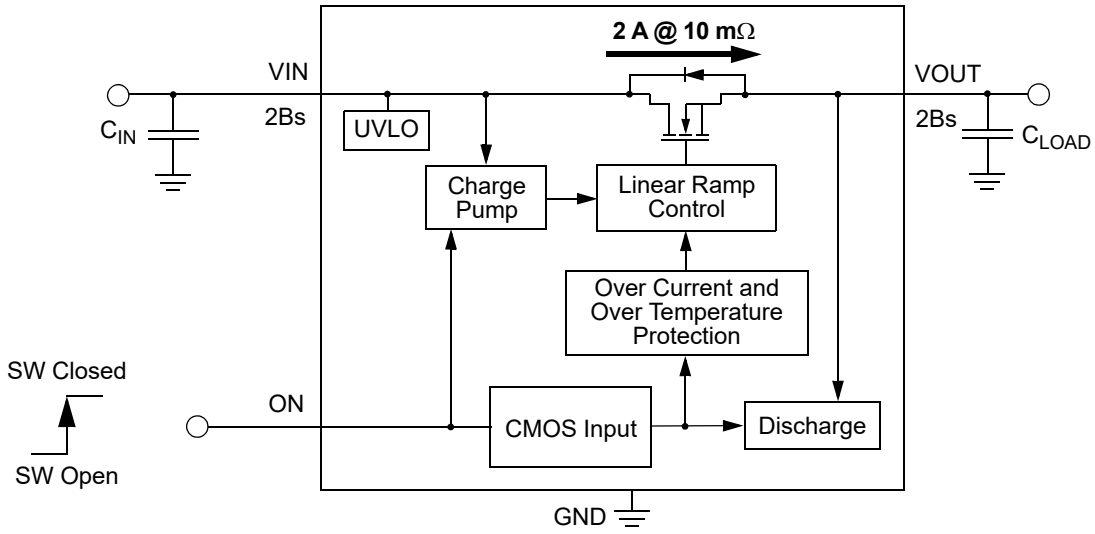
Features

- High-performance nFET Design:
  - Low Typical RDS_{ON}: 10 mΩ
- Steady-state Operating Current: 2 A
- Operating V_{IN} Range: 1.3 V ≤ V_{IN} ≤ 3.6 V
- Fixed V_{OUT} Slew Rate: 2.7 V/ms at V_{IN} = 3.6 V
- Two-stage Overcurent Protection
  - Fixed 2.7 A Active Current Limit
  - Fixed 0.7 A Short-circuit Current Limit
- Fast V_{OUT} Discharge
- Thermal Shutdown Protection
- ON/OFF Control: Active HIGH
- Pb-Free / Halogen-Free / RoHS compliant WLCSP
  - 6 pin 0.71 mm x 1.16 mm, 0.35 mm pitch

Applications

- Smartphones
- Tablet and Notebook PCs
- GPS Devices
- Portable POS Terminals
- Portable Bar-code Scanners

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
A2, B2	VIN	Power/ MOSFET	With an internal 1.07 V $V_{IN(UVLO)}$ threshold, VIN supplies the power for the operation of the IC's internal control circuitry. This terminal is also the drain terminal connection of the n-channel MOSFET. Connect a 1 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at the VIN terminal should be rated at 10 V or higher.
A1, B1	VOUT	MOSFET	Source terminal connections of the n-channel MOSFET. Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended C_{LOAD} range. Capacitors used at VOUT should be rated at 10 V or higher.
C2	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1685C's state machine. ON is an asserted HIGH, level-sensitive CMOS input with ON_V_{IL} < 0.25 V and ON_V_{IH} > 0.85 V. While there is an internal pull-down circuit to GND (~6 MΩ), connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
C1	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1685C	WLCSP 6L	Industrial, -40 °C to 85 °C
SLG59M1685CTR	WLCSP 6L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN} to GND	Power Switch Input Voltage to GND		-0.3	--	5	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	5	V
ON to GND	ON Pin Voltage to GND		-0.3	--	5	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	TBD	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	TBD	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	0.71 x 1.16 mm 6L WLCSP; Determined using 0.5 in^2, 1 oz .copper pads under each VIN and VOUT terminal and FR4 pcb material.	--	84	--	°C/W
$T_{J,MAX}$	Maximum Junction Temperature		--	150	--	°C
MOSFET IDS_{PK}	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	4	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

1.3 V ≤ V_{IN} ≤ 3.6 V; T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are at T_A = 25°C

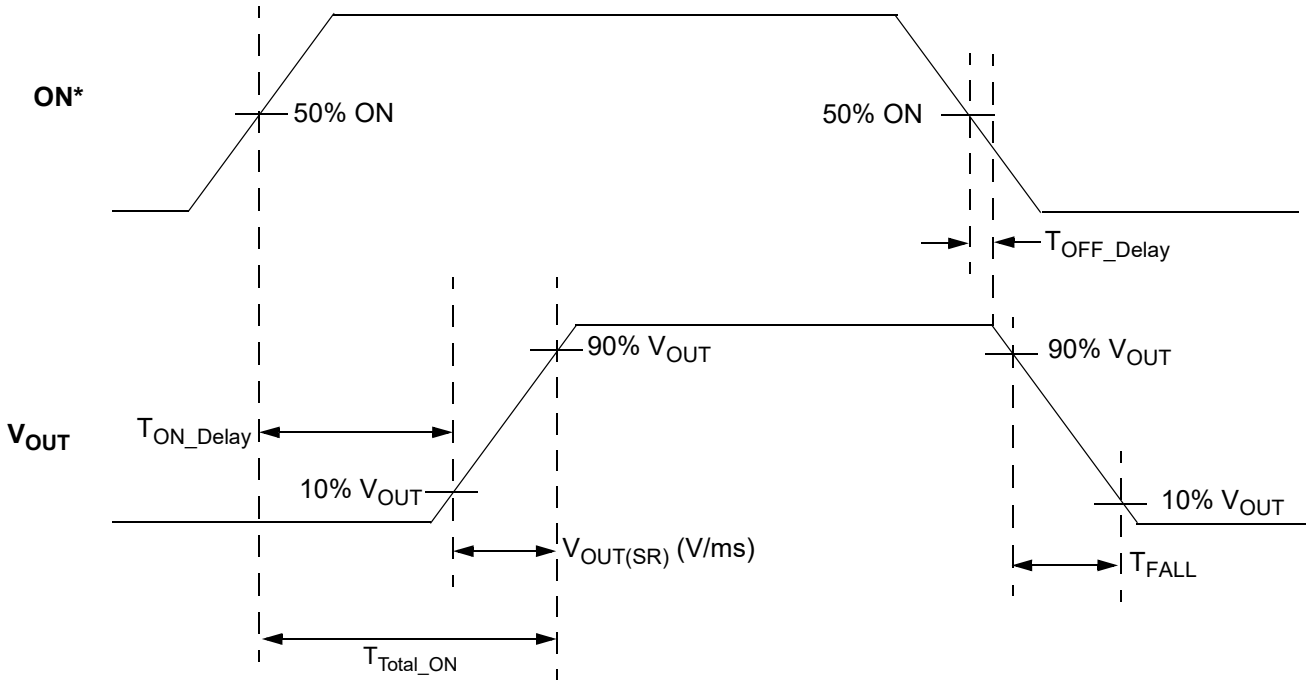
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Supply and MOSFET Input (Drain) Voltage		1.3	--	3.6	V
$V_{IN(UVLO)}$	V_{IN} Rising Undervoltage Lockout Threshold	V_{IN} ↑	0.95	1.07	1.29	V
	V_{IN} Falling Undervoltage Lockout Threshold	V_{IN} ↓	0.90	1.04	1.22	V
I_{IN}	Quiescent Supply Current	V_{IN} = 1.3 V; ON = HIGH; No load	--	66	83	µA
		V_{IN} = 3.6 V; ON = HIGH; No load	--	83	100	µA
$I_{IN(OFF)}$	OFF Mode Supply Current	1.3 ≤ V_{IN} ≤ 3.6 V; ON = LOW; No load	--	0.005	2.2	µA
MOSFET IDS	Current from VIN to VOUT	Continuous	--	--	2	A
RDS_{ON}	ON Resistance	T_A = 25°C; 1.3 ≤ V_{IN} ≤ 3.6 V; I_{DS} = 0.1 A	--	10	13	mΩ
		T_A = 85°C; 1.3 ≤ V_{IN} ≤ 3.6 V; I_{DS} = 0.1 A	--	12	16	mΩ
I_{FET_OFF}	MOSFET OFF Leakage Current	1.3 ≤ V_{IN} ≤ 3.6 V; V_{OUT} = GND; ON = LOW	--	0.005	2.2	µA
I_{LIMIT}	Active Current Limit, I_{ACL}	V_{OUT} > 0.25 V	2.05	2.7	3.5	A
	Short-circuit Current Limit, I_{SCL}	V_{OUT} < 0.25 V	--	0.7	--	A
T_{ACL}	Active Current Limit Response Time	I_{DS} > I_{ACL}	--	10	--	µs

Electrical Characteristics (continued)

1.3 V ≤ V_{IN} ≤ 3.6 V; T_A = -40 °C to 85 °C, unless otherwise noted. Typical values are at T_A = 25°C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{SCL}	Short-Circuit Current Limit Response Time	I_{DS} > I_{SCL}	--	1.5	--	µs
T_{ON_Delay}	ON Delay Time	50% ON to 10% V_{OUT} ↑; V_{IN} = 1.3 V; R_{LOAD} = 10 Ω, C_{LOAD} = 30 µF	0.75	1.05	1.5	ms
		50% ON to 10% V_{OUT} ↑; V_{IN} = 3.6 V; R_{LOAD} = 10 Ω, C_{LOAD} = 30 µF	0.65	1.0	1.4	ms
$V_{OUT(SR)}$	Slew Rate	10% V_{OUT} to 90% V_{OUT} ↑; V_{IN} = 1.3 V; R_{LOAD} = 10 Ω, C_{LOAD} = 30 µF	0.98	1.7	2.65	V/ms
		10% V_{OUT} to 90% V_{OUT} ↑; V_{IN} = 3.6 V; R_{LOAD} = 10 Ω, C_{LOAD} = 30 µF	1.55	2.7	4.2	V/ms
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_{OUT} ↑; V_{IN} = 1.3 V; R_{LOAD} = 10 Ω, C_{LOAD} = 30 µF	1.1	1.6	2.2	ms
		50% ON to 90% V_{OUT} ↑; V_{IN} = 3.6 V; R_{LOAD} = 10 Ω, C_{LOAD} = 30 µF	1.45	2.1	2.7	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_{OUT} Fall Start; V_{IN} = 1.3 V; R_{LOAD} = 10 Ω, no C_{LOAD}	9.5	25	40	µs
		50% ON to V_{OUT} Fall Start; V_{IN} = 3.6 V; R_{LOAD} = 10 Ω, no C_{LOAD}	5.5	9	12	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from VOUT to GND	--	30	500	µF
$R_{DISCHRG}$	Output Discharge Resistance	1.3 ≤ V_{IN} ≤ 3.6 V; V_{OUT} < 0.4 V	--	160	210	Ω
ON_V_{IH}	ON Pin Input High Voltage		0.85	--	V_{IN}	V
ON_V_{IL}	ON Pin Input Low Voltage		-0.3	0	0.25	V
$THERM_{ON}$	Thermal Protection Shutdown Threshold		--	135	--	°C
$THERM_{OFF}$	Thermal Protection Restart Threshold		--	115	--	°C
$THERM_{OFF}$	Thermal Protection Hysteresis		--	20	--	°C

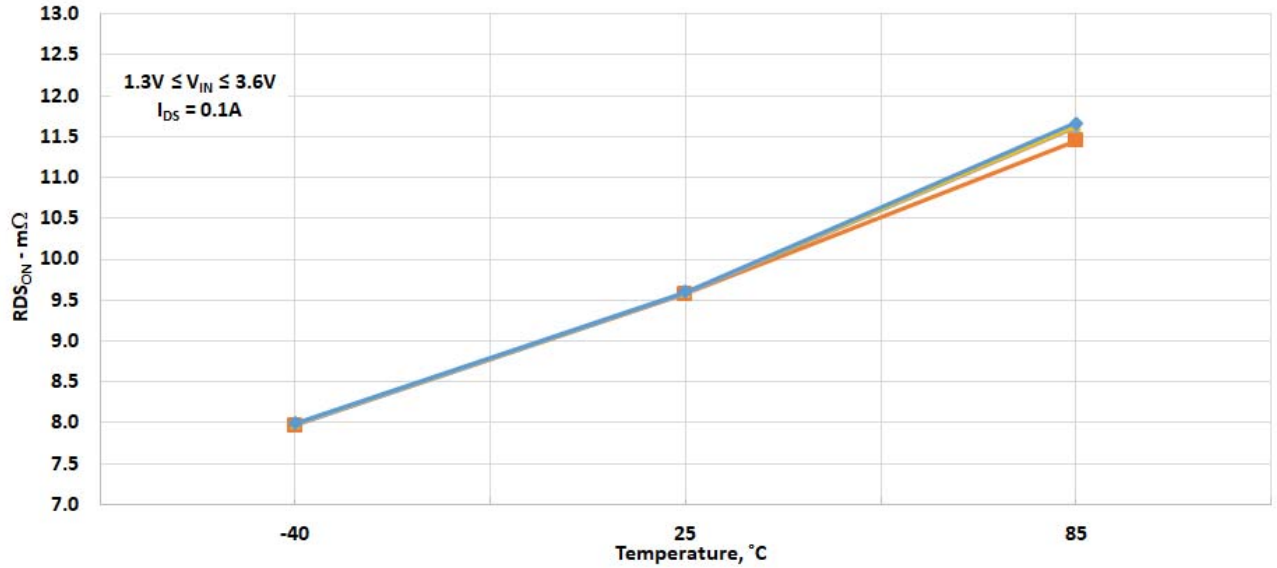
T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



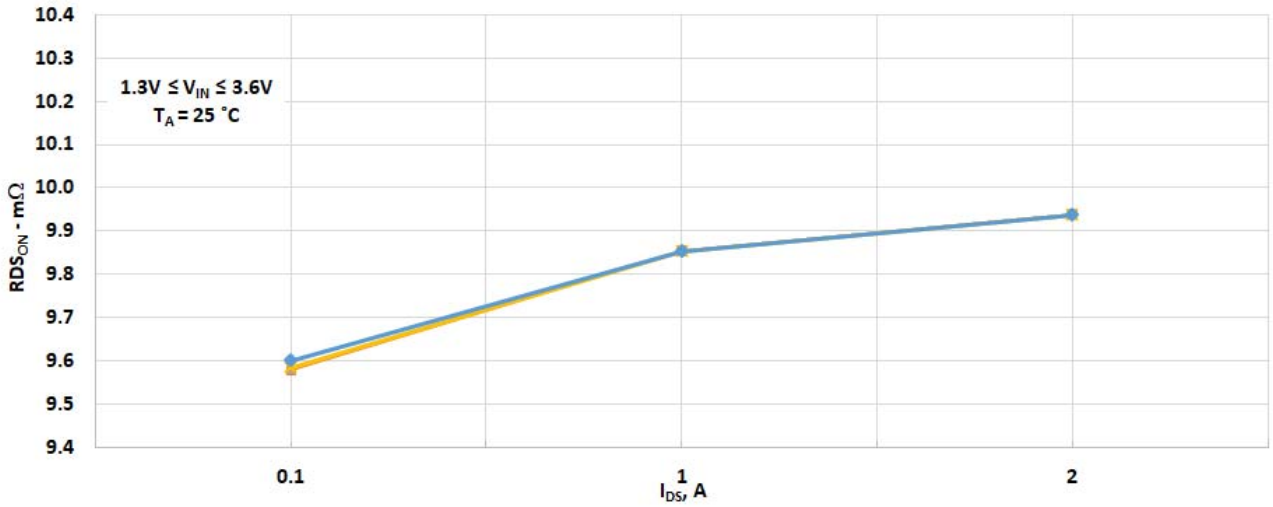
*Rise and Fall Times of the ON Signal are 100 ns

Typical Performance Characteristics

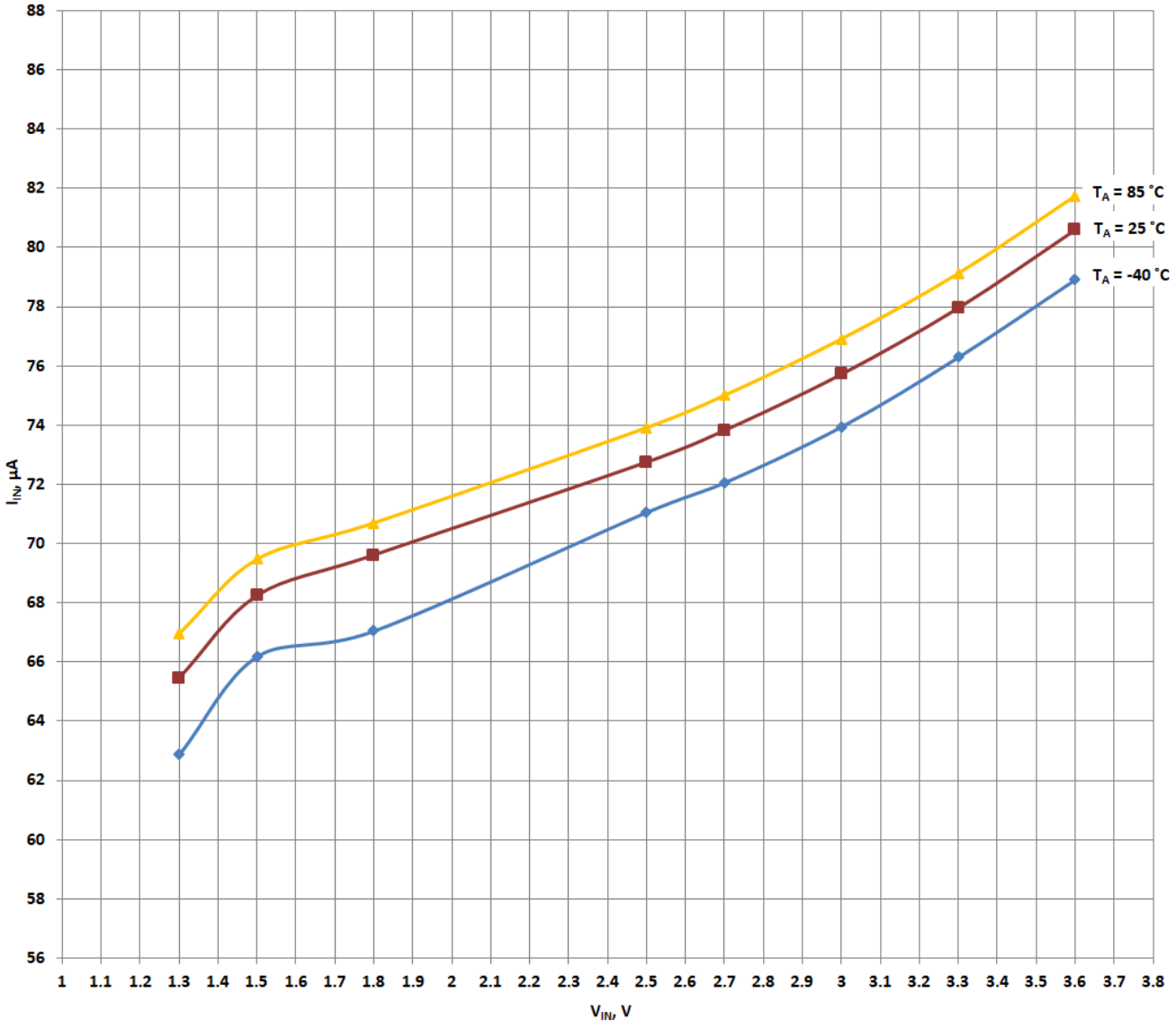
RDS_{ON} vs. Temperature, and V_{IN}



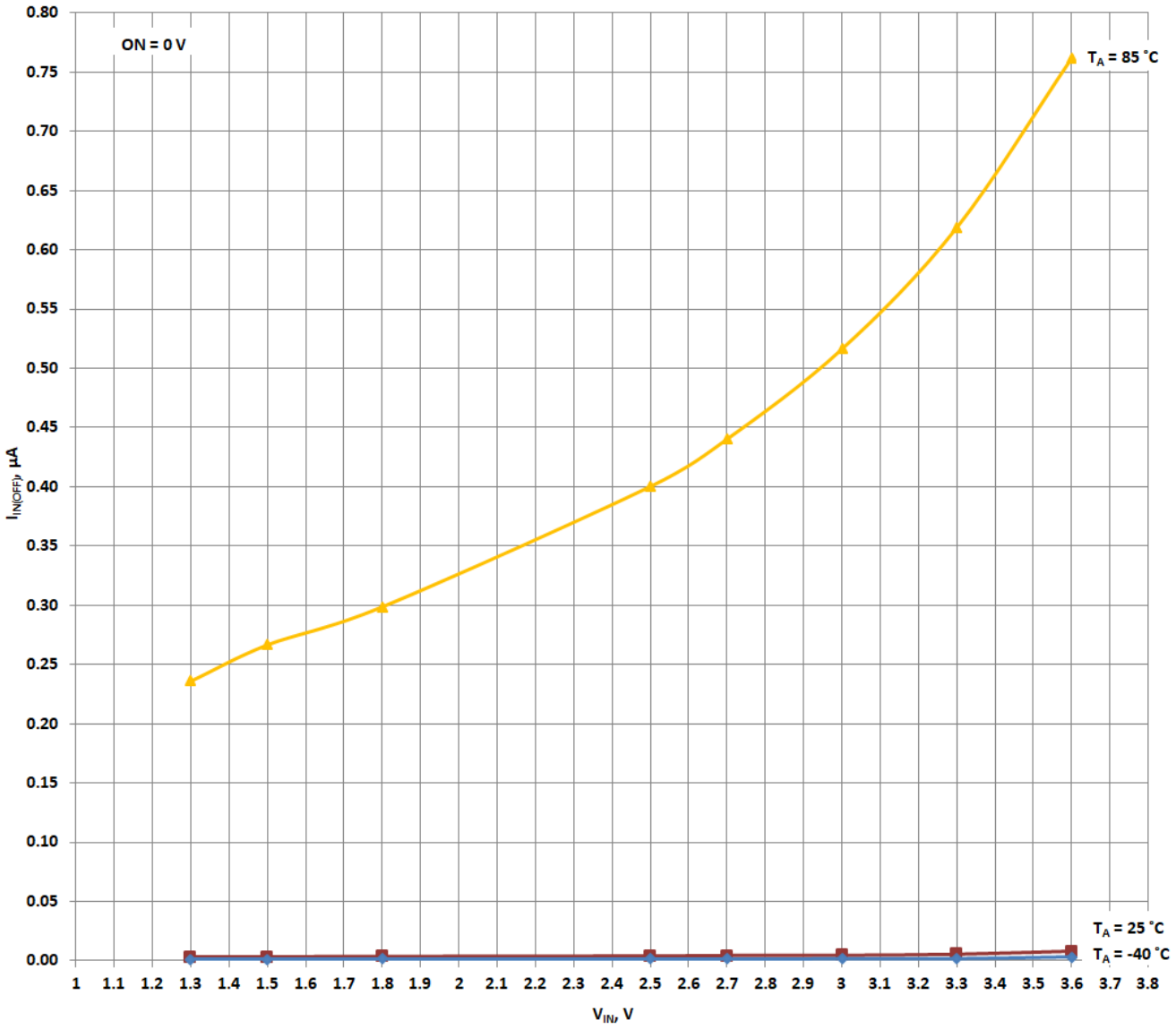
RDS_{ON} vs. I_{DS}, and V_{IN}



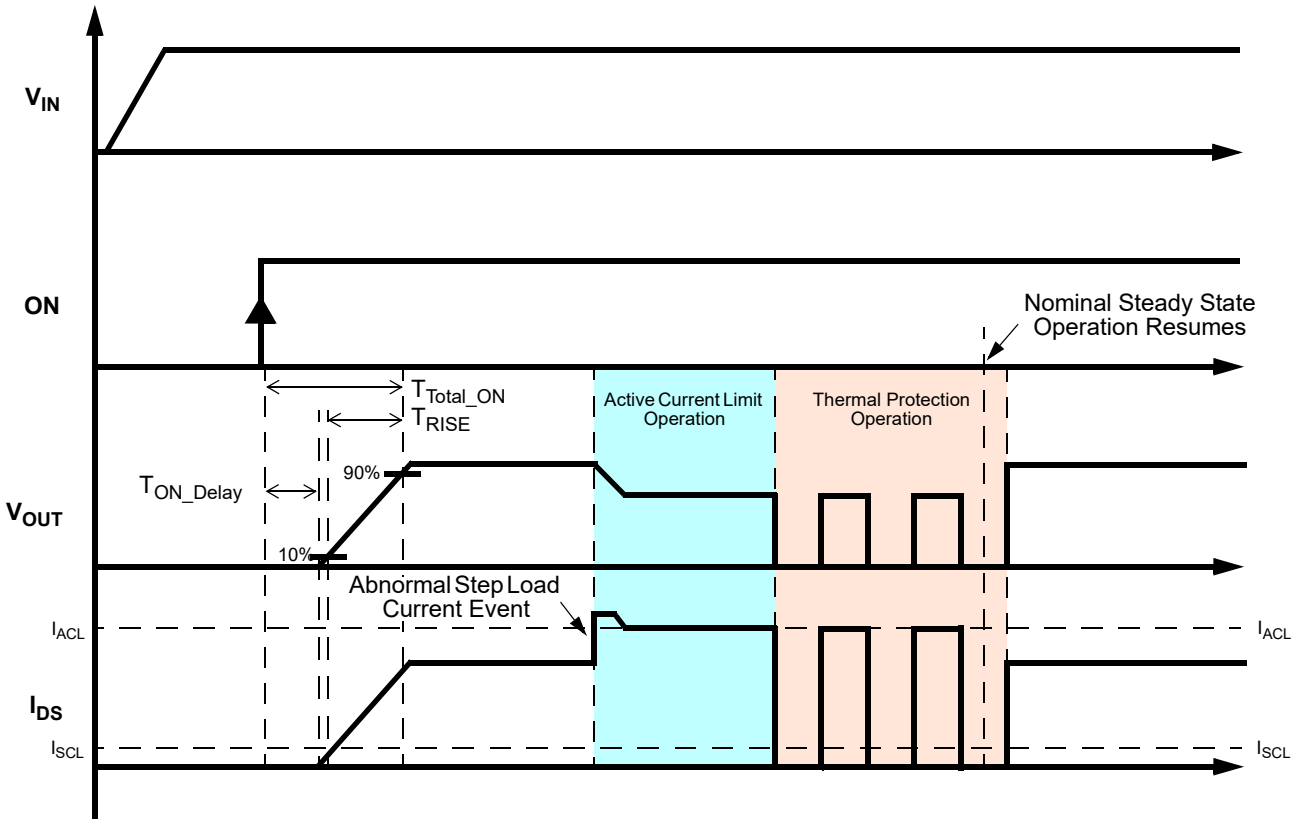
I_{IN} vs. V_{IN} and Temperature



$I_{IN(OFF)}$ vs. V_{IN} and Temperature



Timing Diagram - Active Current Limit & Thermal Protection Operation



Typical Turn-on Waveforms

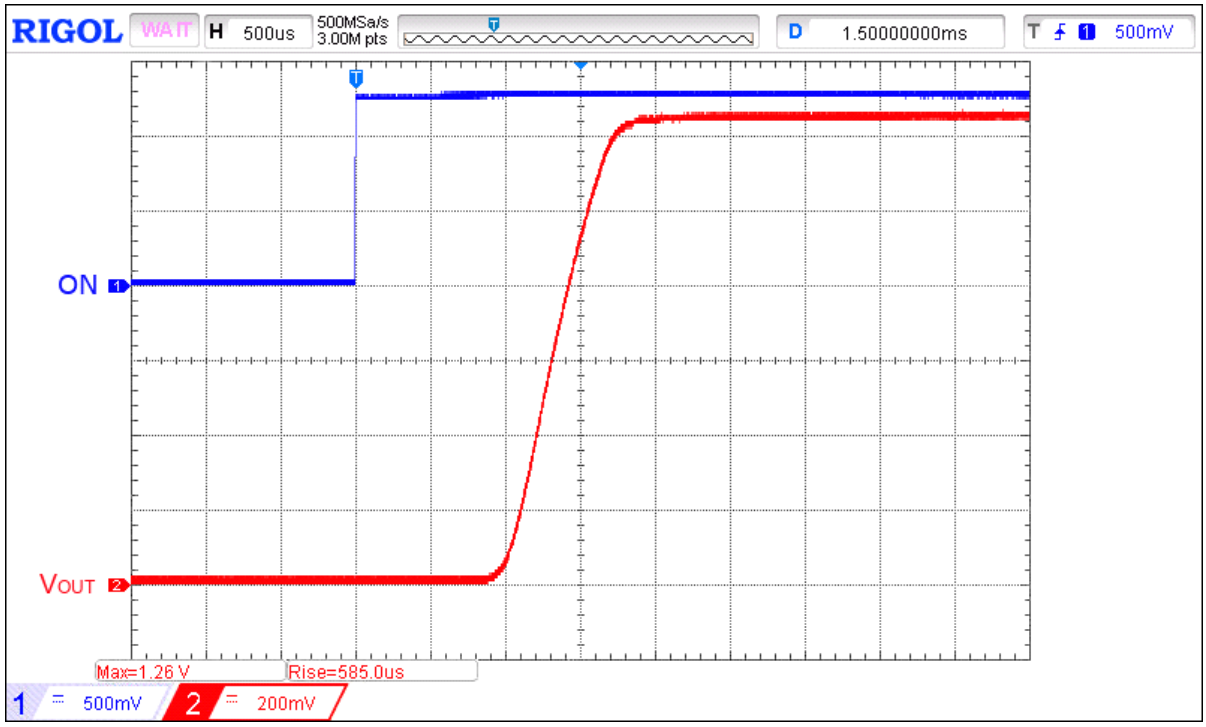


Figure 1. Typical Turn ON operation waveform for V_{IN} = 1.3 V, C_{LOAD} = 30 µF, R_{LOAD} = 10 Ω

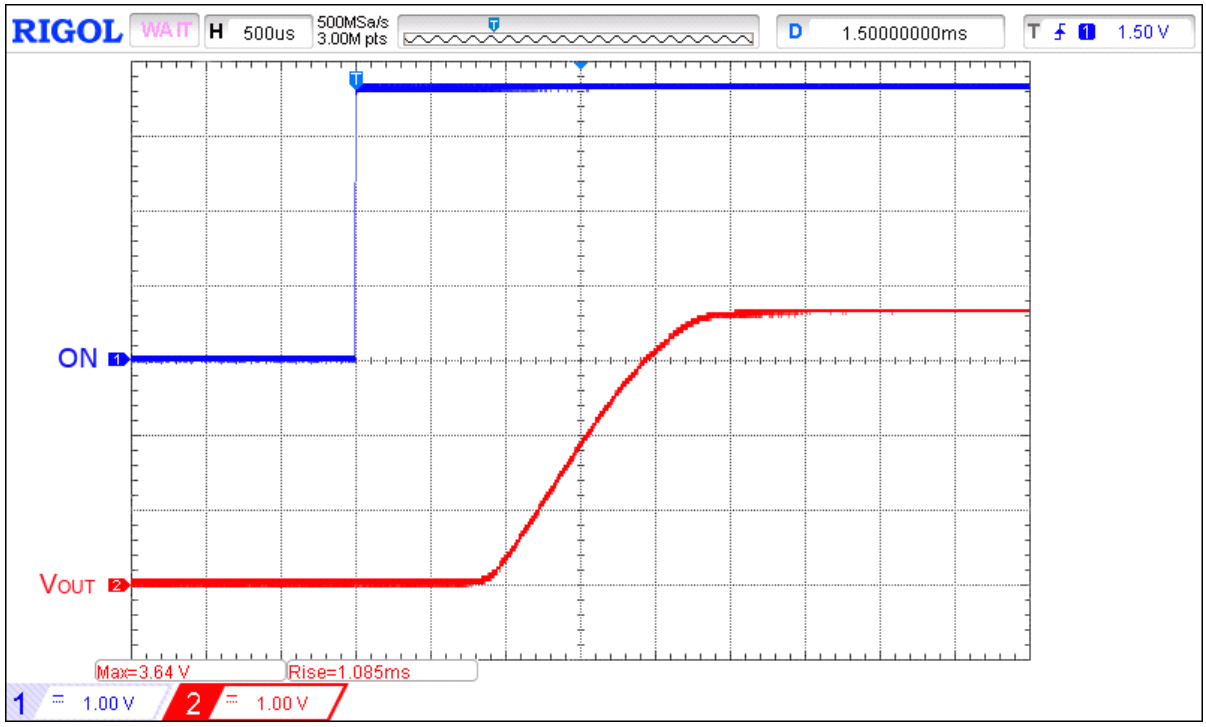


Figure 2. Typical Turn ON operation waveform for V_{IN} = 3.6 V, C_{LOAD} = 30 µF, R_{LOAD} = 10 Ω

Typical Turn-off Waveforms

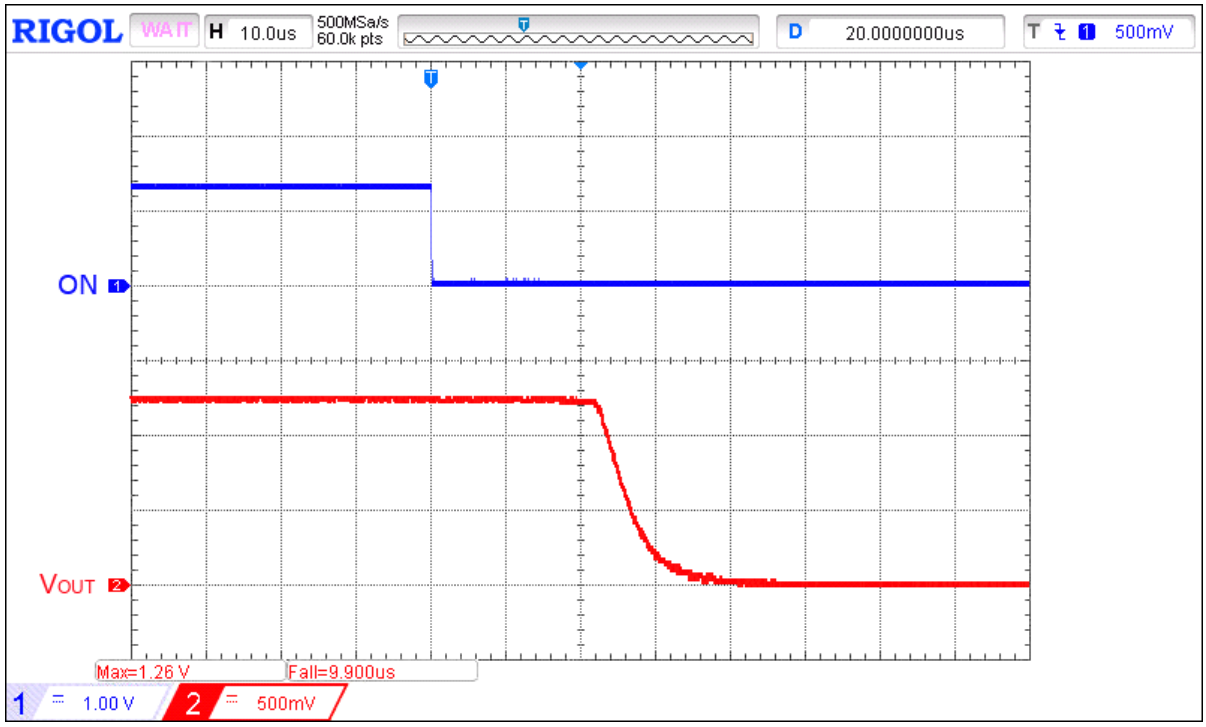


Figure 3. Typical Turn OFF operation waveform for V_{IN} = 1.3 V, R_{LOAD} = 10 Ω, no C_{LOAD}.

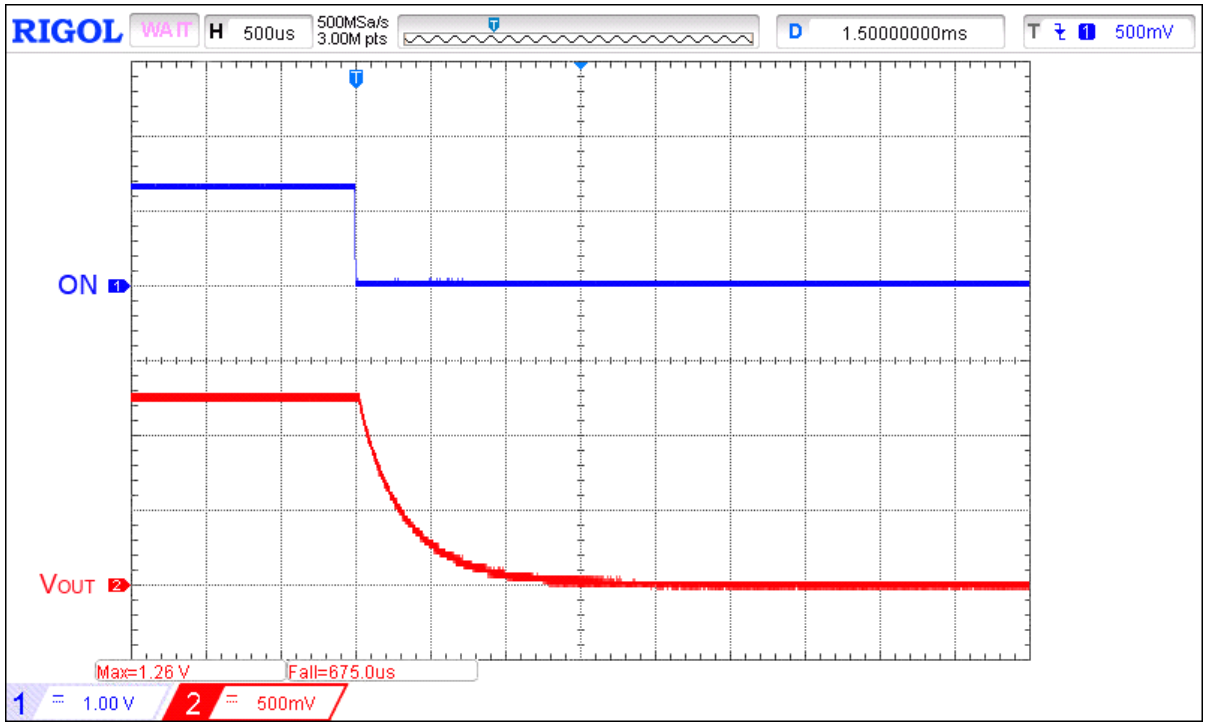


Figure 4. Typical Turn OFF operation waveform for V_{IN} = 1.3 V, C_{LOAD} = 30 µF, R_{LOAD} = 10 Ω

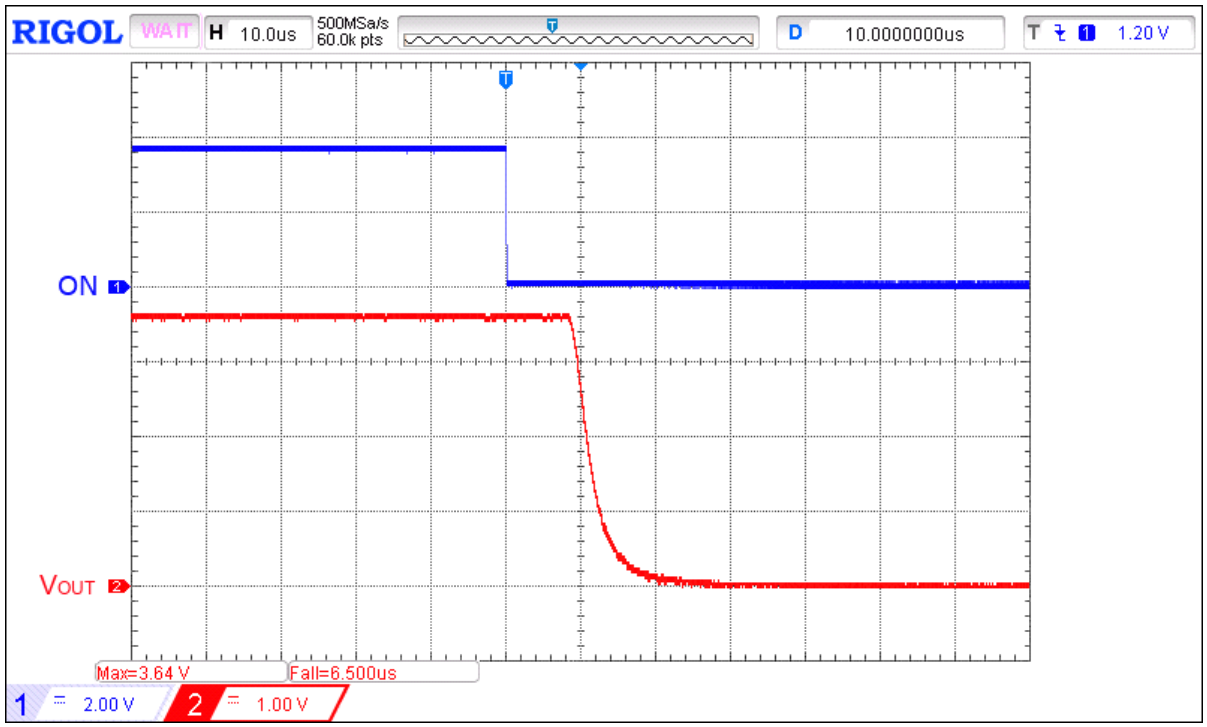


Figure 5. Typical Turn OFF operation waveform for V_{IN} = 3.6 V, R_{LOAD} = 10 Ω, no C_{LOAD}.

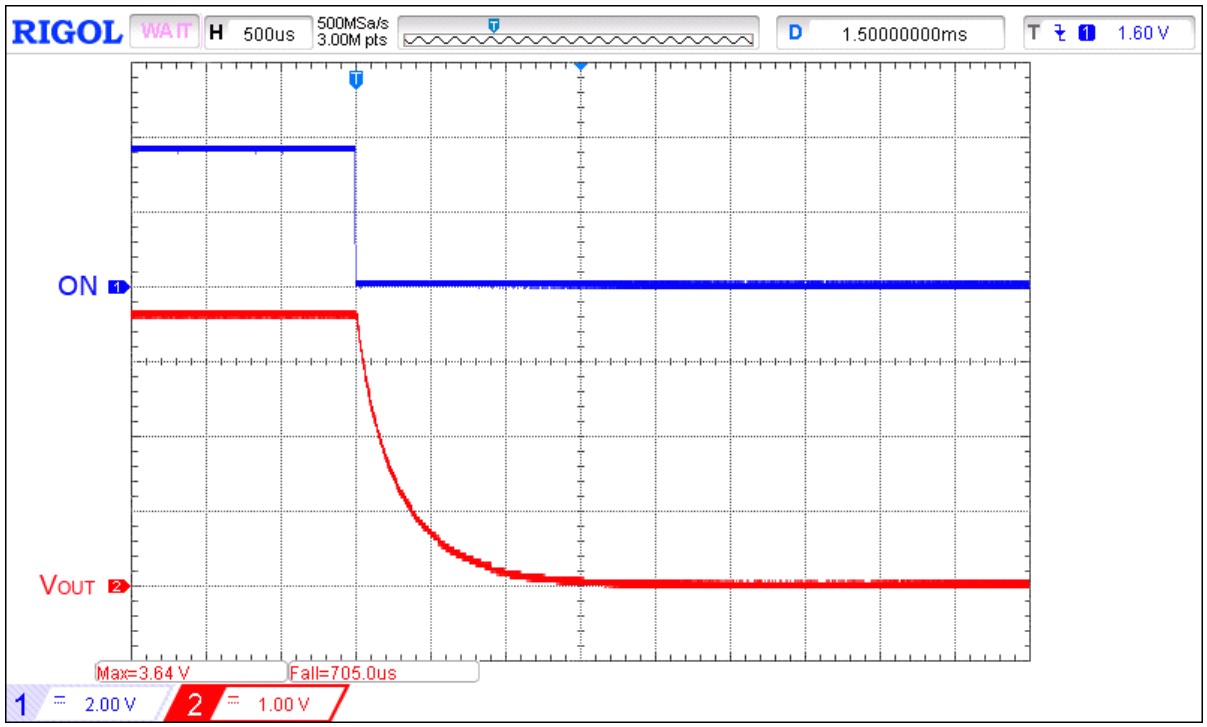


Figure 6. Typical Turn OFF operation waveform for V_{IN} = 3.6 V, C_{LOAD} = 30 µF, R_{LOAD} = 10 Ω

Typical ACL and Thermal Protection Operation Waveform

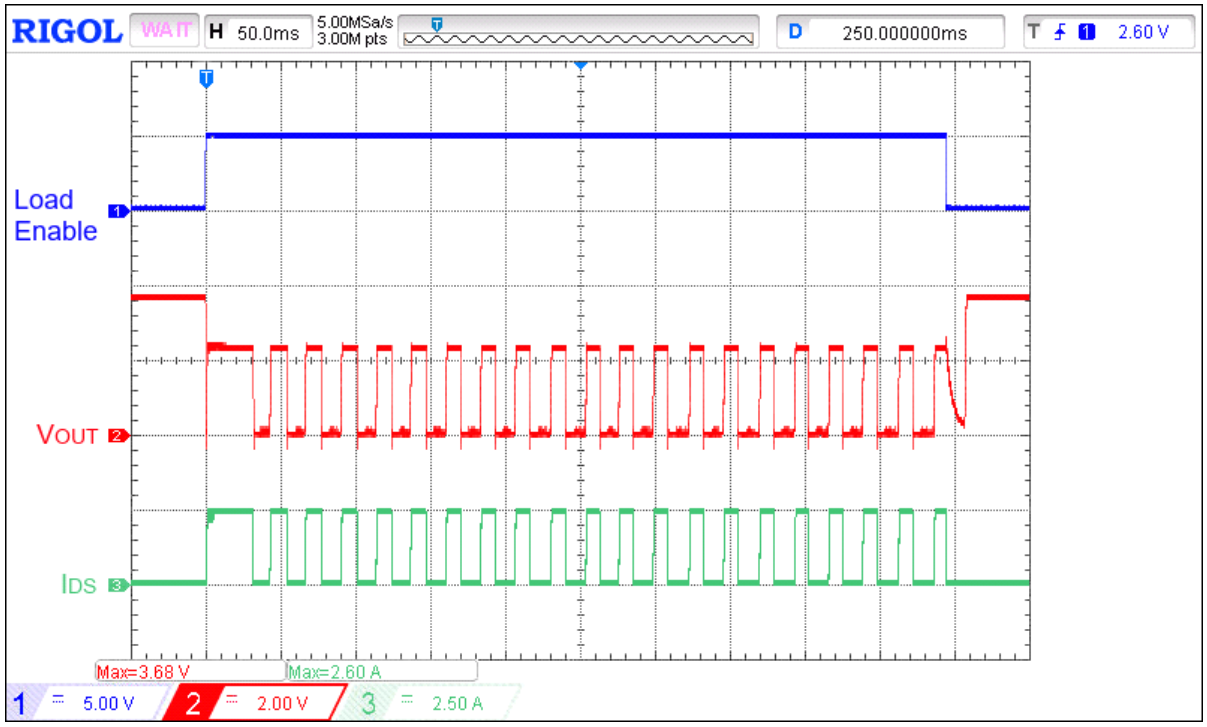


Figure 7. Typical ACL and Thermal Protection operation waveform for V_{IN} = 3.6 V, C_{LOAD} = 30 µF, R_{LOAD} = 0.5 Ω

Applications Information

SLG59M1685C Power-Up/Power-Down Sequence Considerations

During power-up operation, the SLG59M1685C's internal circuitry is activated once V_{IN} reaches 1.07 V. Once V_{IN} has reached 90% of its steady-state value (and within the SLG59M1685C's nominal supply voltage range of 1.3 V to 3.6 V), the ON pin can then be toggled LOW-to-HIGH to close the switch.

A nominal power-up sequence is to apply V_{IN} first and then toggling the ON pin LOW-to-HIGH after V_{IN} is (at a minimum) > 1.07 V or at least 90% of its final value.

A nominal power-down sequence is the power-up sequence in reverse order.

If V_{IN} and ON are applied at the same time, a voltage glitch may appear on the output pin at V_{OUT}. To prevent glitches at the output, it is recommended to connect at least 1 µF capacitor from the V_{OUT} pin to GND and to keep V_{IN} ramp times higher than 2 ms.

As illustrated in the typical performance transient scope captures, the V_{OUT} output follows a linear ramp when the power switch is turned on.

If ON and VIN are tied together and powered up, the IPS can be turned on, but the behavior may differ from datasheet specifications.

SLG59M1685C Current Limiting Operation

The SLG59M1685C has two types of current limiting triggered by the output (VOUT) pin voltage.

1. Standard Current Limiting Mode (with Thermal Shutdown Protection)

When V_{OUT} > 250 mV, the output current is initially limited to the Active Current Limit (I_{ACL}) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the power switch's I_{ACL} threshold.

However, if a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the power switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed $THERM_{ON}$ specification, the FET is shut OFF completely, thereby allowing the die to cool. When the die cools to the listed $THERM_{OFF}$ temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

When V_{OUT} < 250 mV (which is the case with a hard short, such as a solder bridge on the power rail), the power switch's internal Short-circuit Current Limit (SCL) monitor limits the FET current to approximately 500 mA (the I_{SCL} threshold). While the internal Thermal Shutdown Protection circuit remains activated and since the I_{SCL} threshold is much lower than the I_{ACL} threshold, thermal shutdown protection may become activated only at higher ambient temperatures.

For more information on Dialog GreenFET3 integrated power switch features, please visit our Documents search page at our website and see App Note "AN-1068 GreenFET3 Integrated Power Switch Basics".

Power Dissipation

The junction temperature of the SLG59M1685C depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M1685C is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$P_D = RDS_{ON} \times I_{DS}^2$$

$$P_D = RDS_{ON} \times I_{DS}^2 + V_{IN} \times I_{IN}$$

where:
P_D = Power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{DS} = Output current, in Amps (A)
V_{IN} = Applied Supply Voltage, in Volts (V)
I_{IN} = IC's Supply Current, in Amps (A)

and

$$T_J = P_D \times \theta_{JA} + T_A$$

where:

T_J = Junction temperature, in Celsius degrees (°C)
θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)
T_A = Ambient temperature, in Celsius degrees (°C)

In current-regulation mode, SLG59M1685C power dissipation can be calculated by taking into account the voltage drop across the power switch (V_{IN} - V_{OUT}) and the magnitude of the output current in current-regulation mode (I_{ACL}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{ACL}$$

$$P_D = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:
P_D = Power dissipation, in Watts (W)
V_{IN} = Input Voltage, in Volts (V)
R_{LOAD} = Load Resistance, in Ohms (Ω)
I_{ACL} = Output regulated current, in Amps (A)
$V_{OUT} = R_{LOAD} \times I_{ACL}$, in Volts (V)

Layout Guidelines:

1. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 8, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1685C's VIN and VOUT pins;

3. The GND pin should be connected to system analog or power ground plane.

SLG59M1685C Evaluation Board:

A GFET3 Evaluation Board for SLG59M1685C is designed according to the statements above and is illustrated on Figure 8. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

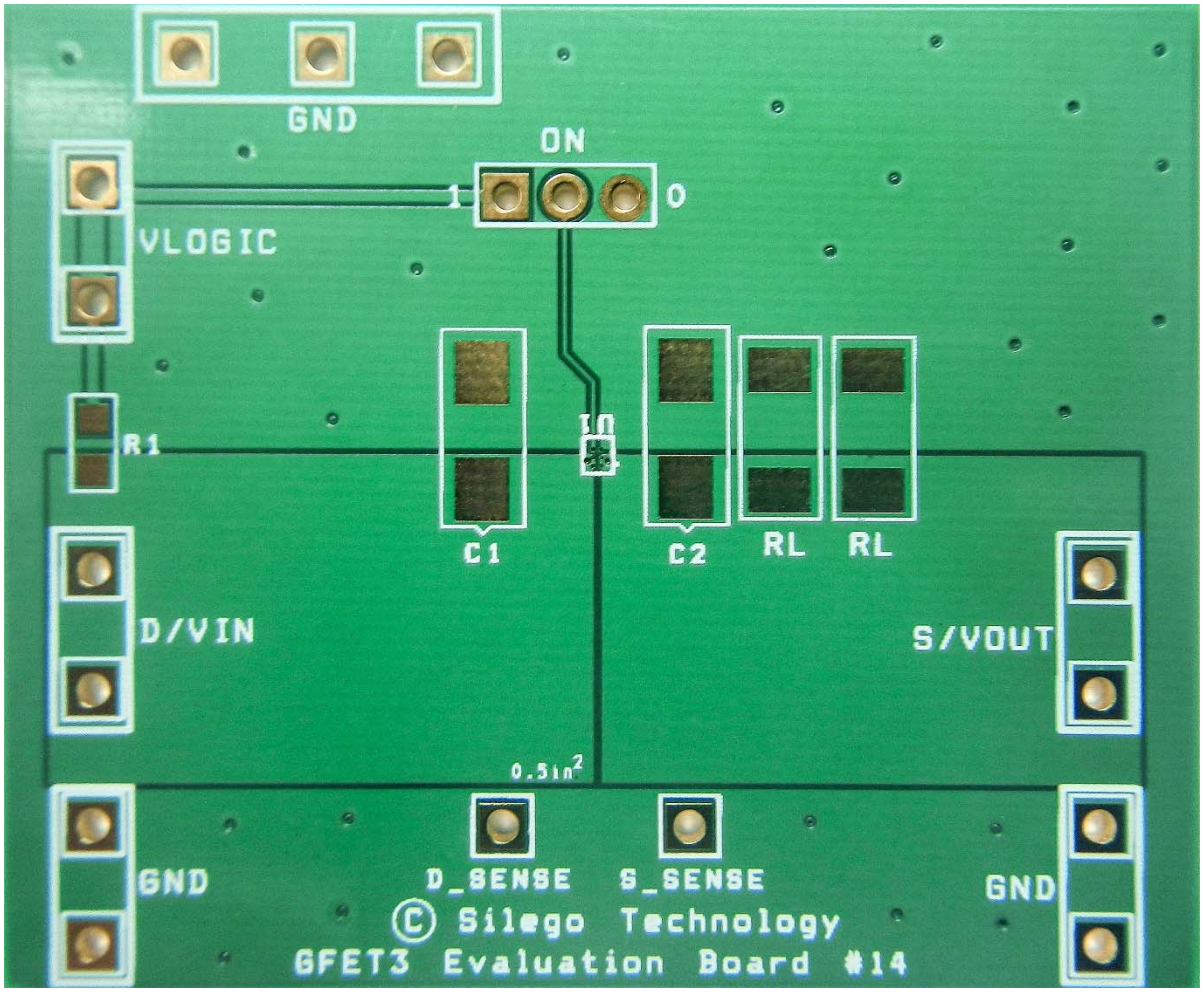


Figure 8. SLG59M1685C Evaluation Board.

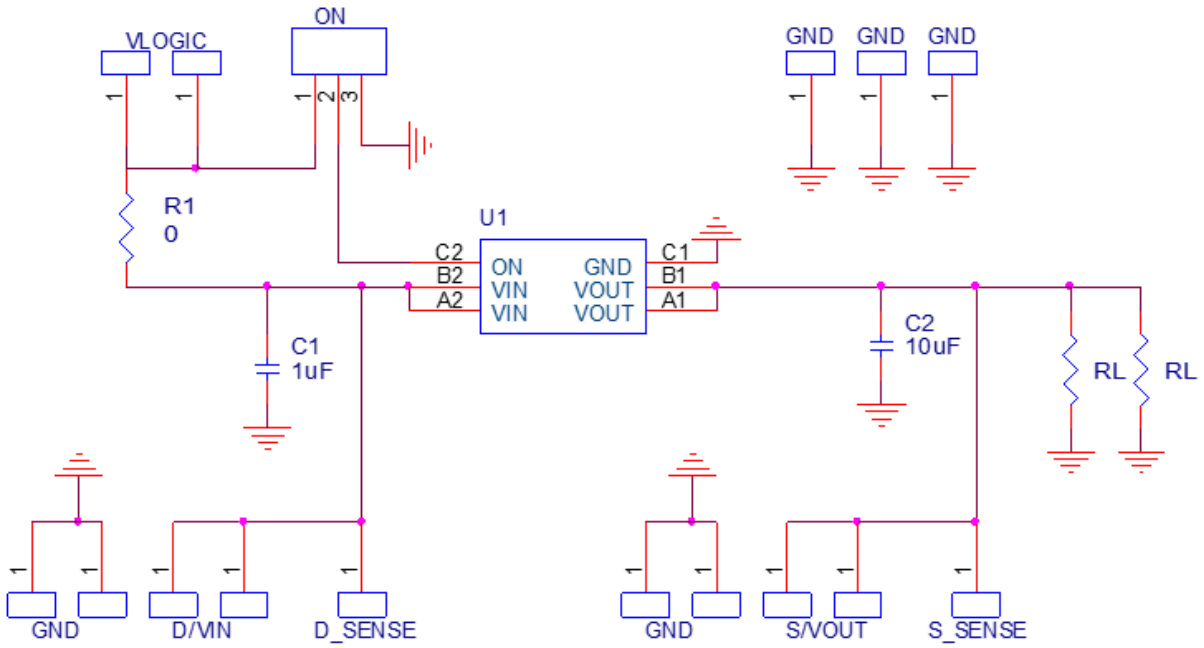


Figure 9. SLG59M1685C Evaluation Board Connection Circuit.

Basic Test Setup and Connections

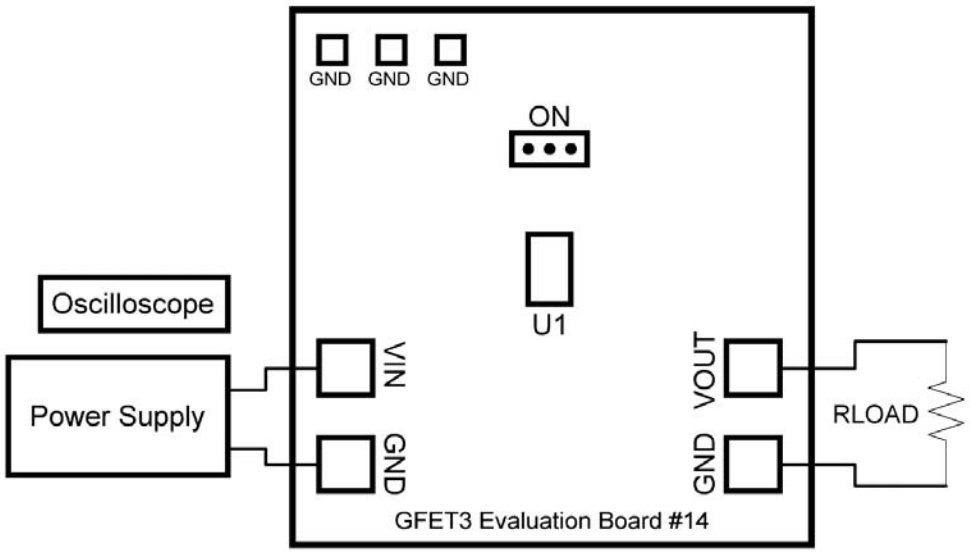


Figure 10. Typical connections for GFET3 Evaluation.

EVB Configuration

1.Connect oscilloscope probes to VIN, VOUT, ON, etc.;

2.Turn on Power Supply and set desired V_{IN} from 1.3 V…3.6 V range;

3.Toggle the ON signal High or Low to observe SLG59M1685C operation.

Package Top Marking System Definition

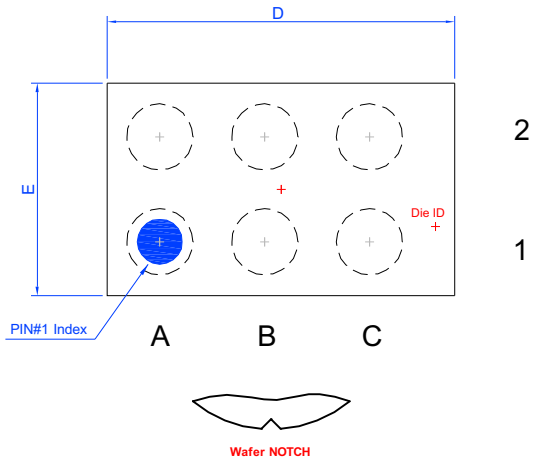
NNN - Serial Number Code Field[1]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9

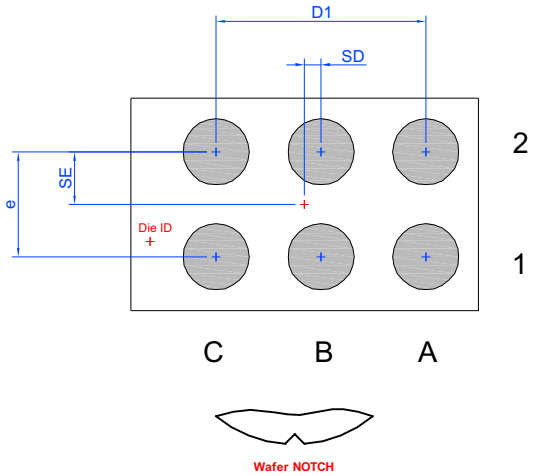
Package Drawing and Dimensions

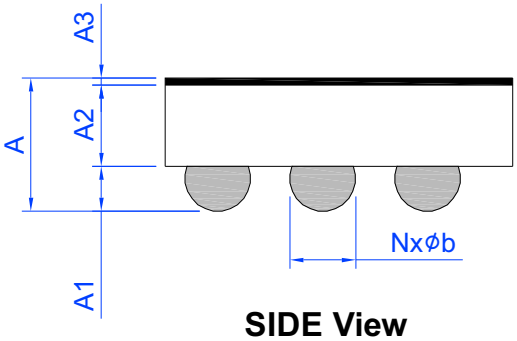
6 Pin WLCSP Green Package 0.71 x 1.16 mm

Laser Marking View



Bump View





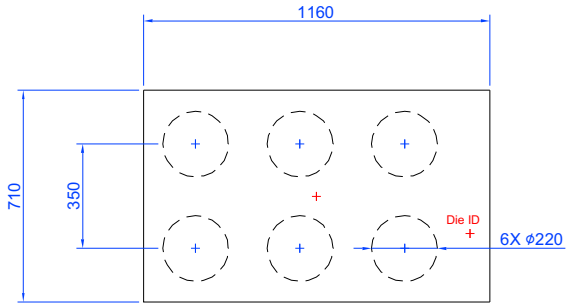
SIDE View

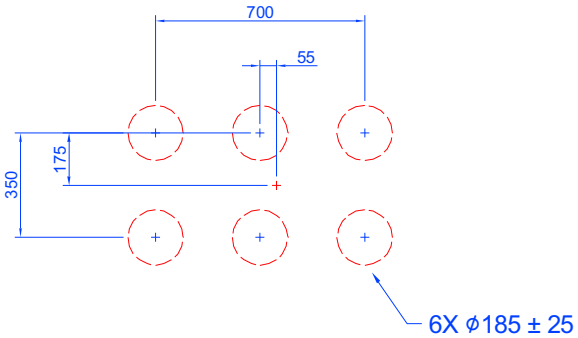
UNIT: mm							
Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.390	0.445	0.500	D	1.130	1.160	1.190
A1	0.125	0.150	0.175	E	0.680	0.710	0.740
A2	0.245	0.270	0.295	e	0.35 BSC		
A3	0.020	0.025	0.030	D1	0.70 BSC		
b	0.195	0.220	0.245	SD	0.055 BSC		
N	6 (bump)			SE	0.175 BSC		

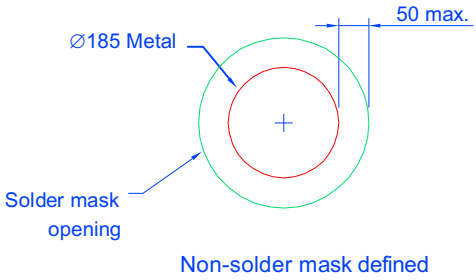
SLG59M1685C 6 Pin WLCSP PCB Landing Pattern

Exposed Bump
(Laser marking view)

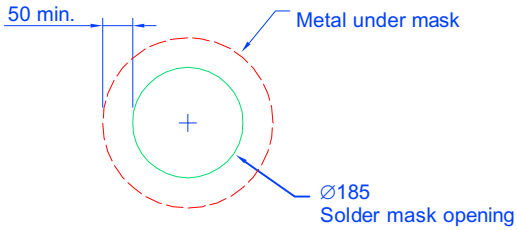
Recommended
Land Pattern







Non-solder mask defined



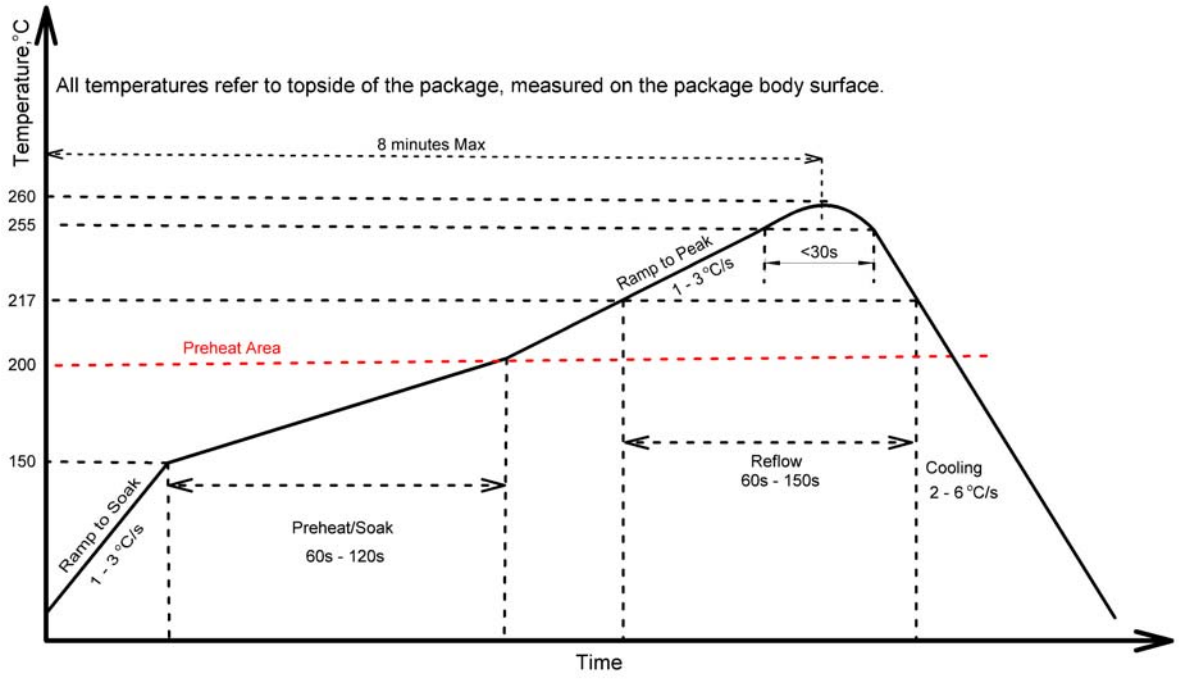
Solder mask defined

Solder mask detail (not to scale)

Unit: µm

Recommended Reflow Soldering Profile

For successful reflow of the SLG59M1685C a recommended thermal profile is illustrated below:



Note: This reflow profile is for classification/preconditioning and are not meant to specify board assembly profile. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed parameters depicted on figure above.

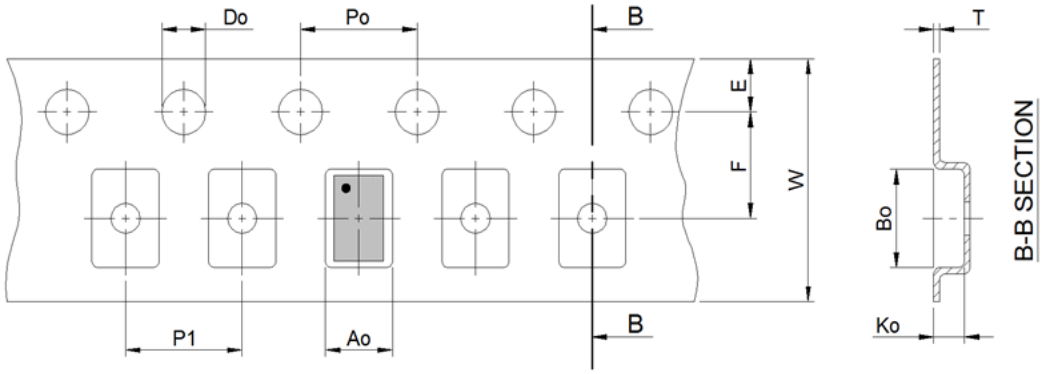
Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.352 mm^3 (nominal).

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP 6L 0.71 x 1.16 mm 0.35P Green	6	0.71 x 1.16	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
WLCSP 6L 0.71 x 1.16 mm 0.35P Green	0.77	1.22	0.53	4	4	1.5	1.75	3.5	0.2



Refer to EIA-481 specification

Revision History

Date	Version	Change
10/23/2018	1.00	Production Release