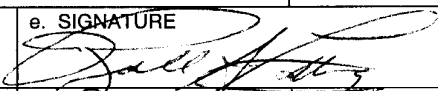| NOTICE OF REVISION (NOR) THIS REVISION DESCRIBED BELOW HAS BEEN AUTHORIZED FOR THE DOCUMENT LISTED	1. DATE (YYMMDD) 00/08/04	Form Approved OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 2 hours per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington VA 22202-4302, and to the Office of Management and Budget. Paperwork Reduction Project (0704-0188) Washington DC 20503. *PLEASE DO NOT RETURN YOUR COMPLETED FORM TO EITHER OF THESE ADDRESSES. RETURN COMPLETED FORM TO THE GOVERNMENT ISSUING CONTRACTING OFFICER FOR THE CONTRACT/PROCURING ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FORM.*	2. PROCURING ACTIVITY NO.
	3. DODAAC

4. ORIGINATOR a. TYPED NAME *(First, Middle Initial, Last)* Defense Supply Center, Columbus	b. ADDRESS *(Street, City, State, Zip Code)* Post Office Box 3990 Columbus, OH 43216-5000	5. CAGE CODE 037Z3	6. NOR NO. 5999-R004-00
		7. CAGE CODE 14933	8. DOCUMENT NO. 85008

9. TITLE OF DOCUMENT DELAY LINES, ACTIVE, 5 TAPS, 14-PIN DIP, TTL INTERFACED	10. REVISION LETTER		11. ECP NO. NONE
	a. CURRENT E	b. NEW F	

12. CONFIGURATION ITEM *(OR SYSTEM)* TO WHICH ECP APPLIES

13. DESCRIPTION OF REVISION

Page 1: Revisions letter column; add "F".
Revisions description column; add "Changes in accordance with NOR 5999-R004-00."
Revisions date column; add "00/08/04".

Page 8: Table, delete CAGE "16714" and all associated part numbers.

Page 9: Delete CAGE "16714, Rhombus Industries, Incorporated, 15801 Chemical Lane, Huntington Beach, CA 92649, (714) 898-0960" as a source of supply.

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. *(X one)*	X	(1) Existing document supplemented by this NOR may be used in manufacture
		(2) Revised document must be received before manufacturer may incorporate this change
		(3) Custodian of master document shall make above revision and furnish revised document

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DSCC-VAT	c. TYPED NAME *(First, Middle Initial, Last)* KENDALL A. COTTONGIM

d. TITLE CHIEF, ELECTRONIC COMPONENTS TEAM	e. SIGNATURE	f. DATE SIGNED *(YYMMDD)* 00/08/04

15a. ACTIVITY ACCOMPLISHING REVISION DSCC - VAT	b. REVISION COMPLETED *(Signature)*	c. DATE SIGNED *(YYMMDD)* 00/08/04

DD FORM 1695, APR 92   PREVIOUS EDITIONS ARE OBSOLETE

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	Added three sources for all dash numbers.	05 Sep 85	Ivan R. Jones
B	Modified figure 1 and added footnotes. Added tables II and III. Deleted references to MIL-D-23859; substituted references to MIL-D-83532. Updated vendor table.	01 Jul 87	Randy Larson
C	Changed standoff requirements in note 4 of figure 1.	19 Oct 87	Randy Larson
D	Corrected I_{CCL} max limit on table III. Added note 6 to figure 1. Changed pin length and added tolerances to pin dimensions. Added three vendors. Editorial changes throughout.	17 Aug 88	Randy Larson
E	Changed 3.3. Moved output rise time data from table III to 3.6. Changed several dimensions on figure 1 and added notes 7 and 8. Deleted vendors 92912 and 56289.	21 Dec 92	Tony Westphal

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

Prepared in accordance with MIL-STD-100   Selected item drawing

REV																								
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REV STATUS OF PAGES	REV	E	E	E	E	E	E	E	E	E										
	PAGES	1	2	3	4	5	6	7	8	9										

Original date of drawing: 25 February 1985	PREPARED BY Randy Larson	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO		
	CHECKED BY Randy Larson	TITLE DELAY LINES, ACTIVE, 5 TAPS, 14-PIN DIP, TTL INTERFACED		
	APPROVED BY Ivan R. Jones			
	SIZE A	CODE IDENT. NO. 14933	DWG NO. 85008	
	REV E	PAGE 1 OF 9		

1. SCOPE

1.1 Scope. This drawing describes the requirements for a family of active 14-pin, 5 tap, TTL interfaced delay lines.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

85008   -01

Drawing number   Dash number
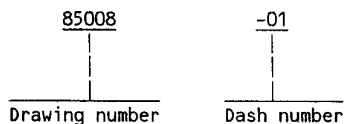
2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Government specifications and standards. The following specifications and standards form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards and supplement thereto, cited in the solicitation.

SPECIFICATIONS

    MILITARY

        MIL-S-19491   - Semiconductor Devices, Packaging of.

        MIL-M-38510   - Microcircuits, General Specification for.

        MIL-D-83532   - Delay Lines, Active, General Specification for.

STANDARDS

    MILITARY

        MIL-STD-883   - Test Methods and Procedures for Microelectronics.

        MIL-STD-1295 - Marking of Electrical and Electronic Parts.

(Copies of the specifications and standards required by contractors in connection with specific acquisition functions may be obtained from the DODSSP, Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this drawing, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Case material. The case material shall be molded diallyl phthalate or encapsulated epoxy and be in accordance with MIL-D-83532.

3.2 Terminal material. The terminal material shall be in accordance with MIL-M-38510.

3.3 Integrated circuits (IC's). IC's shall meet the requirements of MIL-STD-883, level B, as a minimum.

3.4 Design and dimensions. The design and dimensions shall be in accordance with figure 1 and table I.

3.5 Delay times. The delay times from input to all taps shall be as specified in table I (+25°C) and table II (-55°C and +125°C).

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3.6 <u>Output rise time</u>. 4 ns maximum under the following conditions:

V_{CC} = 5.0 V; TR_I ≤ 3 ns; C_L = 50 pF; R_L = 500 ohms. Applied to leading edge only.

3.7 <u>DC characteristics</u>. DC characteristics shall be as specified in table III.

3.8 <u>Delay line fan-out</u>. The delay line fan-out shall be 20 maximum (20 TTL loads per delay line).

3.9 <u>Tap fan-out</u>. The tap fan-out shall be 10/tap maximum (one tap is capable of driving 10 TTL load maximum).

3.10 <u>Marking</u>. Each delay line shall be marked on the top in accordance with method I of MIL-STD-1285 with the following information:

    a. Complete PIN (see 1.2).

    b. Index mark identification (over pin 1, input).

    c. Manufacturer's Commercial and Government Entity (CAGE) code or logo.

    d. Date code.

3.11 <u>Workmanship</u>. Parts shall be processed in such a manner as to be representative of controlled industrial techniques. Surfaces shall be free from burrs, die marks, chatter marks, scratches, dirt, grease, scale, splinters, and other defects that will affect life, serviceability, performance, or appearance. Visible parting line is acceptable.

3.12 <u>Certificate of compliance</u>. A certificate of compliance is required from each manufacturer requesting to be listed as a suggested source of supply (see 6.3). The certificate shall state that the manufacturer's product meets all the requirements of this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 <u>Quality conformance inspection</u>.

4.1.1 <u>Inspection of product for delivery</u>. Inspection of product for delivery shall consist of compliance with group A inspection for level A of MIL-D-83532.

4.1.2 <u>Inspection of packaging</u>. The sampling and inspection of the preservation, packing, and container marking shall be in accordance with the requirements for semiconductor devices in MIL-S-19491.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-S-19491.

6. NOTES

6.1 <u>Intended use</u>. Devices conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application.

6.2 <u>Ordering data</u>. The acquisition document should specify the following as a minimum:

    a. Complete PIN (see 1.2).

    b. Requirement for the manufacturer to include one copy of the quality conformance inspection data with each shipment of parts.

    c. Requirement for the manufacturer to notify the acquiring activity in the event of a change in product.

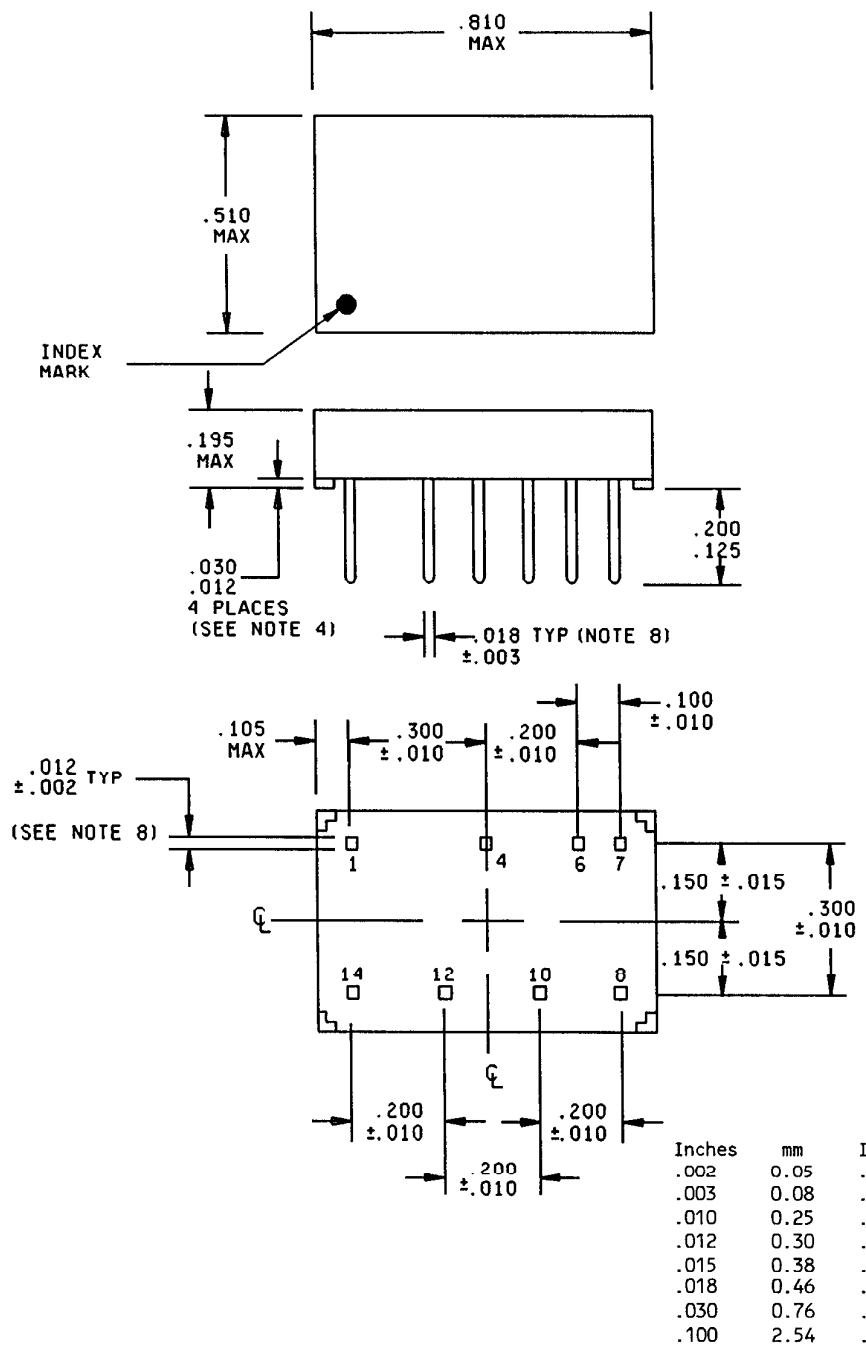| DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 85008
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.810
MAX

.510
MAX

INDEX
MARK

.195
MAX

.030
.012
4 PLACES
(SEE NOTE 4)

.200
.125

.018 TYP (NOTE 8)
±.003

.012
±.002 TYP

(SEE NOTE 8)

.105
MAX

.300
±.010

.200
±.010

.100
±.010

1   4   6 7

.150 ±.015

.300
±.010

.150 ±.015

14   12   10   8

.200
±.010

.200
±.010

.200
±.010

Inches	mm	Inches	mm
.002	0.05	.105	2.67
.003	0.08	.125	3.18
.010	0.25	.150	3.81
.012	0.30	.195	4.95
.015	0.38	.200	5.08
.018	0.46	.300	7.62
.030	0.76	.510	12.95
.100	2.54	.810	20.57

FIGURE 1. Design and dimensions.

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TAP1 TAP2 TAP3 TAP4

12   4   10   6   8   OUT

V_{CC} 14

IN   1

7
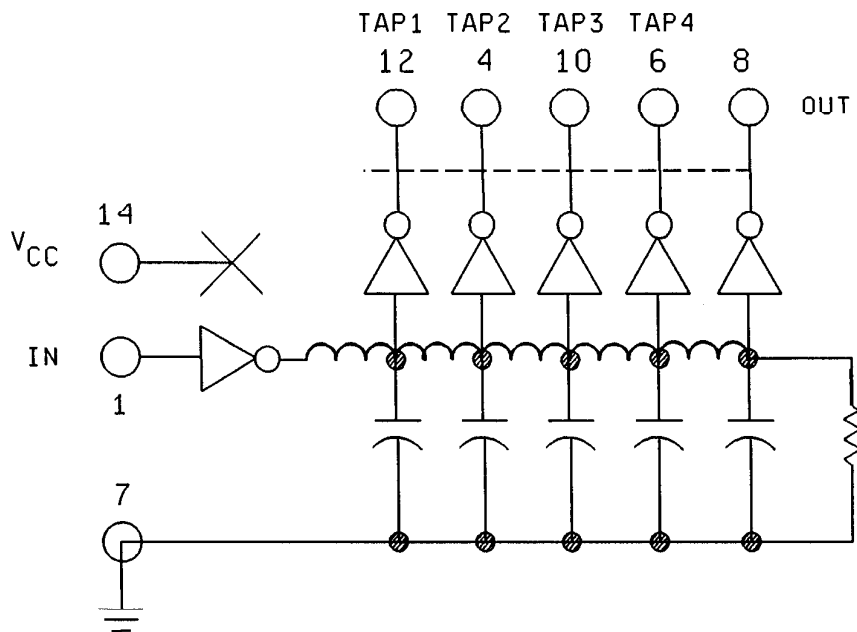
CIRCUIT DIAGRAM

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Unless otherwise specified, tolerance is ±.005 (0.13 mm).
4. Location and shape of standoffs are optional.
5. Pins 2, 3, 5, 9, 11, and 13 may be omitted at the manufacturer's option.
6. Tolerances on dimensions separating leads are nonaccumulative.
7. Leads shall be free of case meniscus and other foreign material and shall be solderable for a minimum of .010 inch above the seating plane of the delay line.
8. Leads may be round at the discretion of the manufacturer. Round lead diameter shall be .020 ±.002.

FIGURE 1. Design and dimensions – Continued.

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TABLE I.   Delay times at +25°C, V_{CC} = 5.00 ±.01 volts.

PIN 85008-	Delay times in nanoseconds				
	Pin 12 tap 1	Pin 4 tap 2	Pin 10 tap 3	Pin 6 tap 4	Pin 8 output
01	5 ±2 ns	10 ±2 ns	15 ±2 ns	20 ±2 ns	25 ±2 ns
02	6 ±2 ns	12 ±2 ns	18 ±2 ns	24 ±2 ns	30 ±2 ns
03	7 ±2 ns	14 ±2 ns	21 ±2 ns	28 ±2 ns	35 ±2 ns
04	8 ±2 ns	16 ±2 ns	24 ±2 ns	32 ±2 ns	40 ±2 ns
05	9 ±2 ns	18 ±2 ns	27 ±2 ns	36 ±2 ns	45 ±5%
06	10 ±2 ns	20 ±2 ns	30 ±2 ns	40 ±2 ns	50 ±5%
07	15 ±2 ns	30 ±2 ns	45 ±5%	60 ±5%	75 ±5%
08	20 ±2 ns	40 ±2 ns	60 ±5%	80 ±5%	100 ±5%
09	25 ±2 ns	50 ±5%	75 ±5%	100 ±5%	125 ±5%
10	30 ±2 ns	60 ±5%	90 ±5%	120 ±5%	150 ±5%
11	35 ±2 ns	70 ±5%	105 ±5%	140 ±5%	175 ±5%
12	40 ±2 ns	80 ±5%	120 ±5%	160 ±5%	200 ±5%
13	45 ±5%	90 ±5%	135 ±5%	180 ±5%	225 ±5%
14	50 ±5%	100 ±5%	150 ±5%	200 ±5%	250 ±5%
15	60 ±5%	120 ±5%	180 ±5%	240 ±5%	300 ±5%
16	70 ±5%	140 ±5%	210 ±5%	280 ±5%	350 ±5%
17	80 ±5%	160 ±5%	240 ±5%	320 ±5%	400 ±5%
18	90 ±5%	180 ±5%	270 ±5%	360 ±5%	450 ±5%
19	100 ±5%	200 ±5%	300 ±5%	400 ±5%	500 ±5%

TABLE II.   Delay times at –55°C and +125°C, V_{CC} = 5.00 ±.01 volts.

PIN 85008-	Delay times in nanoseconds				
	Pin 12 tap 1	Pin 4 tap 2	Pin 10 tap 3	Pin 6 tap 4	Pin 8 output
01	5 ±3 ns	10 ±3 ns	15 ±3 ns	20 ±3 ns	25 ±3 ns
02	6 ±3 ns	12 ±3 ns	18 ±3 ns	24 ±3 ns	30 ±3 ns
03	7 ±3 ns	14 ±3 ns	21 ±3 ns	28 ±3 ns	35 ±3 ns
04	8 ±3 ns	16 ±3 ns	24 ±3 ns	32 ±3 ns	40 ±3 ns
05	9 ±3 ns	18 ±3 ns	27 ±3 ns	36 ±3 ns	45 ±8%
06	10 ±3 ns	20 ±3 ns	30 ±3 ns	40 ±3 ns	50 ±8%
07	15 ±3 ns	30 ±3 ns	45 ±8%	60 ±8%	75 ±8%
08	20 ±3 ns	40 ±3 ns	60 ±8%	80 ±8%	100 ±8%
09	25 ±3 ns	50 ±8%	75 ±8%	100 ±8%	125 ±8%
10	30 ±3 ns	60 ±8%	90 ±8%	120 ±8%	150 ±8%
11	35 ±3 ns	70 ±8%	105 ±8%	140 ±8%	175 ±8%
12	40 ±3 ns	80 ±8%	120 ±8%	160 ±8%	200 ±8%
13	45 ±8%	90 ±8%	135 ±8%	180 ±8%	225 ±8%
14	50 ±8%	100 ±8%	150 ±8%	200 ±8%	250 ±8%
15	60 ±8%	120 ±8%	180 ±8%	240 ±8%	300 ±8%
16	70 ±8%	140 ±8%	210 ±8%	280 ±8%	350 ±8%
17	80 ±8%	160 ±8%	240 ±8%	320 ±8%	400 ±8%
18	90 ±10%	180 ±8%	270 ±8%	360 ±8%	450 ±8%
19	100 ±10%	200 ±8%	300 ±8%	400 ±8%	500 ±8%

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TABLE III. DC characteristics.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Limits		Unit
			Min	Max	
High level output voltage	V_{OH}	$V_{CC} = 4.5$ V $V_{IH} = 2.0$ V $I_{OH} = -1$ mA	2.5		V
Low level output voltage	V_{OL}	$V_{CC} = 4.5$ V $V_{IL} = 0.8$ V $I_{OL} = 20$ mA		.5	V
Input clamp voltage	V_{IC}	$V_{CC} = 4.5$ V $I_I = -18$ mA $T_C = +25°C$		-1.2	V
High level input current	I_{IH1}	$V_{CC} = 5.5$ V, $V_{IH} = 2.7$ V		50	μA
	I_{IH2}	$V_{CC} = 5.5$ V, $V_{IH} = 5.5$ V		1000	μA
Low level input current	I_{IL}	$V_{CC} = 5.5$ V, $V_{IL} = .5$ V		-2.00	mA
Short circuit output current	I_{OS}	$V_{CC} = 5.5$ V, $V_{OS} = 0.0$ V Not more than one output shorted at a time	-40	-150	mA
Low level supply current	I_{CCL}	$V_{CC} = 5.5$ V $V_I = 0.0$ V		75	mA

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6.3 <u>Suggested sources of supply</u>. Suggested sources of supply are listed below. Additional sources will be added as they become available. This table is not a qualified products list or an approved source list. The vendors indicated have submitted certificates of compliance to DESC; however, parts may be ordered from any manufacturer who agrees to supply components which conform to all the requirements of this drawing.

DESC PIN 85008-	Similar vendor PIN and CAGE code 1/					
	00222	50965	22519	20933	16714	62694
01	9T25S	4508-01	DDU6-8512-1	00T204	DSP008-01	L-13-904
02	9T30S	4508-02	DDU6-8512-2	00T205	DSP008-02	L-13-905
03	9T35S	4508-03	DDU6-8512-3	00T206	DSP008-03	L-13-906
04	9T40S	4508-04	DDU6-8512-4	00T207	DSP008-04	L-13-907
05	9T45S	4508-05	DDU6-8512-5	00T208	DSP008-05	L-13-908
06	9T50S	4508-06	DDU6-8512-6	00T209	DSP008-06	L-13-909
07	9T75S	4508-07	DDU6-8512-7	00T210	DSP008-07	L-13-910
08	9T100S	4508-08	DDU6-8512-8	10T363	DSP008-08	L-13-911
09	9T125S	4508-09	DDU6-8512-9	10T364	DSP008-09	L-13-912
10	9T150S	4508-10	DDU6-8512-10	10T365	DSP008-10	L-13-913
11	9T175S	4508-11	DDU6-8512-11	10T366	DSP008-11	L-13-914
12	9T200S	4508-12	DDU6-8512-12	10T367	DSP008-12	L-13-915
13	9T225S	4508-13	DDU6-8512-13	10T368	DSP008-13	L-13-916
14	9T250S	4508-14	DDU6-8512-14	10T369	DSP008-14	L-13-917
15	9T300S	4508-15	DDU6-8512-15	10T370	DSP008-15	L-13-918
16	9T350S	4508-16	DDU6-8512-16	10T371	DSP008-16	L-13-919
17	9T400S	4508-17	DDU6-8512-17	10T372	DSP008-17	L-13-920
18	9T450S	4508-18	DDU6-8512-18	10T373	DSP008-18	L-13-921
19	9T500S	4508-19	DDU6-8512-19	10T374	DSP008-19	L-13-922

1/ CAUTION: Vendor PIN's are provided for reference purposes only. Do not use these numbers for item acquisition and marking.

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Vendor CAGE number	Vendor name and address
00222	ESC Electronics Corporation 534 Bergen Boulevard Palisades Park, NJ 07650 (201) 947-0400
16714	Rhombus Industries, Incorporated 15801 Chemical Lane Huntington Beach, CA 92649 (714) 898-0960
20933	Kappa Technologies, Incorporated 1443 Pinewood Street Rahway, NJ 07065 (908) 396-9400
22519	Data Delay Devices, Incorporated 3 Mt. Prospect Avenue Clifton, NJ 07013 (201) 773-2299
50965	Princeton Advanced Components, Incorporated 860 State Road Princeton, NJ 08540 (609) 924-2444
62694	JBM Electronics 1 Commerce Drive Bedford, NH 03110 (603) 623-0222

6.4 Assistance. Questions or comments concerning this drawing should be referred to DESC-EMM, 1507 Wilmington Pike, Dayton, OH 45444-5270, telephone (513) 296-5255.

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