S6AE101A

Energy Harvesting PMIC for Wireless Sensor Node

Data Sheet (Preliminary)

Notice to Readers: This document states the current technical specifications regarding the Cypress product(s) described herein. Cypress Semiconductor Corp. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur.

Publication Number S6AE101A_DS405-00026 Revision 0.1 Issue Date April 27, 2015

Notice On Data Sheet Designations

Cypress Semiconductor Corp. issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Cypress data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Cypress Semiconductor Corp. is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Cypress Semiconductor Corp. therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Cypress Semiconductor Corp. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Cypress Semiconductor Corp. reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Cypress places the following conditions upon Preliminary content:

> "This document states the current technical specifications regarding the Cypress product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications."

Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or VIO range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Cypress Semiconductor Corp. applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Cypress product(s) described herein. Cypress Semiconductor Corp. deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local sales office.

S6AE101A

Energy Harvesting PMIC for Wireless Sensor Node

Data Sheet (Preliminary)

1. Description

The S6AE101A is a power management IC (PMIC) for energy harvesting that is built into circuits of solar cells connected in series, output power control circuits, output capacitor storage circuits, and power switching circuits of primary batteries. Super-low-power operation is possible using a consumption current of only 250 nA and startup power of only 1.2 μW. As a result, even slight amounts of power generation can be obtained from compact solar cells under low-brightness environments of approximately 100 lx.

The S6AE101A stores power generated by solar cells to an output capacitor using built-in switch control, and it turns on the power switching circuit while the capacitor voltage is within a preset maximum and minimum range for supplying energy to a load. If the power generated from solar cells is not enough, energy can also be supplied in the same way as solar cells from connected primary batteries for auxiliary power. Also, an overvoltage protection (OVP) function is built into the input pins of the solar cells, and the open voltage of solar cells is used by this IC to prevent an overvoltage state.

The S6AE101A is provided as a battery-free wireless sensor node solution that is operable by super-compact solar cells.

2. Features

- Input power selection control: Solar cell or primary battery
- Operated by solar cells without the need for primary batteries
- Storage of energy from power supply to storage capacitors
- Output power gating control, output voltage regulation
- Operation input voltage range
  - Solar cell power : 2.0V to 5.5V
  - Primary battery power : 2.0V to 5.5V
- Adjustable output voltage range : 1.1V to 5.2V
- Low-consumption current : 250 nA
- Minimum input power at startup : 1.2 μW
- Input overvoltage protection : 5.4V
- Compact SON-10 package : 3 mm × 3 mm

3. Applications

- Energy harvesting power system with a very small solar cell
- Bluetooth Smart® sensor
- Wireless HVAC sensor
- Wireless lighting control
- Security system
- Smart home / Building / Industrial wireless sensor

Publication Number S6AE101A_DS405-00026 Revision 0.1 Issue Date April 27, 2015

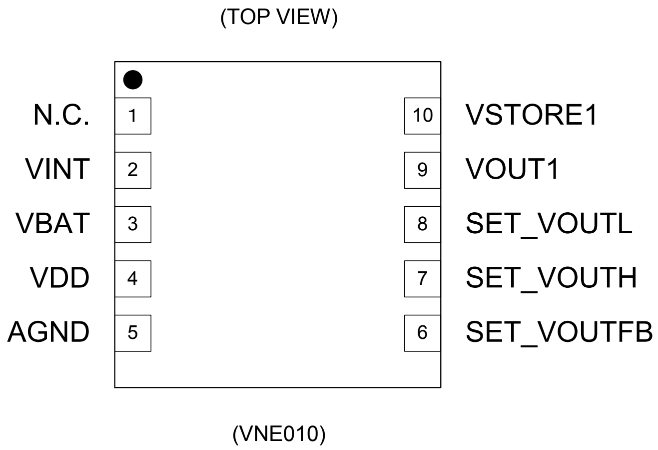
Table of Contents

Figures

Tables

4. Pin Assignment

Figure 4-1 Pin Assignment



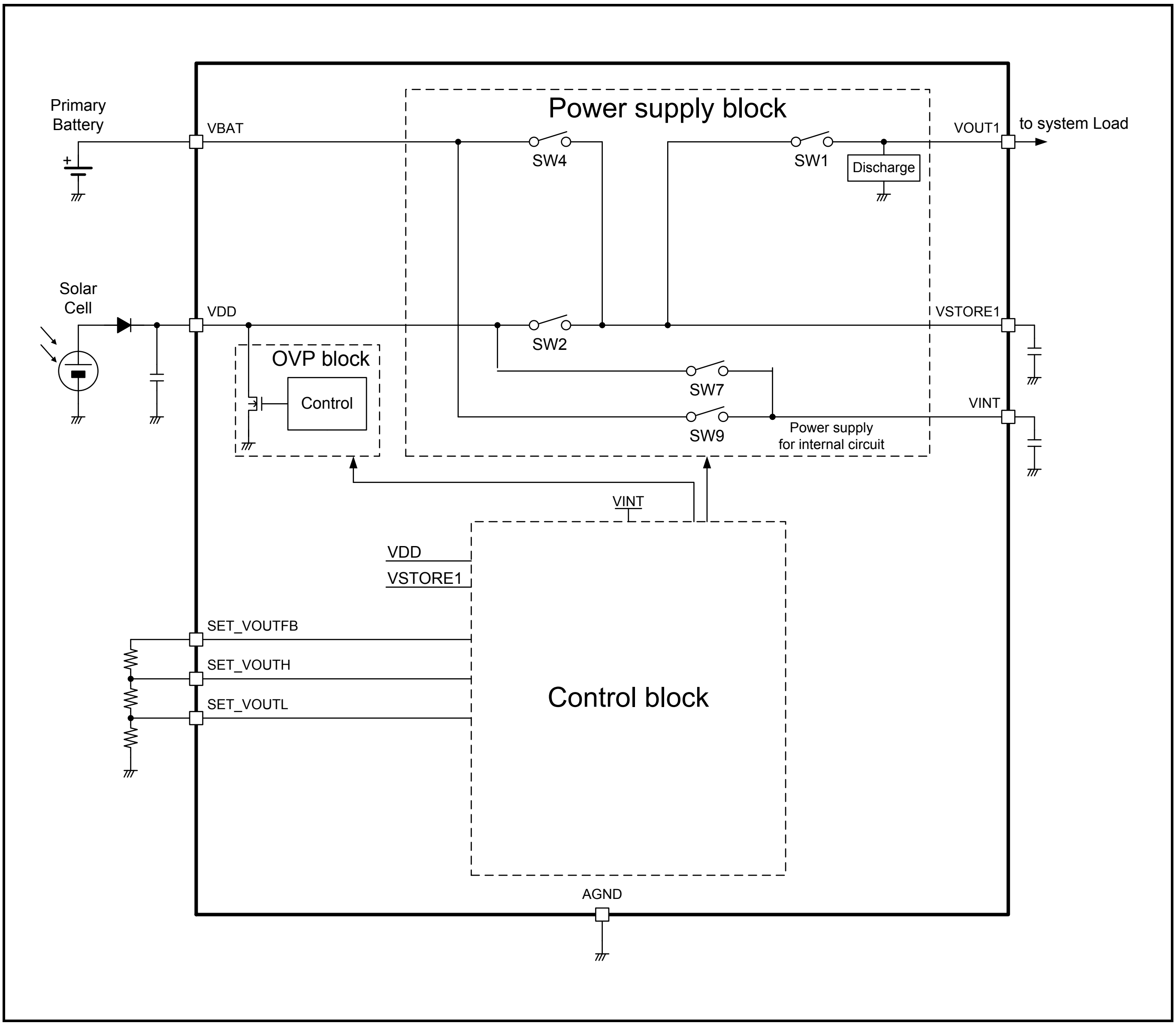
5. Pin Descriptions

Table 5-1 Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	N.C	−	Non connection pin (Leave this pin open)
2	VINT	O	Internal circuit storage output pin
3	VBAT	I	Primary battery input pin (when being not used, leave this pin open)
4	VDD	I	Solar cell input pin (when being not used, leave this pin open)
5	AGND	−	Ground pin.
6	SET_VOUTFB	O	Reference voltage output pin (for connecting resistor)
7	SET_VOUTH	I	VOUT1 output voltage setting pin (for connecting resistor)
8	SET_VOUTL	I	VOUT1 output voltage setting pin (for connecting resistor)
9	VOUT1	O	Output voltage pin
10	VSTORE1	O	Storage output pin

6. Block Diagram

Figure 6-1 Block Diagram



7. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage (*1)	V_{MAX}	VDD, VBAT pin	−0.3	+6.9	V
Signal input voltage(*1)	$V_{INPUTMAX}$	SET_VOUTH, SET_VOUTL pin	−0.3	V_{VDD}	V
VDD slew rate	V_{SLOPE}	VDD pin	−	0.1	mV/μs
Power dissipation (*1)	P_D	Ta ≤+ 25°C	−	1200 (*2)	mW
Storage temperature	T_{STG}	−	−55	+125	°C

*1: When GND=0V

*2: θja (wind speed 0m/s): +58°C/W

Warning:

1. *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.Do not exceed any of these ratings.*

8. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage 1 (*1)	V_{VDD}	VDD pin	2.0	3.3	5.5	V
Power supply voltage 2 (*1)	V_{VBAT}	VBAT pin	2.0	3.0	5.5	V
Signal input voltage (*1)	V_{INPUT}	SET_VOUTH, SET_VOUTL pin	−	−	VINT pin voltage	V
VOUT1 setting resistance	R_{VOUT}	Sum of R1, R2, R3	10	−	−	MΩ
VDD capacitance	C1	VDD pin	10	−	−	μF
VINT capacitance	C2	VINT pin	1	−	−	μF
VOUT maximum setting voltage	V_{SYSH}	VSTORE1 pin	1.25	−	5.2	V
VOUT minimum setting voltage	V_{SYSL}	VSTORE1 pin	1.1	−	V_{SYSH} ×0.9	V
Operating ambient temperature	Ta	−	−40	−	+85	°C

*1: When GND = 0V

Warning:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

9. Electrical Characteristics

The electrical characteristics excluding the effect of external resistors and external capacitors are shown in Table 9-1.

Table 9-1 Electrical Characteristics (System Overall)

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Minimum Input power in start-up	W_{START}	VDD pin, Ta = +25°C, V_{VOUTH} setting =3V, By applying 0.4μA to VDD, when VOUT1 reaches 3V×95% after the point when VDD reaches 3V.	–	–	1.2	μW
Consumption current 1	I_{QIN1}	VDD pin input current, VDD=3V, Open VBAT pin, V_{VOUTH}=1.25V setting, Ta=+25°C, SET_VOUTFB resistance>100MΩ, VOUT1 Load=0mA	–	250	375	nA
Power detection voltage	V_{DETH}	VDD, VBAT ,VINT pin	1.30	1.55	2.00	V
Power undetection voltage	V_{DETL}		1.15	1.45	1.90	V
Power detection hysteresis	V_{DETHYS}		–	0.1	–	V
VOUT maximum voltage	V_{VOUTH}	VSTORE1 pin, VOUT1 Load=0 mA	–	V_{SYSH}	–	V
Input power reconnect voltage	V_{VOUTM}	VSTORE1 pin, VOUT1 Load=0 mA	–	V_{VOUTH} ×0.95	–	V
VOUT minimum voltage	V_{VOUTL}	VSTORE1 pin, VOUT1 Load=0 mA	–	V_{SYSL}	–	V
OVP detection voltage	V_{OVPH}	VDD pin	5.2	5.4	5.5	V
OVP release voltage	V_{OVPL}		5.1	5.3	5.4	V
OVP detection hysteresis	V_{OVPHYS}		–	0.1	–	V
OVP protection current	I_{OVP}	VDD pin input current	6	–	–	mA

Table 9-2 Electrical Characteristics (Switch)

VDD ≥ 3V, VBAT ≥ 3V, VINT ≥ 3V, V_{VOUTL} ≥ 3V, VSTORE1 ≥ V_{VOUTL}

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
On resistance 1	R_{ON1}	SW1, In connection of VSTORE1 pin and VOUT1 pin	–	1.5	2.5	Ω
On resistance 2	R_{ON2}	SW2, In connection of VDD pin and VSTORE1 pin	–	5	10	kΩ
On resistance 4	R_{ON4}	SW4, In connection of VDD pin and VSTORE1 pin	–	5	10	kΩ
Discharge resistance	R_{DIS}	VOUT1 pin	–	1	2	kΩ

10. Functional Description

10.1 Power Supply Control

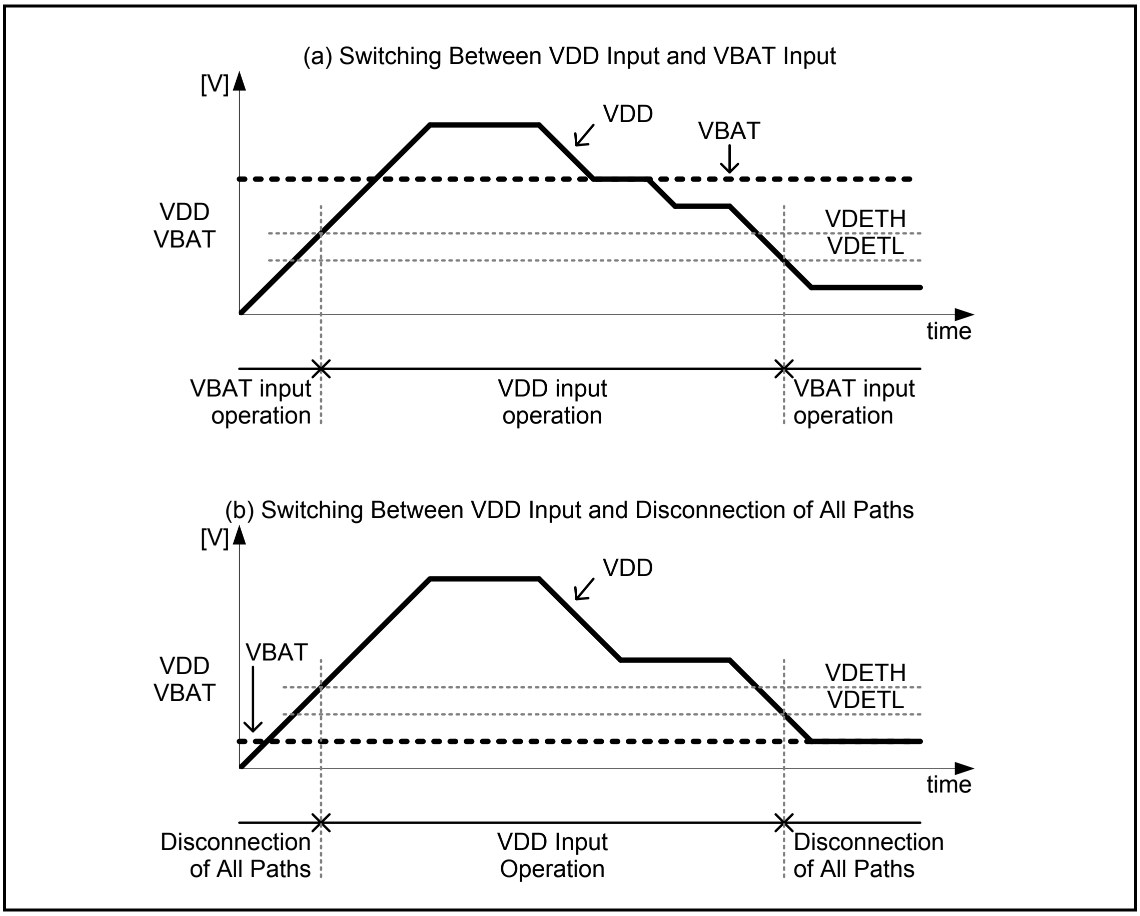
This IC can operate by two input power supplies, namely, the solar cell voltage VDD and the primary battery voltage VBAT. The voltages at the VDD pin and VBAT pin are monitored, and selection control of the input power supply is performed based on this voltage state (Table 10-1).

The input power (solar cell or primary battery) is temporarily stored to a capacitor connected to the VSTORE1 pin. When the voltage of the VSTORE1 pin reaches a certain threshold value or higher, the power switching switch (SW1) connects VSTORE1 and VOUT1.

Table 10-1 Input Power Supply Selection Control

VDD voltage (solar cell)	VBAT voltage (primary battery)	Operation
V_{DETH} (1.55V) or higher	V_{DETH} (1.55V) or higher	VDD input power supply is performed
	V_{DETL} (1.45V) or less	VDD input power supply is performed
V_{DETL} (1.45V) or less	V_{DETH} (1.55V) or higher	VBAT input power supply is performed
	V_{DETL} (1.45V) or less	All paths are disconnected

Figure 10-1 Input Power Selection Control



1. VDD input voltage operation

This section describes operation when the VDD pin is set as the input power (Figure 10-2).

[1] When the voltage of the VDD pin reaches the power detection voltage (V_{DETH} = 1.55V) or higher, the switch (SW2) connects VDD and VSTORE1 (path S1). Also, when the voltage of the VDD pin falls to the power undetection voltage (V_{DETL} = 1.45V) or less, SW2 disconnects the path S1.

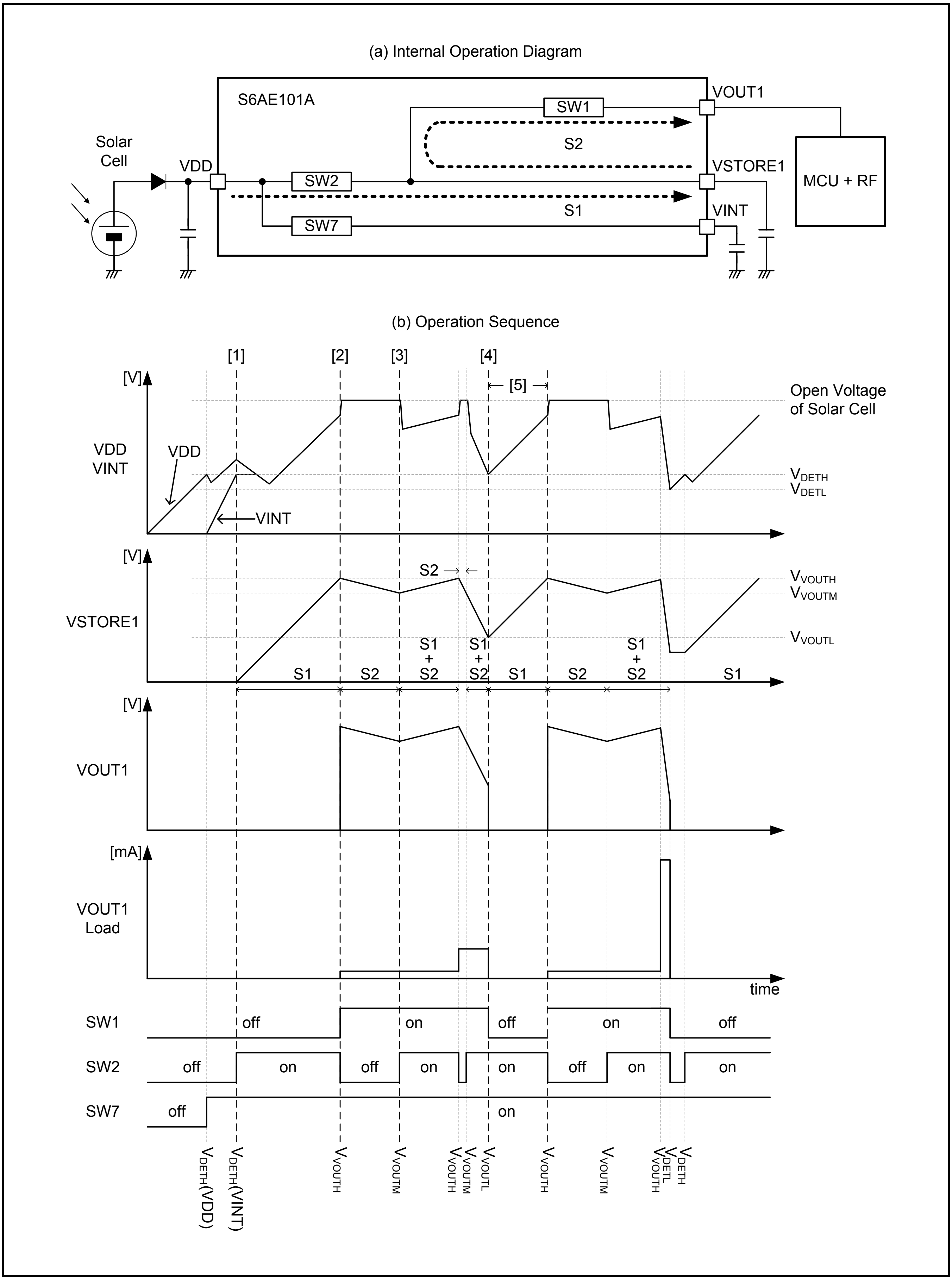
[2] When the voltage of the VSTORE1 pin reaches the threshold value (V_{VOUTH}) or higher that was set by the SET_VOUTH pin, SW2 disconnects the path S1. Also, the VOUT switch (SW1) connects VSTORE1 and VOUT1 (path S2).

[3] When the voltage of the VSTORE1 pin falls to the input power reconnect voltage (V_{VOUTM}) or less, SW2 connects the path S1 (path S1+S2).

[4] In addition, when the voltage falls to the threshold value (V_{VOUTL}) or less that was set by the SET_VOUTL pin, SW1 disconnects the path S2.

[5] When SW1 disconnects the path S2, the discharge function is activated.

Figure 10-2 VDD Pin Input Power Operation



2. VBAT input voltage operation

This section describes operation when the VBAT pin is set as the input power (Figure 10-3).

[1] When the voltage of the VBAT pin reaches the power detection voltage (V_{DETH} = 1.55V) or higher, the switch (SW2) connects VBAT and VSTORE1 (path S3). Also, when the voltage of the VDD pin falls to the power undetection voltage (V_{DETL} = 1.45V) or less, SW4 disconnects the path S3.

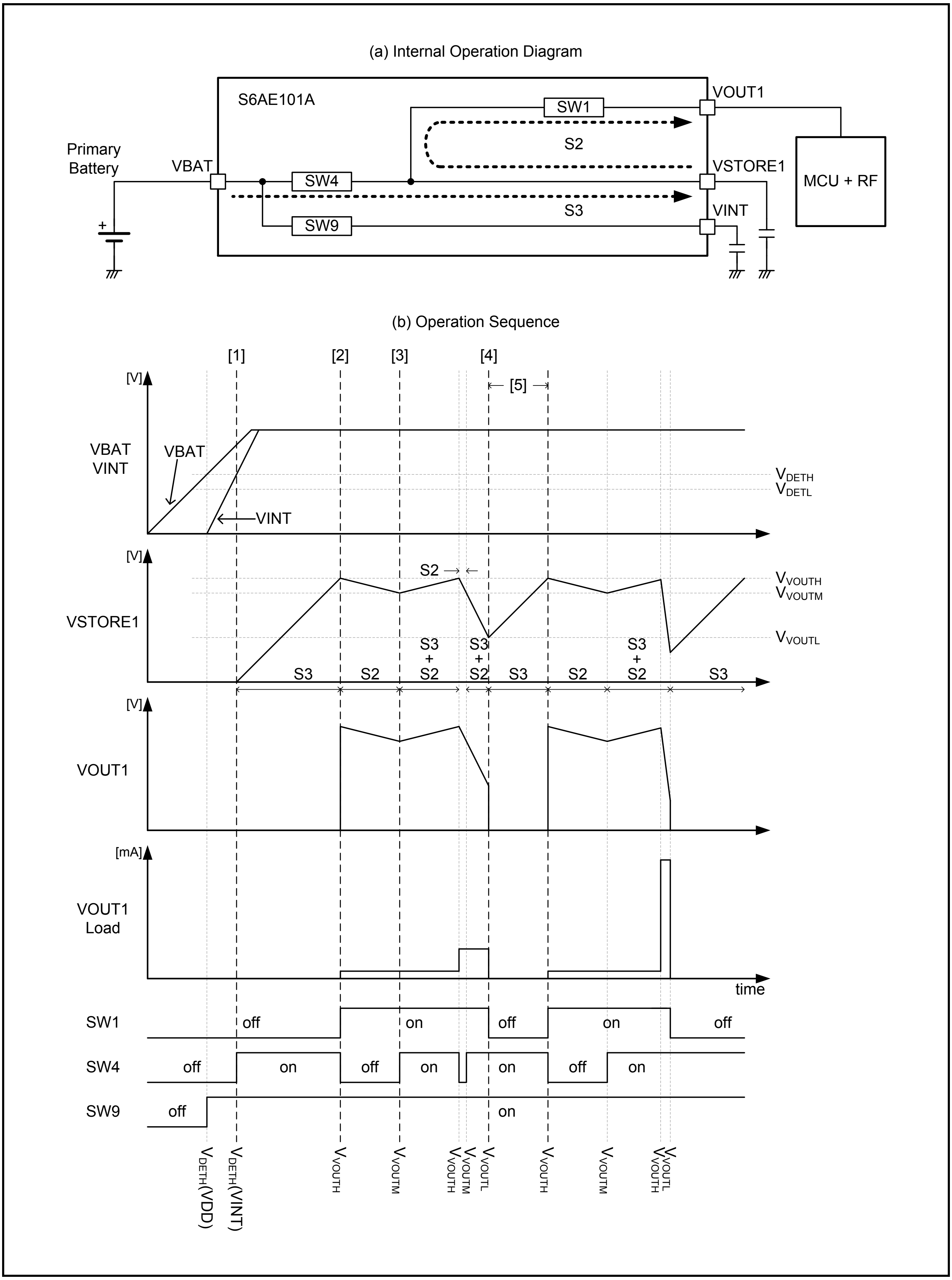
[2] When the voltage of the VSTORE1 pin reaches the threshold value (V_{VOUTH}) or higher that was set by the SET_VOUTH pin, SW4 disconnects the path S3. Also, the VOUT switch (SW1) connects VSTORE1 and VOUT1 (path S2).

[3] When the voltage of the VSTORE1 pin falls to the input power reconnect voltage (V_{VOUTM}) or less, SW4 connects the path S3 (path S3+S2).

[4] In addition, when the voltage falls to the threshold value (V_{VOUTL}) or less that was set by the SET_VOUTL pin, SW1 disconnects the path S2.

[5] When SW1 disconnects the path S2, the discharge function is activated.

Figure 10-3 VBAT Pin Input Power Operation



3. Input power supply switching

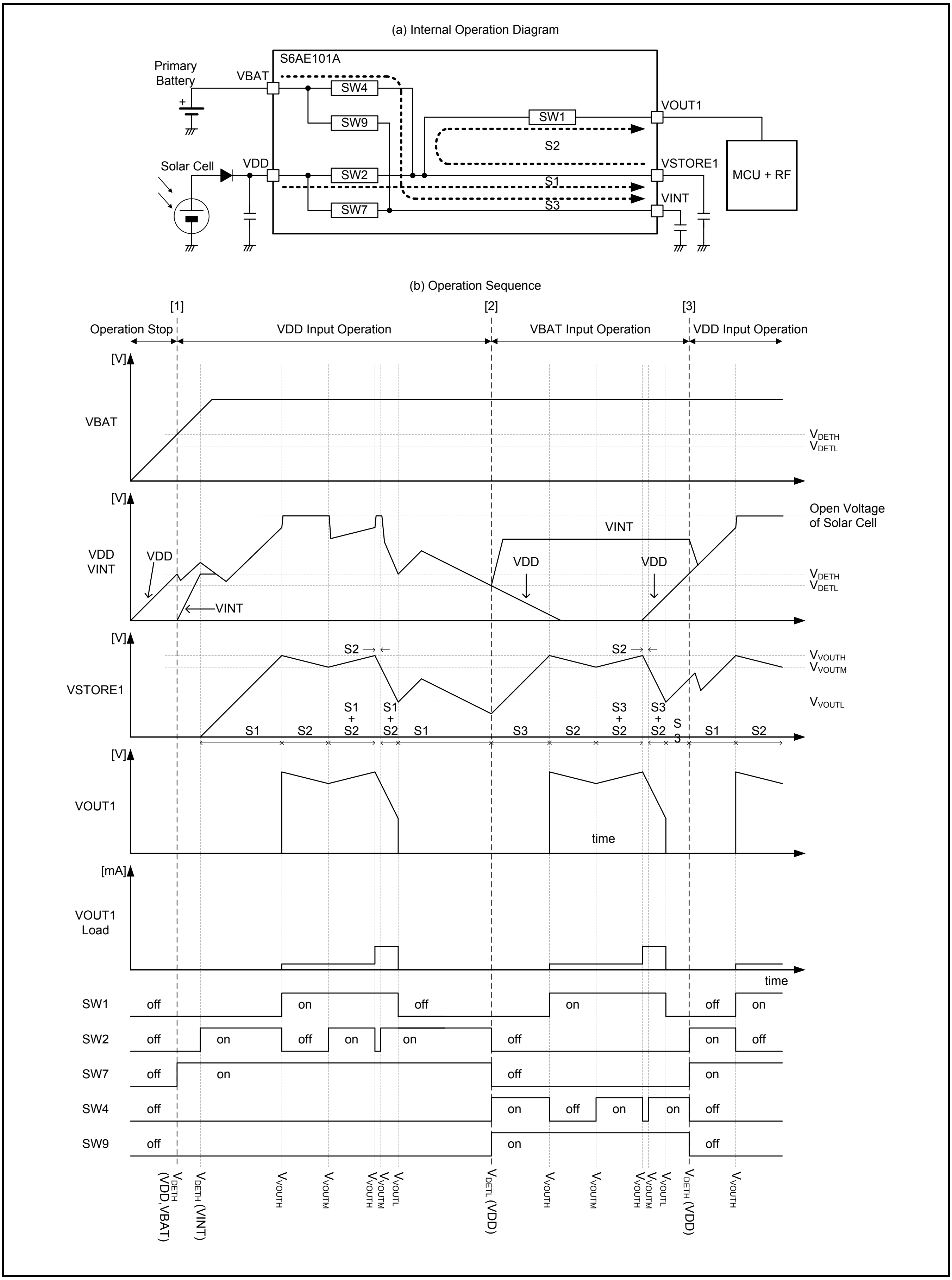
This section describes the input power switching operation (Figure 10-4).

[1] If the voltages of the VDD pin and VBAT pin increase from a state where both are less than the power detection voltage (V_{DETH} = 1.55V) so that the voltage of the VDD pin reaches the power detection voltage (V_{DETH} = 1.55V) or higher, and operation switches to VDD input power operation back from the stage of disconnecting all paths.

[2] When the voltage of the VBAT pin increases to the power detection voltage (V_{DETH} = 1.55V) or higher, if the power from the solar cell is reduced, and when the voltage of the VDD pin falls to the power undetection voltage (V_{DETL} = 1.45V) or less, operation switches from VDD input power operation to VBAT input power operation.

[3] When the amount of power supplied from the solar cell increases, and the voltage of the VDD pin reaches the power detection voltage (V_{DETH} = 1.55V) or higher, operation switches back to VDD input power operation. After switching, operation is performed based on VDD input power operation.

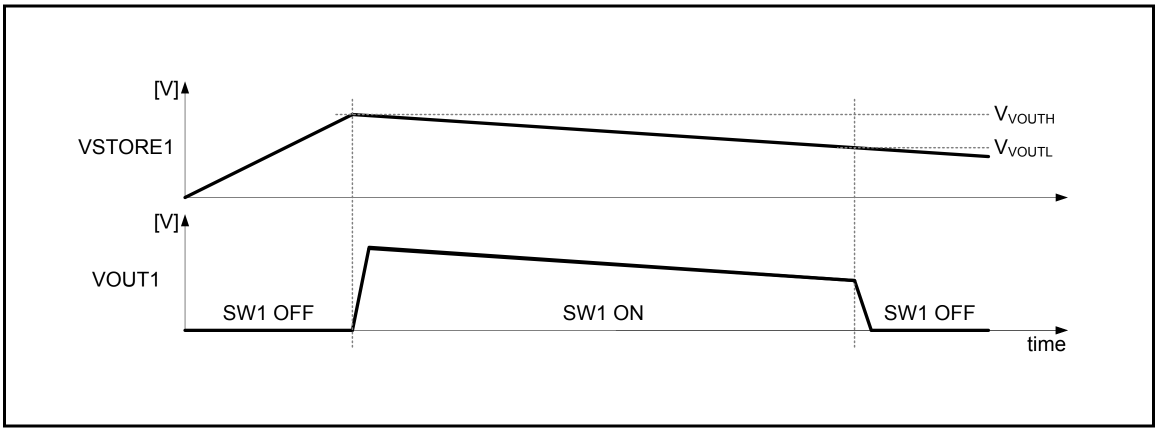
Figure 10-4 Input Power Switching



10.2 Power Gating

This IC has a power gating function for the external system. Once it is detected that the voltage of the VSTORE1 pin has reached the VOUT maximum voltage (V_{VOUTH}), the VSTORE1 pin and VOUT pin are connected by an internal switch until the VOUT minimum voltage (V_{VOUTL}) is reached.

Figure 10-5 Power Gating Operation



10.3 Discharge

This IC includes a VOUT1 pin discharge function.

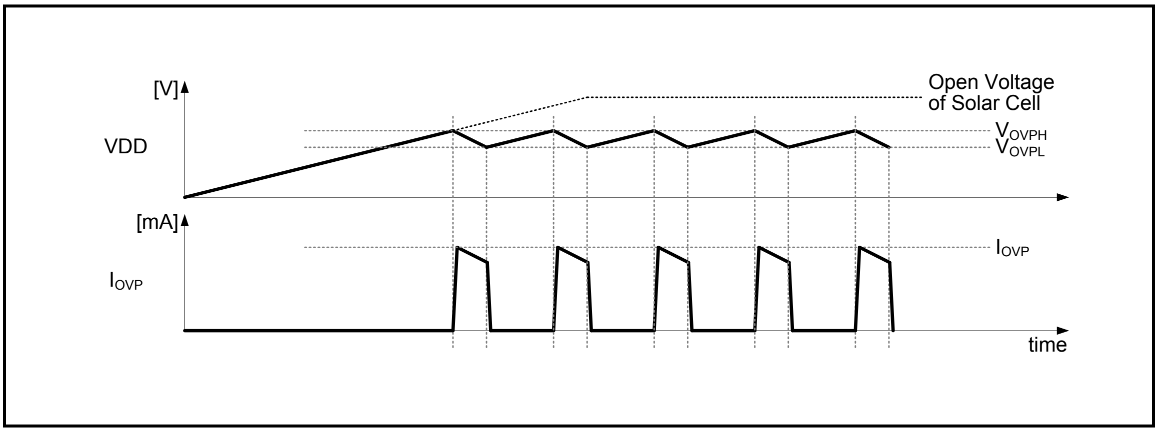
When SW1 disconnects the VSTORE1 and VOUT1 path, the discharge circuit is activated between the VOUT1 pin and GND. The power of the VOUT1 pin is discharged to the GND level.

10.4 Over Voltage Protection (OVP Block)

This IC includes an input overvoltage protection (OVP) function for the VDD pin voltage.

When the VDD pin voltage reaches the OVP detection voltage (V_{OVPH}=5.4V) or higher, the OVP current (IOVP) from the VDD pin is drawn in for limiting the increase in the VDD pin voltage for preventing damage to the IC. Also, when the OVP release voltage (V_{OVPL}=5.3V) or less is reached, drawing-in of the OVP current is stopped.

Figure 10-6 OVP Operation



11. Application Circuit Example and Parts list

Figure 11-1 Application Circuit Example

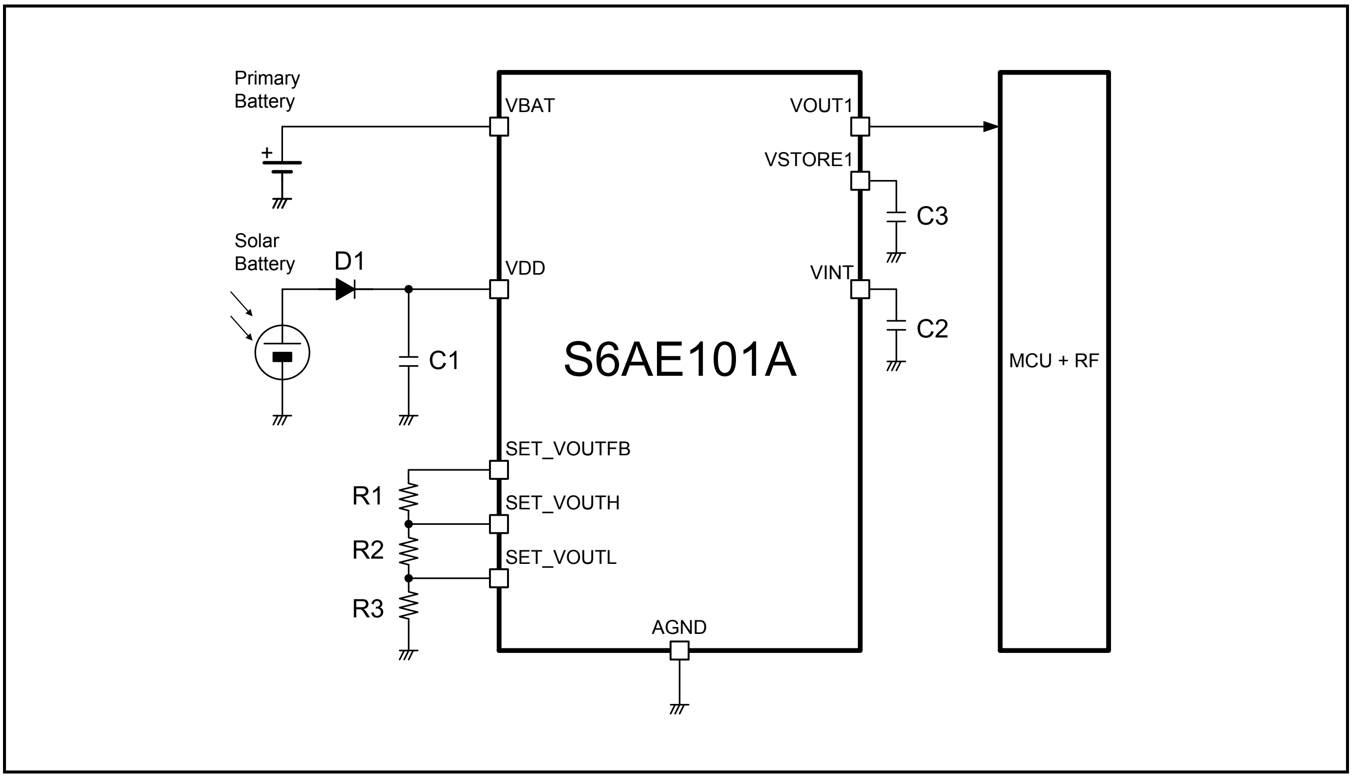


Table 11-1 Parts List

Part number	Item	Specification	Remarks
C1	Ceramic capacitor	10 μF	–
C2	Ceramic capacitor	1 μF	–
C3	Ceramic capacitor	100 μF	–
R1	Resistor	33 MΩ (*1)	–
R2	Resistor	12 MΩ (*1)	–
R3	Resistor	47 MΩ (*1)	–
D1	Diode	–	–

*1: Setting of VOUT maximum voltage: $V_{VOUTH} \fallingdotseq 3.3V$, VOUT minimum voltage: $V_{VOUTL} \fallingdotseq 2.6V$.

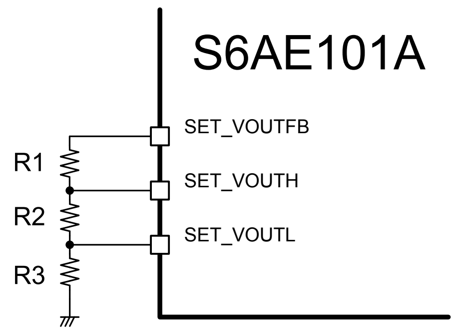
12. Application Note

12.1 Setting the Operation Conditions

1. Setting of output voltage (VOUT1)

The resistor connecting the SET_VOUTH pin and SET_VOUTL pin can be changed to set the VOUT1 output voltage of this IC. This is because the VOUT maximum voltage (V_{VOUTH}) and VOUT minimum voltage (V_{VOUTL}) are set based on the connected resistance. The SET_VOUTFB pin outputs a reference voltage for setting the VOUT maximum voltage and VOUT minimum voltage. Resistor voltage division can be performed on this reference voltage outside the IC for creating a voltage applied to the SET_VOUTH pin and SET_VOUTL pin.

Figure 12-1 Setting of output voltage (VOUT1)



The VOUT maximum voltage (V_{VOUTH}) and VOUT minimum voltage (V_{VOUTL}) can be calculated using the formulas below.

VOUT maximum voltage

$$V_{VOUTH}[V] = \frac{57.5 \times (R2 + R3)}{11.1 \times (R1 + R2 + R3)}$$

VOUT minimum voltage

$$V_{VOUTL}[V] = \frac{57.5 \times R3}{11.1 \times (R1 + R2 + R3)}$$

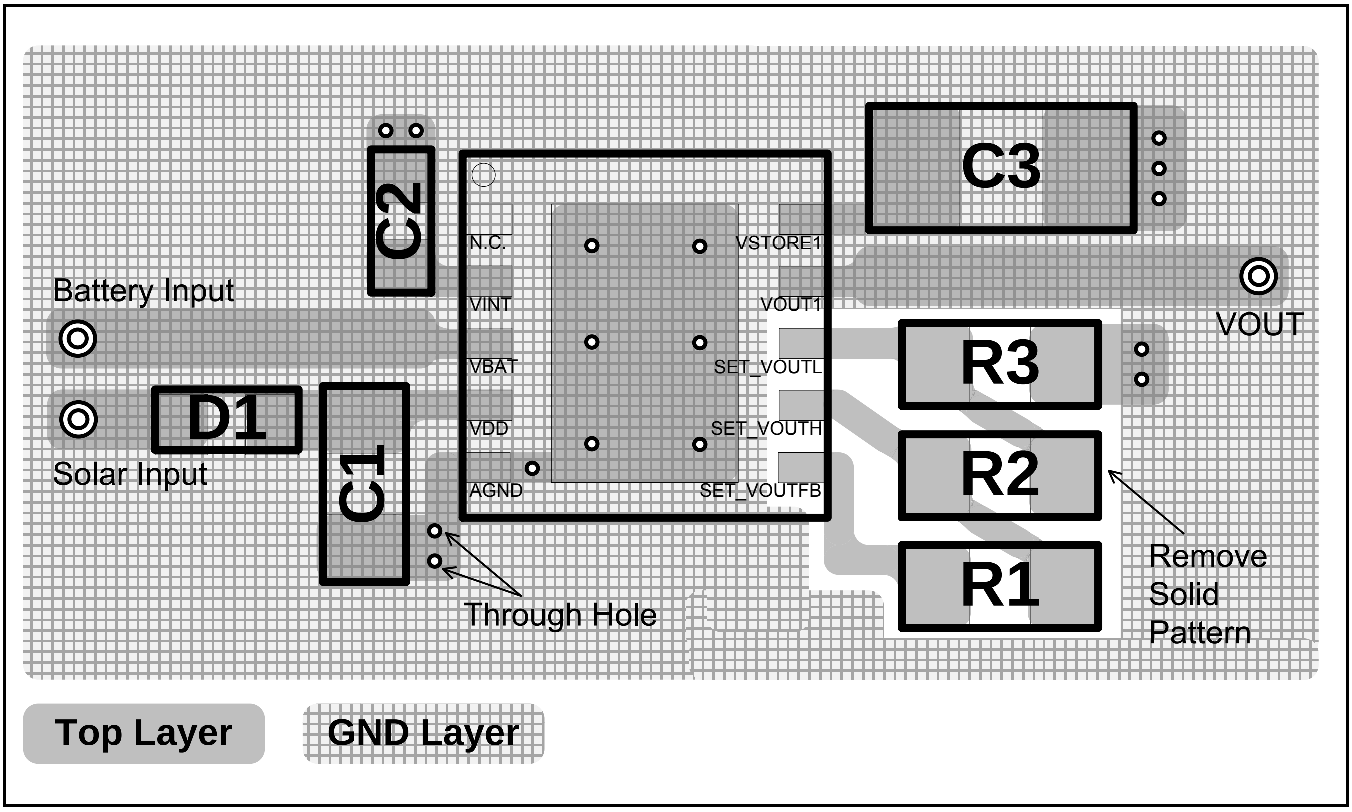
The characteristics when the total for R1, R2, and R3 is 10 MΩ or more (consumption current 1 is 100 MΩ or more) are shown in "9. Electrical Characteristics".

12.2 PCB Layout

Take into account the following points when designing the layout.

- Try to route the wiring for the diode (D1) and input capacitor (C1) for connecting the solar cell on the top layer as much as possible, and avoid implementing a connection using a through hole.
- For the AGND pin of S6AE101A, provide a through hole nearby, and connect it to the GND plane.
- Locate the capacitor (C2) for the internal power as near as possible to the VINT pin.
- Locate the resistors (R1, R2, R3) for setting the output voltage in a grid-type configuration with small loops, and locate them as near as possible to each pin (SET_VOUTFB, SET_VOUTH, SET_VOUTL). Also, removing the GND plane under the parts can be effective in preventing malfunctions due to the leakage current.
- To prevent a leakage current, locate and route the storage capacitor (C3) as far as possible from patterns that are different from the electrical potential of VSTORE1 (such as the GND line). Generally, the insulation resistor of printed circuit boards is extremely high, and normally, the passing of leakage current through the board does not pose a problem. However, in certain rare cases, the surface of the board may have a low insulation resistance, and when using these boards, a leakage current that cannot be ignored may occur.

Figure 12-2 PCB Layout Example



13. Usage Precaution

Printed circuit board ground lines should be set up with consideration for common impedance.

Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti−static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

Do not apply negative voltages.

The use of negative voltages below −0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

14. RoHS Compliance Information

This product has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

15. Ordering Information

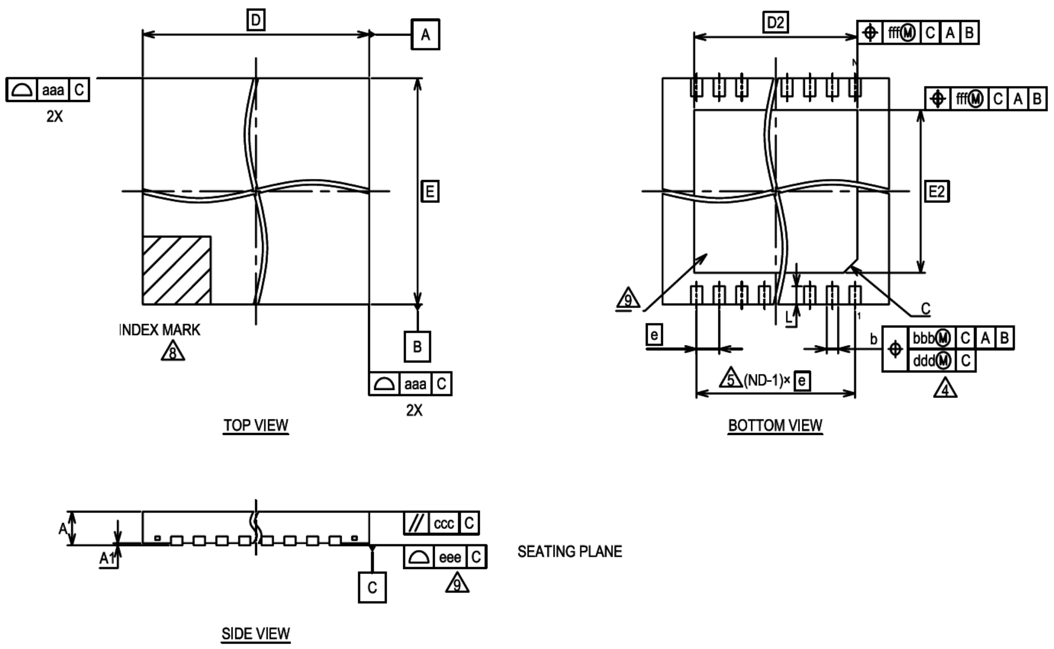
Part number	Package
S6AE101A0DENAB000(*1)	10-pin plastic SON (0.5mm pitch) (VNE010)
S6AE101A0DGNAB000(*2)	

*1: Engineering Sample (ES)

*2: Commercial Sample (CS)

16. Package Dimensions

ULTRA THIN SMALL OUTLINE NO LEAD PACKAGES (VNE010)



PACKAGE	VNE010			NOTE
SYMBOL	MIN.	NOM.	MAX.	
A	—	—	0.90	PROFILE
A_1	0.00	—	0.05	TERMINAL HEIGHT
D	3.00 BSC.			BODY SIZE
E	3.00 BSC.			BODY SIZE
b	0.20	0.25	0.30	TERMINAL WIDTH
D_2	2.20 BSC.			EXPOSED PAD SIZE
E_2	1.60 BSC.			EXPOSED PAD SIZE
e	0.50 BSC.			TERMINAL PITCH
N	10			TERMINAL COUNT
L	0.30	0.40	0.50	TERMINAL LENGTH
C	C0.50			EXPOSED PAD CHAMFER
aaa	0.2			
bbb	0.05			
ccc	-			
ddd	-			
eee	0.05			COPLANARITY
fff	-			

1. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

17. Major Changes

Page	Section	Change Results
Preliminary 0.1		
-	-	Initial release

Colophon

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for any use that includes fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for any use where chance of failure is intolerable (i.e., submersible repeater and artificial satellite). Please note that Cypress will not be liable to you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products. Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions. If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the US Export Administration Regulations or the applicable laws of any other country, the prior authorization by the respective government entity will be required for export of those products.

Trademarks and Notice

The contents of this document are subject to change without notice. This document may contain information on a Cypress product under development by Cypress. Cypress reserves the right to change or discontinue work on any product without notice. The information in this document is provided as is without warranty or guarantee of any kind as to its accuracy, completeness, operability, fitness for particular purpose, merchantability, non-infringement of third-party rights, or any other warranty, express, implied, or statutory. Cypress assumes no liability for any damages of any kind arising out of the use of the information in this document.