WM8594

24-bit 192kHz 2Vrms Multi-Channel CODEC

DESCRIPTION

The WM8594 is a high performance multi-channel audio CODEC with flexible input/output selection and digital and analogue volume control. Features include a 24-bit stereo ADC with digital gain control, two 24-bit DACs with independent volume control and clocking, and a range of input/output channel selection options with analogue volume control for flexible routing within current and future audio systems.

The WM8594 has a five stereo input selector which accepts input levels up to 2Vrms. One stereo input can be routed to the ADC. All inputs can be routed to an output selector.

The WM8594 outputs three stereo audio channels at line levels up to 2Vrms, which can be selected from any of the analogue inputs and DAC outputs. Additionally, one stereo output is available with a headphone driver. The DAC channels include independent digital volume control, and all three stereo output channels include analogue volume control with soft ramp.

The WM8594 supports up to 2Vrms analogue inputs, 2Vrms outputs, with sampling rates from 32kHz to 192kHz for the DACs, and 32kHz to 96kHz for the ADC.

The WM8594 is controlled via a serial interface with support for 2-wire and 3-wire control with full readback. Control of mute, powerdown and reset can also be achieved by pin selection.

The WM8594 is ideal for audio applications requiring high performance and flexible routing options, including flat panel digital TV and DVD recorder.

The WM8594 is available in a 48-lead TQFP package.

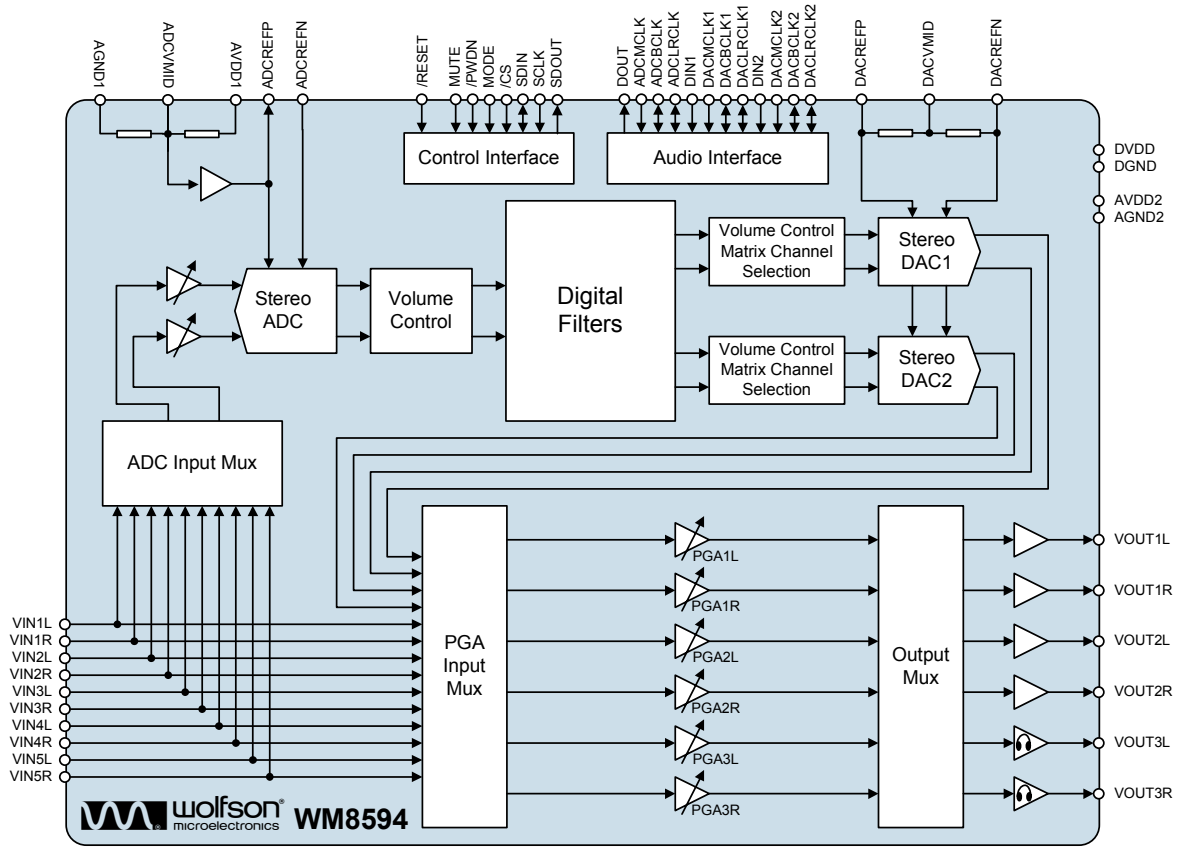
FEATURES

- Multi-channel CODEC with 5 stereo input selector and 3 stereo output selector
- 4-channel DAC, 2-channel ADC
- 5x2Vrms stereo input selector with 3x2 channel analogue bypass to output selector
- 3x2Vrms stereo output selector
- Stereo headphone driver
- Audio performance
  - DAC: 100dB SNR typical ('A' weighted @ 48kHz)
  - DAC: -87dB THD typical
  - ADC: 96dB SNR typical ('A' weighted @ 48kHz)
  - ADC: -80dB THD typical
- Independent sampling rate for ADC and DACs
- Independent sampling rate for DAC1 and DAC2
- DACs sampling frequency 32kHz – 192kHz
- ADC sampling frequency 32kHz – 96kHz
- DAC digital volume control +12dB to -100dB in 0.5dB steps
- ADC digital volume control from +30dB to -97dB in 0.5dB steps
- ADC input analogue boost control, selectable from 0dB, +3dB, +6dB and +12dB
- Output analogue volume control +6dB to -73.5dB in 0.5dB steps with zero cross or soft ramp to prevent pops and clicks
- Headphone drive capability on one stereo output with jack detect
- 2 and 3-wire serial control interface with readback and hardware reset, mute and powerdown pins
- Independent master or slave clocking modes
- Programmable format audio data interface modes
  - I^2S, LJ, RJ, DSP
- 3.3V / 9V analogue, 3.3V digital supply operation
- 48-lead TQFP package

APPLICATIONS

- Digital Flat Panel TV
- DVD-RW

BLOCK DIAGRAM



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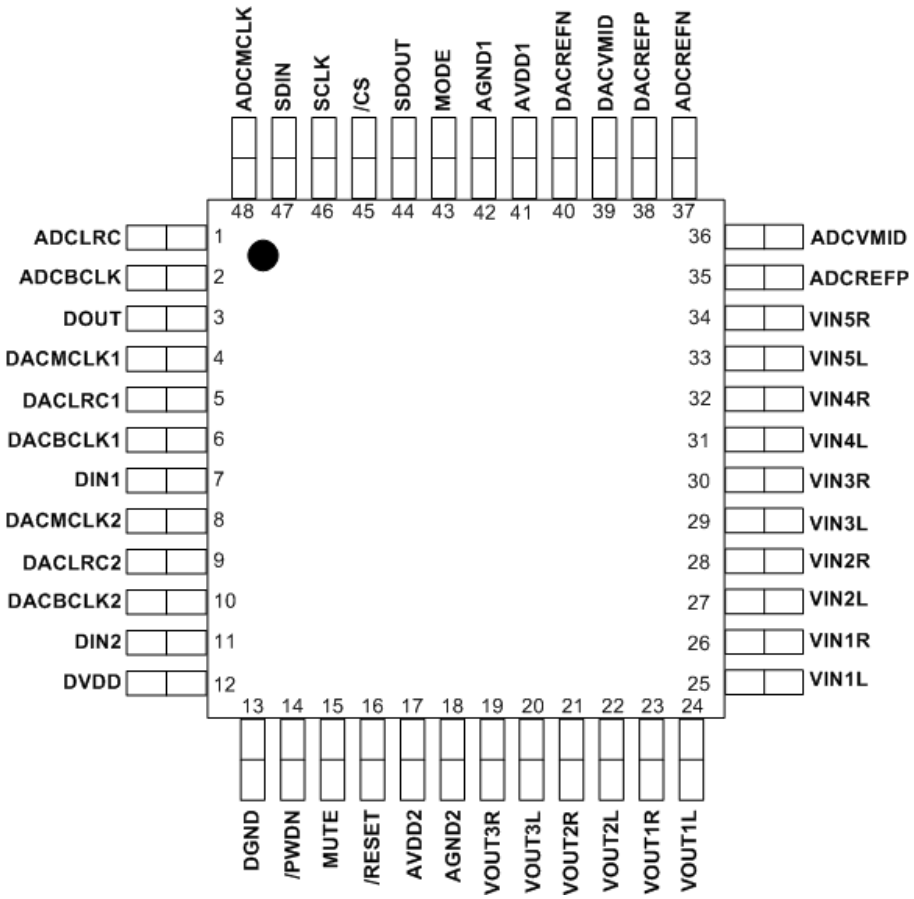
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8594SEFT/V	-40 to +85°C	48-lead TQFP (Pb-free)	MSL3	260˚C
WM8594SEFT/RV	-40 to +85°C	48-lead TQFP (Pb-free, tape and reel)	MSL3	260˚C

Note:

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	ADCLRC	Digital Input/Output	ADC audio interface left/right clock input/output
2	ADCBCLK	Digital Input/Output	ADC audio interface bit clock input/output
3	DOUT	Digital Output	ADC data output
4	DACMCLK1	Digital Input	DAC1 master clock
5	DACLRC1	Digital input	DAC1 audio interface left/right clock input
6	DACBCLK1	Digital Input	DAC1 audio interface bit clock input
7	DIN1	Digital Input	DAC 1 data input
8	DACMCLK2	Digital Input	DAC2 master clock
9	DACLRC2	Digital input	DAC2 audio interface left/right clock input
10	DACBCLK2	Digital Input	DAC2 audio interface bit clock input
11	DIN2	Digital Input	DAC 2 data input
12	DVDD	Supply	Digital supply
13	DGND	Supply	Digital ground
14	/PWDN	Digital Input	Hardware standby mode
15	MUTE	Digital Input	Hardware DAC mute
16	/RESET	Digital Input	Hardware reset
17	AVDD2	Supply	Analogue 9V supply
18	AGND2	Supply	Analogue ground
19	VOUT3R	Analogue Output	Output selector channel 3 right output
20	VOUT3L	Analogue Output	Output selector channel 3 left output
21	VOUT2R	Analogue Output	Output selector channel 2 right output
22	VOUT2L	Analogue Output	Output selector channel 2 left output
23	VOUT1R	Analogue Output	Output selector channel 1 right output
24	VOUT1L	Analogue Output	Output selector channel 1 left output
25	VIN1L	Analogue Input	Input selector channel 1 left input
26	VIN1R	Analogue Input	Input selector channel 1 right input
27	VIN2L	Analogue Input	Input selector channel 2 left input
28	VIN2R	Analogue Input	Input selector channel 2 right input
29	VIN3L	Analogue Input	Input selector channel 3 left input
30	VIN3R	Analogue Input	Input selector channel 3 right input
31	VIN4L	Analogue Input	Input selector channel 4 left input
32	VIN4R	Analogue Input	Input selector channel 4 right input
33	VIN5L	Analogue Input	Input selector channel 5 left input
34	VIN5R	Analogue Input	Input selector channel 5 right input
35	ADCREFP	Analogue Input	Positive reference for ADC
36	ADCVMID	Analogue Output	Midrail divider decoupling pin for ADC
37	ADCREFN	Analogue Input	Ground reference for ADC
38	DACREFP	Analogue Input	Positive reference for DACs
39	DACVMID	Analogue Output	Midrail divider decoupling pin for DACs
40	DACREFN	Analogue Input	Ground reference for DACs
41	AVDD1	Supply	Analogue 3.3V supply
42	AGND1	Supply	Analogue ground
43	MODE	Digital Input	Software mode select (High = 3-wire, Low = 2-wire)
44	SDOUT	Digital Output	Software mode: serial control interface data output
45	/CS	Digital Input	Software mode: serial control interface chip select
46	SCLK	Digital Input	Software mode: serial control interface clock signal
47	SDIN	Digital Input	Software mode: serial control interface data signal
48	ADCMCLK	Digital Input	ADC master clock input

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage, DVDD	-0.3V	+4.5V
Analogue supply voltage, AVDD1	-0.3V	+7V
Analogue supply voltage, AVDD2	-0.3V	+15V
Voltage range digital inputs	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND – 2.4V	AVDD1 + 2.4V
Master Clock Frequency		38.462MHz
Ambient temperature (supplies applied)	-55°C	+125°C
Storage temperature	-65°C	+150°C
Pb free package body temperature (reflow 10 seconds)		+260°C
Package body temperature (soldering 2 minutes)		+183°C

Note:

1. Analogue and digital grounds must always be within 0.3V of each other.

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal resistance – junction to ambient	$R_{\theta JA}$			56.5 See note 1		°C/W

Notes:

1. Figure given for package mounted on 4-layer FR4 according to JESD51-7. (No forced air flow is assumed).
2. Thermal performance figures are estimated.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital power supply	DVDD		2.97	3.3	3.6	V
Analogue power supply	AVDD1		2.97	3.3	3.6	V
Analogue power supply	AVDD2		8.1	9	9.9	V
Ground	DGND/AGND1/ AGND2			0		V
Operating temperature range	T_A		-40		+85	°C

Notes:

1. Digital supply (DVDD) must never be more than 0.3V greater than AVDD1 in normal operation.
2. Digital ground (DGND) and analogue grounds (AGND1, AGND2) must never be more than 0.3V apart.

SUPPLY CURRENT CONSUMPTION

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, T_A=+25˚C, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Record (DACs disabled)						
Digital supply current	I_{DVDD}	fs=48kHz, 256fs Quiescent		8.6		mA
Analogue supply 1 current	I_{AVDD1}			9.2		mA
Analogue supply 2 current	I_{AVDD2}			0.01		mA
DAC Playback (ADC disabled, one DAC disabled)						
Digital supply current	I_{DVDD}	fs=48kHz, 256fs Quiescent		5.5		mA
Analogue supply 1 current	I_{AVDD1}			6.5		mA
Analogue supply 2 current	I_{AVDD2}			2.0		mA
Digital supply current	I_{DVDD}	fs=96kHz, 256fs Quiescent		9.5		mA
Analogue supply 1 current	I_{AVDD1}			7.0		mA
Analogue supply 2 current	I_{AVDD2}			2.0		mA
Digital supply current	I_{DVDD}	fs=192kHz, 256fs Quiescent		10.0		mA
Analogue supply 1 current	I_{AVDD1}			7.0		mA
Analogue supply 2 current	I_{AVDD2}			2.0		mA
ADC Record, DAC Playback (all circuit blocks enabled)						
Digital supply current	I_{DVDD}	fs=48kHz, 256fs Quiescent		17.0		mA
Analogue supply 1 current	I_{AVDD1}			20.0		mA
Analogue supply 2 current	I_{AVDD2}			11.0		mA
Power Down (all circuit blocks disabled)						
Digital supply current	I_{DVDD}	No inputs		160		µA
Analogue supply 1 current	I_{AVDD1}			0.1		µA
Analogue supply 2 current	I_{AVDD2}			0.1		µA

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, TA=+25˚C, 1kHz signal, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital logic levels						
Input low level	V_{IL}				0.3xDVDD	V
Input high level	V_{IH}		0.7xDVDD			V
Output low level	V_{OL}				0.1 x DVDD	V
Output high level	V_{OH}		0.9 x DVDD			V
Digital input leakage current				±0.2		µA
Digital input leakage capacitance				5		pF
Analogue Reference Levels						
ADC Midrail Voltage	ADCVMID			AVDD1/2		V
ADC Buffered Positive Reference Voltage	ADCREFP			ADCVMID		V
DAC Midrail Voltage	DACVMID			DACREFP/2		V
Potential divider resistance		AVDD1 to ADCVMID ADCVMID to AGND1		100		kΩ
		DACVREFP to DACVMID DACVMID to DACVREFN VMID_SEL[1:0] = 01		75 (Note 2)		kΩ
Analogue Line Outputs						
Output signal level (0dB)		R_L = 10kΩ	-10%	2.0x AVDD2 / 9	+10%	Vrms
Maximum capacitance load					11	nF
Minimum resistance load			1			kΩ
Analogue Headphone Outputs						
Output signal level (0dB)		R_L = 32Ω, P_O=20mW		0.8x AVDD2 / 9		Vrms
Minimum resistance load			16			Ω
Analogue Inputs						
Input signal level (0dB)				2.0 x AVDD1/3.3		Vrms
Input impedance			10	12	14	kΩ
Extended input impedance (Note 3)		External resistor = 10kΩ		21		kΩ
Input capacitance				5		pF

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, TA=+25°C, 1kHz signal, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Performance						
Signal to Noise Ratio[1,5]	SNR	A-weighted @ fs = 48kHz	90	100		dB
		A-weighted @ fs = 96kHz		100		dB
		A-weighted @ fs = 192kHz		100		dB
Dynamic Range[2,5]	DNR	A-weighted, -60dB full scale input	90	100		dB
Total Harmonic Distortion[3,5]	THD	1kHz, 0dBFS @ fs = 48kHz		-87	-80	dB
		1kHz, 0dBFS @ fs = 96kHz		-86		dB
		1kHz, 0dBFS @ fs = 192kHz		-85		dB
Channel Separation[4,5]		1kHz		110		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.05		Degree
Power supply rejection ratio	PSRR	1kHz, 100mVpp		50		dB
		20Hz to 20kHz, 100mVpp		45		dB
ADC Performance						
Signal to Noise Ratio[1,5]	SNR	A-weighted, 0dB gain @ fs = 48kHz	85	96		dB
		A-weighted, 0dB gain @ fs = 96kHz		98		dB
Dynamic Range[2,5]	DNR	A-weighted, -60dB full scale input	85	96		dB
Total Harmonic Distortion[3,5]	THD	1kHz, -1dBFS @ fs = 48kHz		-80	-70	dB
		1kHz, -1dBFS @ fs = 96kHz		-78		dB
Channel Separation[4,5]				110		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.05		Degree
Power Supply Rejection Ratio	PSRR			70		dB
				52		dB
Analogue Bypass Paths						
Signal to Noise Ratio[1,5]	SNR	A-weighted		103		dB
Dynamic Range[2,5]	DNR	A-weighted		103		dB
Total Harmonic Distortion[3,5]	THD			90		dB
Channel Separation[4,5]				110		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.05		Degree
Headphone Amplifier						
Output signal level (0dB)		R_L=32Ω P_O=20mW		0.8		Vrms
Signal to Noise Ratio[1,5]	SNR	A-weighted		98		dB
Total Harmonic Distortion	THD	P_O=10mW, R_L=16Ω		-66		dB
		P_O=20mW, R_L=32Ω		-70		dB
Channel Separation[4,5]		1kHz		92		dB
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp		50		dB

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, TA=+25˚C, 1kHz signal, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Volume Control						
ADC minimum digital volume				-97		dB
ADC maximum digital volume				+30		dB
ADC volume step size				0.5		dB
DAC minimum digital volume				-100		dB
DAC maximum digital volume				+12		dB
DAC volume step size				0.5		dB
Analogue Volume Control						
Minimum gain				-73.5		dB
Maximum gain				+6		dB
Step size				0.5		dB
Mute attenuation				120		dB
Crosstalk						
DAC to ADC		1kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB
		20kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB
ADC to DAC		1kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB
		20kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB

TERMINOLOGY

1. Signal-to-noise ratio (dBFS) – SNR is the difference in level between a reference full scale output signal and the device output with no signal applied. This ratio is also called idle channel noise. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dBFS) – DNR is a measure of the difference in level between the highest and lowest components of a signal. Normally a THD measurement at -60dBFS. The measured signal is then corrected by adding 60dB to the result, e.g. THD @ -60dBFS = -30dB, DNR = 90dB.
3. Total Harmonic Distortion (dBFS) – THD is the difference in level between a reference full scale output signal and the first seven odd harmonics of the output signal. To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the next seven odd harmonics is calculated.
4. Channel Separation (dB) – Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
5. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

Notes:

1. All minimum and maximum values are subject to change.
2. This resistance is selectable using VMID_SEL[1:0] – see Figure 52 for full details.
3. See p77 for details of extended input impedance configuration.

MASTER CLOCK TIMING

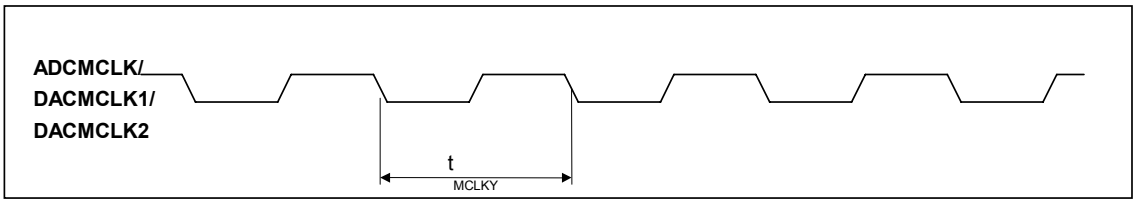


Figure 1 MCLK Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25^{O}C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Master Clock Timing Information					
MCLK System clock cycle time	t_{MCLKY}	27		120	ns
MCLK Duty cycle		40:60		60:40	%
MCLK Period Jitter				200	ps
MCLK Rise/Fall times				10	ns

Table 1 Master Clock Timing Requirements

/RESET TIMING

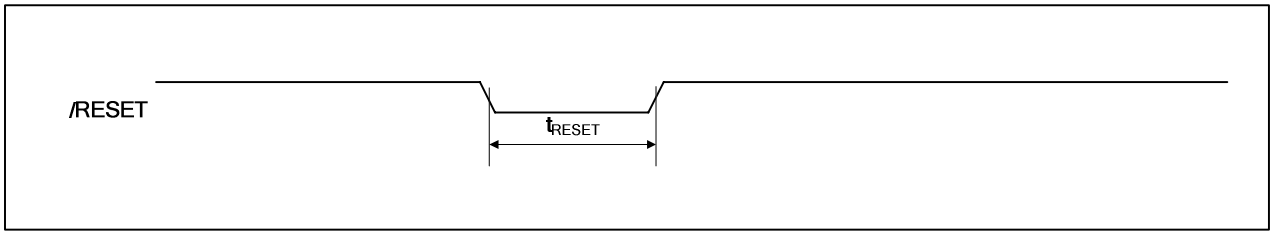


Figure 2 /RESET Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25^{O}C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
/RESET Timing Information					
/RESET pulsewidth low	T_{RESET}	10			ns

Table 2 /RESET Timing Requirements

DIGITAL AUDIO INTERFACE TIMING – SLAVE MODE

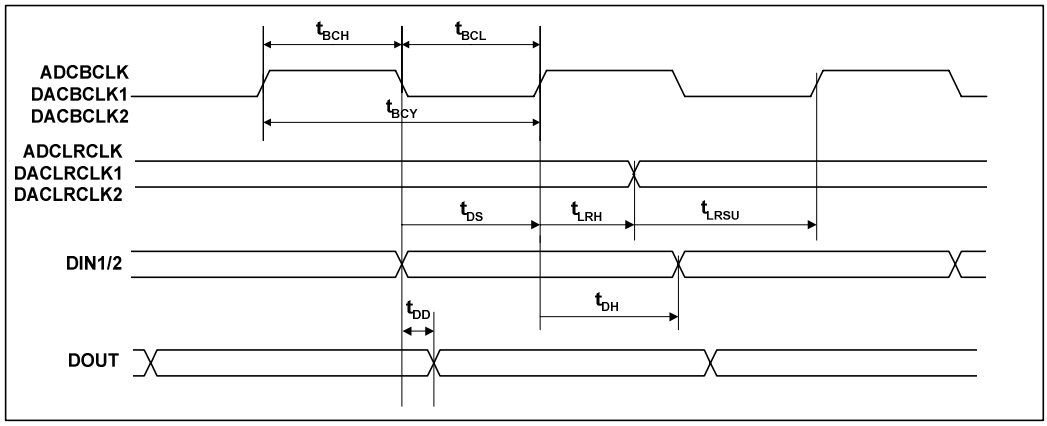


Figure 3 Slave Mode Digital Audio Data Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
ADCBCLK / DACBCLK1 / DACBCLK2 cycle time	t_{BCY}	80			ns
ADCBCLK / DACBCLK1 / DACBCLK2 pulse width high	t_{BCH}	30			ns
ADCBCLK / DACBCLK1 / DACBCLK2 pulse width low	t_{BCL}	30			ns
ADCBCLK / DACBCLK1 / DACBCLK2 rise/fall times				5	ns
ADCLRCLK / DACLRCLK1 / DACLRCLK2 set-up time to ADCBCLK / DACBCLK1 / DACLRCLK2 rising edge	t_{LRSU}	22			ns
ADCLRCLK / DACLRCLK1 / DACLRCLK2 hold time from ADCBCLK / DACBCLK1 / DACBCLK2 rising edge	t_{LRH}	25			ns
ADCLRCLK / DACLRCLK1 / DACLRCLK2 rise/fall times				5	ns
DIN1/2 hold time from DACBCLK1 / DACBCLK2 rising edge	t_{DH}	25			ns
DOUT propagation delay from ADCBCLK falling edge	t_{DD}	4		16	ns

Table 3 Slave Mode Audio Interface Timing

DIGITAL AUDIO INTERFACE TIMING – MASTER MODE

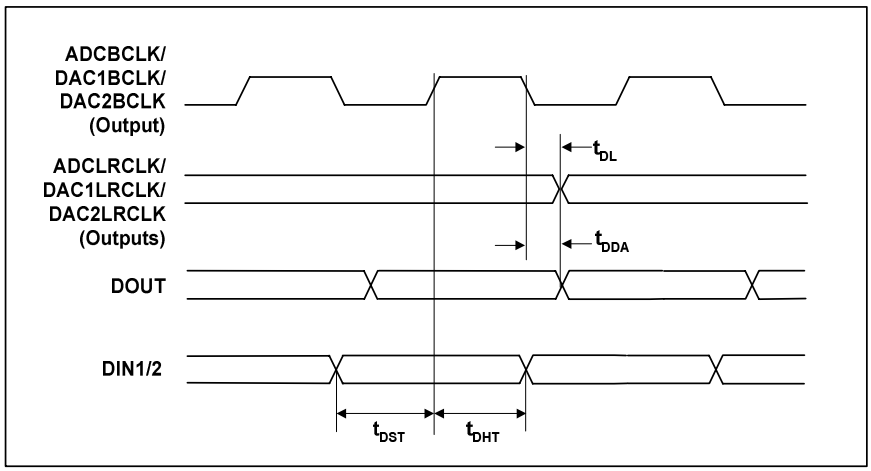


Figure 4 Master Mode Digital Audio Data Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
ADCLRCLK / DACLRCLK1 / DACLRCLK2 propagation delay from ADCBCLK / DACBCLK1 / DACLRCLK2 falling edge	t_{DL}	4		16	ns
DOUT propagation delay from ADCBCLK falling edge	t_{DDA}	4		16	ns
DIN1 / DIN2 setup time to DACBCLK1 / DACBCLK2 rising edge	t_{DST}	22			ns
DIN1 / DIN2 hold time to DACBCLK1 / DACBCLK2 rising edge	t_{DHT}	25			ns

Table 4 Master Mode Audio Interface Timing

CONTROL INTERFACE TIMING – 2-WIRE MODE

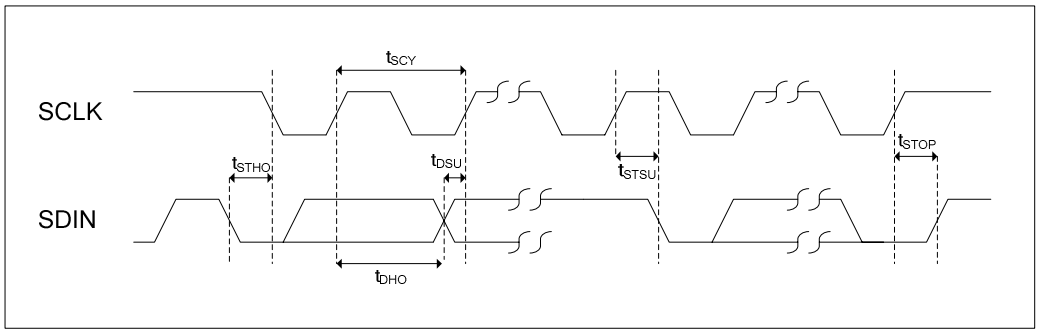


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK pulse cycle time	t_{SCY}	2500			ns
SCLK duty cycle		40/60		60/40	%
SCLK frequency				400	kHz
Hold Time (Start Condition)	t_{STHO}	600			ns
Setup Time (Start Condition)	t_{STSU}	600			ns
Data Setup Time	t_{DSU}	100			ns
SDIN, SCLK Rise Time				300	ns
SDIN, SCLK Fall Time				300	ns
Setup Time (Stop Condition)	t_{STOP}	600			ns
Data Hold Time	t_{DHO}			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 5 Control Interface Timing – 2-Wire Serial Control Mode

CONTROL INTERFACE TIMING – 3-WIRE MODE

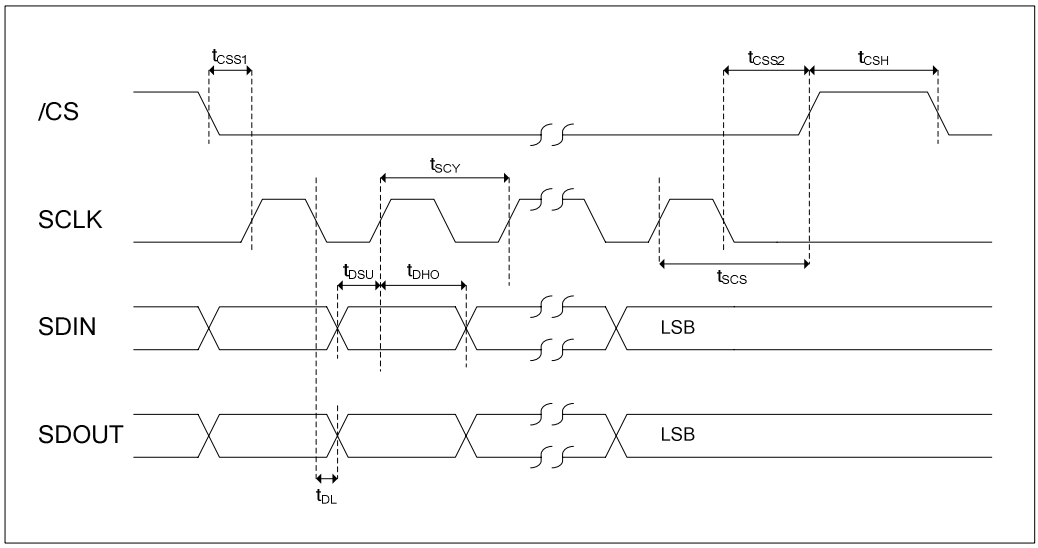


Figure 6 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	160			ns
SCLK duty cycle		40/60		60/40	%
SDIN to SCLK set-up time	t_{DSU}	20			ns
SDIN hold time from SCLK rising edge	t_{DHO}	40			ns
SDOUT propagation delay from SCLK rising edge	t_{DL}			5	ns
/CS pulse width high	t_{CSH}	40			ns
/CS rising/falling to SCLK rising	t_{CSS1}	40			ns
SCLK falling to /CS rising	t_{CSS2}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 6 Control Interface Timing – 3-Wire Serial Control Mode

POWER ON RESET (POR)

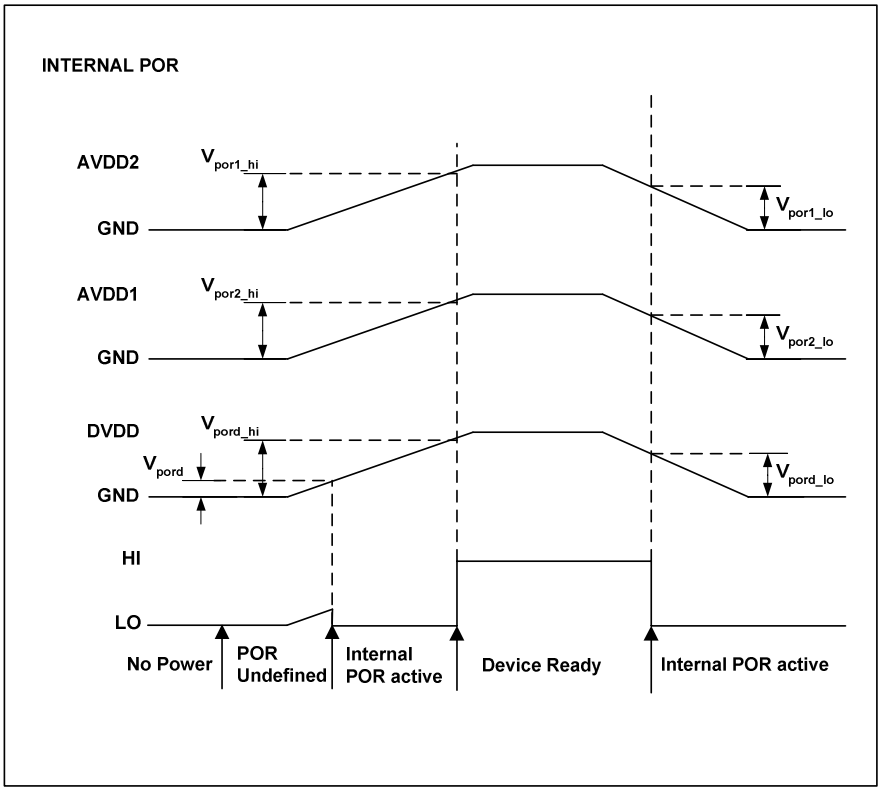


Figure 1 Power Supply Timing Requirements

Test Conditions

DVDD = 3.3V, AVDD1 = 3.3V, AVDD2 = 9V DGND = AGND1 = AGND2 = 0V, T_A = +25°C, T_{A_max} = +125°C, T_{A_min} = -25°C
$AVDD1_{max}$ = $DVDD_{max}$ = 3.63V, $AVDD1_{min}$ = $DVDD_{mim}$= 2.97V, $AVDD2_{max}$ = 9.9V, $AVDD2_{min}$ = 8.1V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
VDD level to POR defined (DVDD rising)	V_{pord}	Measured from DGND	0.27	0.36	0.60	V
VDD level to POR rising edge (DVDD rising)	V_{pord_hi}	Measured from DGND	1.34	1.88	2.32	V
VDD level to POR falling edge (DVDD falling)	V_{pord_lo}	Measured from DGND	1.32	1.86	2.30	V
VDD level to POR rising edge (AVDD1 rising)	V_{por1_hi}	Measured from DGND	1.65	1.68	1.85	V
VDD level to POR falling edge (AVDD1 falling)	V_{por1_lo}	Measured from DGND	1.63	1.65	1.83	V
VDD level to POR rising edge (AVDD2 rising)	V_{por2_hi}	Measured from DGND	1.80	1.86	2.04	V
VDD level to POR falling edge (AVDD2 falling)	V_{por2_lo}	Measured from DGND	1.76	1.8	2.02	V

Table 7 Power on Reset

DEVICE DESCRIPTION

INTRODUCTION

The WM8594 is a high performance multi-channel audio CODEC with 2Vrms line level inputs and outputs and flexible analogue input / output switching. The device comprises a 24-bit stereo ADC, two 24-bit stereo DACs with independent sampling rates and digital volume control, and a flexible analogue input and output multiplexer. Analogue inputs and outputs are all at 2Vrms line level, minimising external component count.

The DACs can operate from independent left/right clocks, bit clocks and master clocks with independent data inputs. Alternatively, the DACs can be synchronised to use the same clocks with independent data inputs. Each of the DAC audio interfaces can be configured to operate in ether master or slave clocking modes. In master mode, left/right clocks and bit clocks are all outputs. In slave mode, left/right clocks and bit clocks are all inputs.

The ADC uses a separate left/right clock, bit clock and master clock, allowing independent recording and playback in audio applications. The ADC audio interface can be configured to operate in either master or slave clocking mode. In master mode, left/right clocks and bit clocks are all outputs. In slave mode, left/right clocks and bit clocks are all inputs.

The ADC includes digital gain control, allowing signals to be gained and attenuated between +30dB and -97dB in 0.5dB steps.

The DACs include independent digital volume control, which is adjustable between +12dB and -100 dB in 0.5dB steps. The DACs can be configured to output stereo audio data and a range of mono audio options.

The input multiplexer accepts five stereo line level inputs at up to 2Vrms. One stereo input can be routed to the ADC, and all five stereo inputs can be routed to the output multiplexer.

The output multiplexer includes analogue volume control with zero cross, adjustable between +6dB and -73.5dB in 0.5dB steps, and configurable soft ramp rate. Analogue audio is output at 2Vrms line level.

Control of the internal functionality of the device is by 2-wire serial control interface with readback. The interface may be asynchronous to the audio data interface as control data will be re-synchronised to the audio processing internally. In addition, control of mute, power-down and reset may also be achieved by pin selection.

Operation using system clocks of 128fs, 192fs, 256fs, 384fs, 512fs, 768fs or 1152fs is provided. ADC and both DACs may be clocked independently. Sampling rates from 32kHz to 192kHz are supported for both DACs provided the appropriate master clocks are input. Sampling rates from 32kHz to 96kHz are supported for the ADC provided the appropriate master clock is input.

The audio data interface supports right justified, left justified, and I^2S interface formats along with a highly flexible DSP serial port interface format.

CONTROL INTERFACE

Control of the WM8594 is achieved by a 2-wire SM-bus-compliant or 3-wire SPI compliant serial interface with readback. Software interface mode is selected using the MODE pin as shown in Table 8 below:

MODE	INTERFACE FORMAT
Low	2 wire
High	3 wire

Table 8 Control Interface Mode Selection

2-WIRE (SM-BUS COMPATIBLE) SERIAL CONTROL INTERFACE MODE

Many devices can be controlled by the same bus, and each device has a unique 7-bit address.

REGISTER WRITE

The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address and read/write bit, MSB first). If the device address received matches the address of the WM8594, the WM8594 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised, the WM8594 returns to the idle condition and waits for a new start condition with valid address.

When the WM8594 has acknowledged a correct address, the controller sends the first byte of control data (B23 to B16, i.e. the WM8594 register address). The WM8594 then acknowledges the first data byte by pulling SDIN low for one SCLK pulse. The controller then sends a second byte of control data (B15 to B8, i.e. the first 8 bits of register data), and the WM8594 acknowledges again by pulling SDIN low for one SCLK pulse. Finally, the controller sends a third byte of control data (B7 to B0, i.e. the final 8 bits of register data), and the WM8594 acknowledges again by pulling SDIN low for one SCLK pulse.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8594 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the WM8594 reverts to the idle condition.

The WM8594 device 2-wire write address is 34h (00110100) or 36h (00110110), selectable by control of /CS.

/CS (PIN 45)	2-WIRE BUS ADDRESS (B[7:1])
0	34h (0011010)
1	36h (0011011)

Table 9 2-Wire Control Interface Bus Address Selection

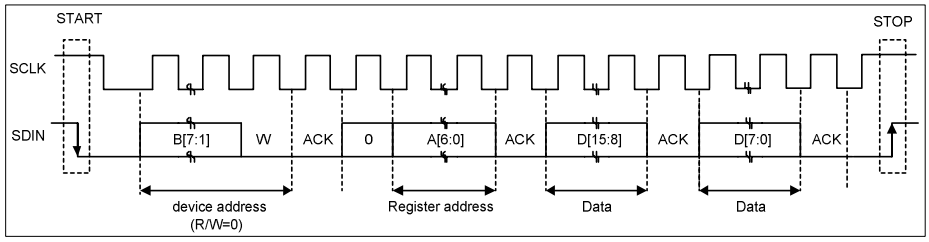


Figure 7 2-Wire Write Protocol

AUTO-INCREMENT REGISTER WRITE

It is possible to write to multiple consecutive registers using the auto-increment feature. When AUTO_INC is set, the register write protocol follows the method shown in Figure 8. As with normal register writes, the controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high, and all devices on the bus receive the device address.

When the WM8594 has acknowledged a correct address, the controller sends the first byte of control data (A6 to A0, i.e. the WM8594 initial register address). The WM8594 then acknowledges the first control data byte by pulling SDIN low for one SCLK pulse. The controller then sends a byte of register data. The WM8594 acknowledges the first byte of register data, auto-increments the register address to be written to, and waits for the next byte of register data. Subsequent bytes of register data can be written to consecutive registers of the WM8594 without setting up the device and register address.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high.

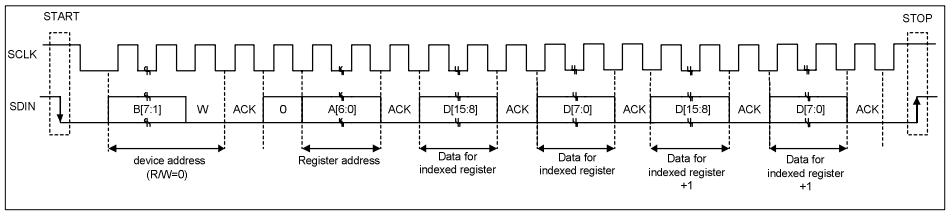


Figure 8 2-Wire Auto-Increment Register Write

REGISTER READBACK

The WM8594 allows readback of all registers with data output on the bidirectional SDIN pin. The protocol is similar to that used to write to the device. The controller will issue the device address followed by a write bit, and the register index will then be passed to the WM8594.

At this point the controller will issue a repeated start condition and resend the device address along with a read bit. The WM8594 will acknowledge this and the WM8594 will become a slave transmitter.

The WM8594 will place the data from the indexed register onto SDIN MSB first. When the controller receives the first byte of data, it acknowledges it. When the controller receives the second and final byte of data it will not acknowledge receipt of the data indicating that it will resume master transmitter control of SDIN. The controller will then issue a stop command completing the read cycle.

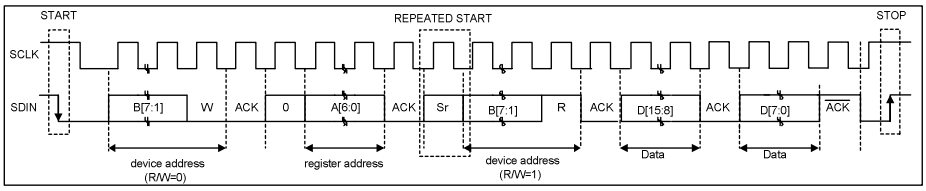


Figure 9 2-wire Read Protocol

AUTO-INCREMENT REGISTER READBACK

It is possible to read from multiple consecutive registers in continuous readback mode. Continuous readback mode is selected by setting AUTO_INC.

In continuous readback mode, the WM8594 will return the indexed register first, followed by consecutive registers in increasing index order until the controller issues a stop sequence.

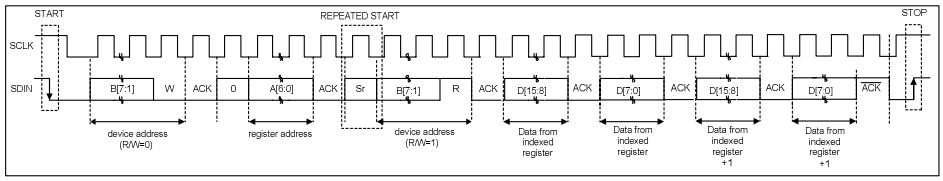


Figure 10 2-Wire Auto-Increment Register Readback

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL INTERFACE MODE

REGISTER WRITE

SDIN is used for the program data, SCLK is used to clock in the program data and /CS is use to latch in the program data. SDIN is sampled on the rising edge of SCLK. The 3-wire interface write protocol is shown in Figure 11.

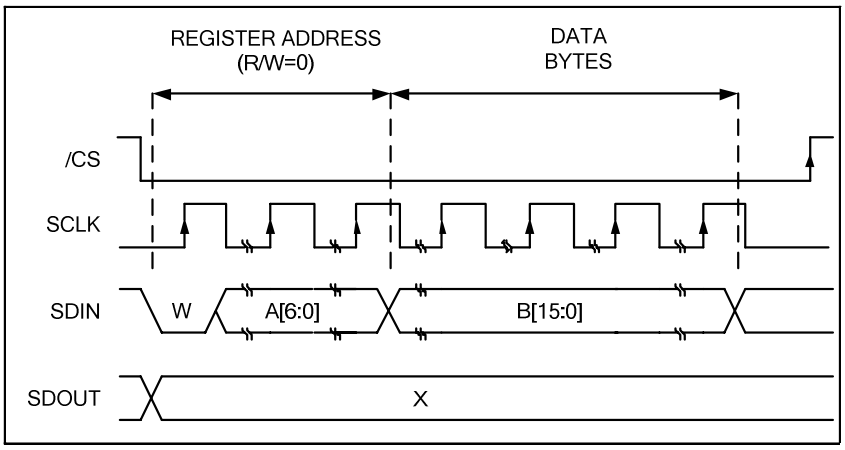


Figure 11 3-Wire Serial Interface Write Protocol

- W indicates write operation.
- A[6:0] is the register index.
- B[15:0] is the data to be written to the register indexed.
- /CS is edge sensitive – the data is latched on the rising edge of /CS.

REGISTER READ-BACK

The read-only status registers can be read back via the SDOUT pin. Read Back is enabled when the R/W bit is high. The data can then be read by writing to the appropriate register address, to which the device will respond with data.

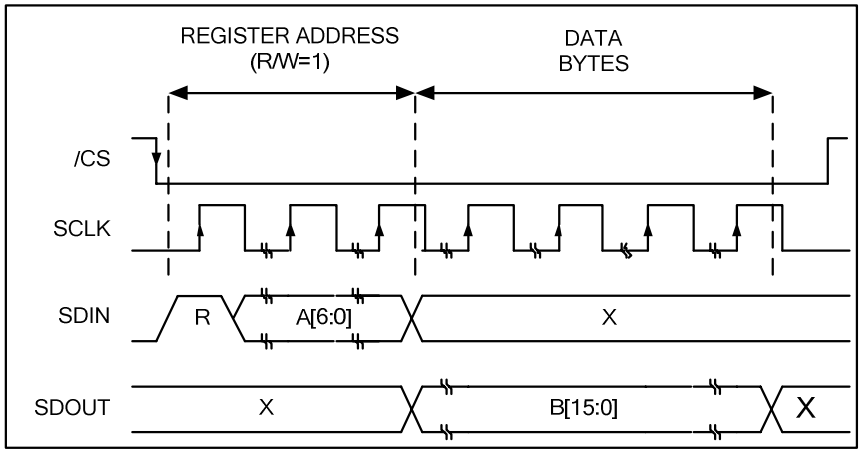


Figure 12 3-Wire Serial Interface Readback Protocol

REGISTER RESET

Any write to register R0 (00h) will reset the WM8594. All register bits are reset to their default values.

DEVICE ID AND REVISION

Reading from register R0 returns the device ID. Reading from register R1 returns the device revision number.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 DEVICE_ID 00h	15:0	DEVICE_ID [15:0]	10000101 10010100	**Device ID** A read of this register will return the device ID, 0x8594.
R1 REVISION 01h	7:0	REVNUM [7:0]	N/A	**Device Revision** A read of this register will return the device revision number. This number is sequentially incremented if the device design is updated.

Table 10 Device ID and Revision Number

DIGITAL AUDIO DATA FORMATS

The WM8594 supports a range of common audio interface formats:

- I^2S
- Left Justified (LJ)
- Right Justified (RJ)
- DSP Mode A
- DSP Mode B

All formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit RJ mode, which is not supported.

Audio data for each stereo channel is time multiplexed with the interface's left/right clock indicating whether the left or right channel is present. The left/right clock is also used as a timing reference to indicate the beginning or end of the data words.

In LJ, RJ and I^2S modes, the minimum number of bit clock periods per left/right clock period is two times the selected word length. The left/right clock must be high for a minimum of bit clock periods equivalent to the word length, and low for the same period. For example, for a word length of 24 bits, the left/right clock must be high for a minimum of 24 bit clock periods and low for a minimum of 24 bit clock periods. Any mark to space ratio is acceptable for the left/right clock provided these requirements are met.

In DSP modes A and B, left and right channels must be time multiplexed and input on DIN1. LRCLK is used as a frame synchronisation signal to identify the MSB of the first input word. The minimum number of bit clock periods per left/right clock period is two times the selected word length. Any mark to space ratio is acceptable for the left/right clock provided the rising edge is correctly positioned.

I2S MODE

In I^2S mode, the MSB of input data is sampled on the second rising edge of bit clock following a left/right clock transition. The MSB of output data changes on the first falling edge of bit clock following a left/right clock transition, and may be sampled on the next rising edge of bit clock. Left/right clocks are low during the left channel audio data samples and high during the right channel audio data samples.

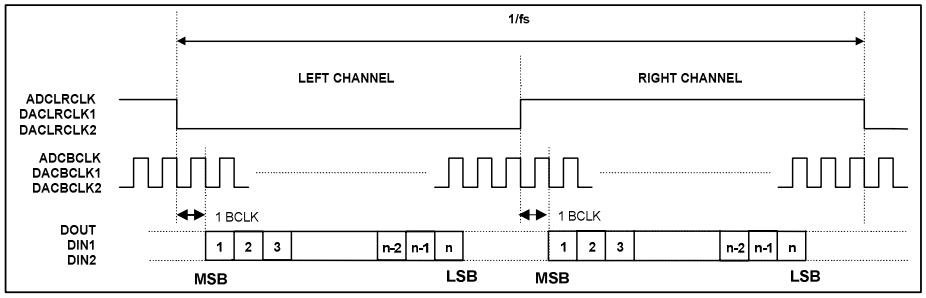


Figure 13 I2S Mode Timing

LEFT JUSTIFIED (LJ) MODE

In LJ mode, the MSB of the input data is sampled by the WM8594 on the first rising edge of bit clock following a left/right clock transition. The MSB of output data changes on the same falling edge of bit clock as left/right clock and may be sampled on the next rising edge of bit clock. Left/right clock is high during the left channel audio data samples and low during the right channel audio data samples.

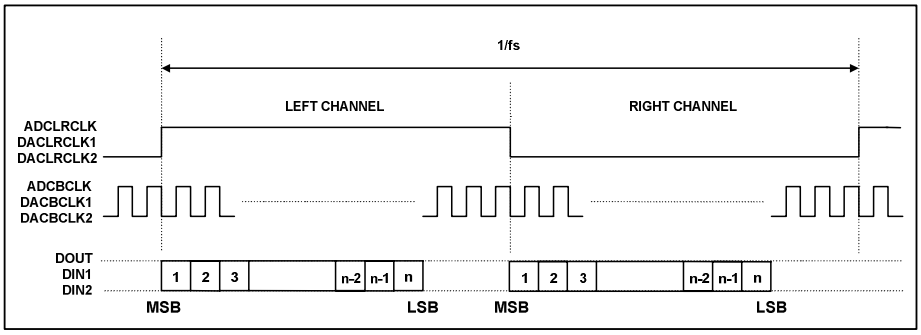


Figure 14 LJ Mode Timing

RIGHT JUSTIFIED (RJ) MODE

In RJ mode the LSB of input data is sampled on the rising edge of bit clock preceding a left/right clock transition. The LSB of output data changes on the falling edge of bit clock preceding a left/right clock transition, and may be sampled on the next rising edge of bit clock. Left/right clock is high during the left channel audio data samples and low during the right channel audio data samples.

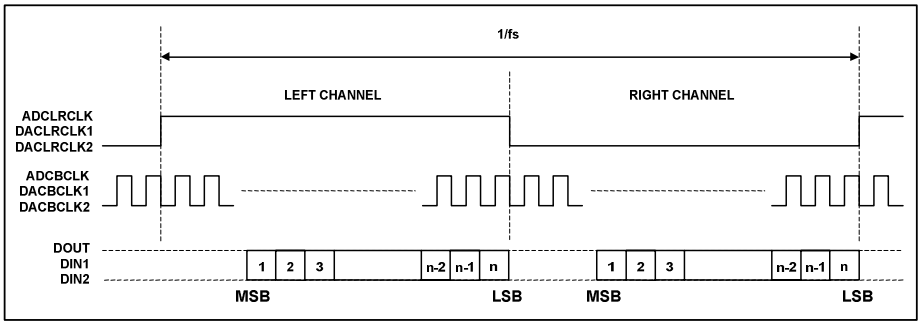


Figure 15 RJ Mode Timing

DSP MODE A

In DSP Mode A, the MSB of channel 1 left data input is sampled on the second rising edge of bit clock following a left/right clock rising edge. Channel 1 right data then follows. The MSB of output data changes on the first falling edge of bit clock following a left/right clock transition and may be sampled on the rising edge of bit clock. The right channel data is contiguous with the left channel data.

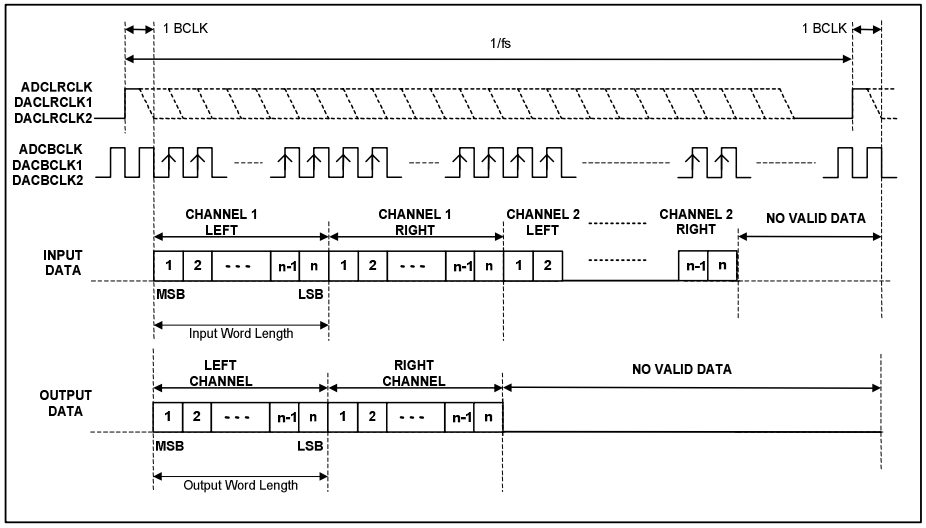


Figure 16 DSP Mode A Timing

DSP MODE B

In DSP Mode B, the MSB of channel 1 left data input is sampled on the first bit clock rising edge following a left/right clock rising edge. Channel 1 right data then follows. The MSB of output data changes on the same falling edge of BCLK as the low to high left/right clock transition and may be sampled on the rising edge of bit clock. The right channel data is contiguous with the left channel data.

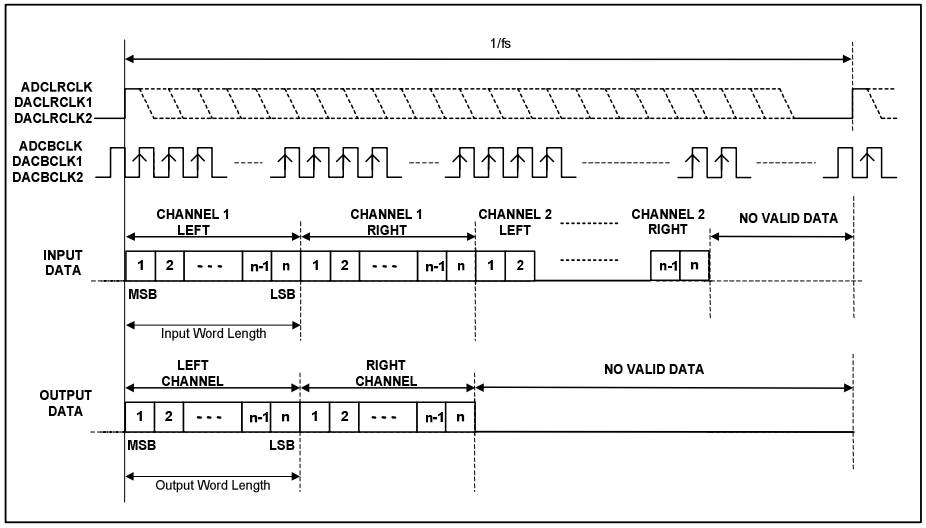


Figure 17 DSP Mode B Timing

DIGITAL AUDIO INTERFACE CONTROL

The control of the audio interface formats is achieved by register write. Dynamically changing the audio data format may cause erroneous operation and is not recommended.

Interface timing is such that the input data and left/right clock are sampled on the rising edge of the interface bit clock. Output data changes on the falling edge of the interface bit clock. By setting the appropriate bit clock and left/tight clock polarity bits, the WM8594 ADC and DACs can sample data on the opposite clock edges.

The control of audio interface formats and clock polarities is summarised in Table 11.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	1:0	DAC1_ FMT[1:0]	10	**DAC1 Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
	3:2	DAC1_ WL[1:0]	10	**DAC1 Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
	4	DAC1_BCP	0	**DAC1 BCLK Polarity** 0 = DACBCLK not inverted - data latched on rising edge of BCLK 1 = DACBCLK inverted - data latched on falling edge of BCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5	DAC1_LRP	0	**DAC1 LRCLK Polarity** 0 = DACLRCLK not inverted 1 = DACLRCLK inverted
R7 DAC2_CTRL1 07h	1:0	DAC2_ FMT[1:0]	10	**DAC2 Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
	3:2	DAC2_ WL[1:0]	10	**DAC2 Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
	4	DAC2_BCP	0	**DAC2 BCLK Polarity** 0 = DACBCLK not inverted - data latched on rising edge of BCLK 1 = DACBCLK inverted - data latched on falling edge of BCLK
	5	DAC2_LRP	0	**DAC2 LRCLK Polarity** 0 = DACLRCLK not inverted 1 = DACLRCLK inverted
R13 ADC_CTRL1 0Dh	1:0	ADC_ FMT[1:0]	10	**ADC Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
	3:2	ADC_ WL[1:0]	10	**ADC Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
	4	ADC_BCP	0	**ADC BCLK Polarity** 0 = ADCBCLK not inverted - data latched on rising edge of BCLK 1 = ADCBCLK inverted - data latched on falling edge of BCLK
	5	ADC_LRP	0	**ADC LRCLK Polarity** 0 = ADCLRCLK not inverted 1 = ADCLRCLK inverted

Table 11 Audio Interface Control

DIGITAL AUDIO INTERFACE

Digital audio data is transferred to and from the WM8594 via the digital audio interface. The DACs have independent data inputs and master clocks, bit clocks and left/right frame clocks, and operate in both master or slave mode. The ADC has independent master clock, bit clock and left/right frame clock in addition to its data output, and can operate in both master and slave modes.

MASTER MODE

The ADC audio interface requires both a left/right frame clock (ADCLRCLK) and a bit clock (ADCBCLK). These can be supplied externally (slave mode) or they can be generated internally (master mode). Selection of master and slave mode is achieved by setting ADC_MSTR in ADC Control Register 15.

The frequency of ADCLRCLK in master mode is dependent upon the ADC master clock frequency and the ADC_SR[2:0] bits.

The frequency of ADCBCLK in master mode can be selected by ADC_BCLKDIV[1:0].

The DAC audio interfaces require both left/right frame clocks (DACLRCLK1, DACLRCLK2) and bit clocks (DACBCLK1, DACBCLK2). These can be supplied externally (slave mode) or they can be generated internally (master mode). Selection of master and slave mode is achieved by setting DAC1_MSTR in DAC1 Control Register 4 and DAC2_MSTR in DAC2 Control Register 9.

The frequency of DACLRCLK1 in master mode is dependent upon the DAC1 master clock frequency and the DAC1_SR[2:0] bits. Similarly the frequency of DACLRCLK2 in master mode is dependent upon the DAC2 master clock frequency and the DAC2_SR[2:0] bits.

The frequency of DACBCLK1 and DACBCLK2 in master mode can be selected by DAC1_BCLKDIV[1:0] and DAC2_BCLKDIV[1:0].

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 DAC1_CTRL2 03h	2:0	DAC1_ SR[2:0]	000	**DAC MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
	5:3	DAC1_ BCLKDIV [2:0]	000	**DAC1 BCLK Rate** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of DAC1_BCLKDIV[2:0] are reserved
R4 DAC1_CTRL3 04h	0	DAC1_ MSTR	0	**DAC1 Master Mode Select** 0 = Slave mode, DACBCLK1 and DACLRCLK1 are inputs to WM8594 1 = Master mode, DACBCLK1 and DACLRCLK1 are outputs from WM8594

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 DAC1_CTRL2 08h	2:0	DAC2_ SR[2:0]	000	**DAC MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
	5:3	DAC2_ BCLKDIV [2:0]	000	**DAC2 BCLK Rate** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of DAC2_BCLKDIV[2:0] are reserved
R9 DAC2_CTRL3 09h	0	DAC2_ MSTR	0	**DAC2 Master Mode Select** 0 = Slave mode, DACBCLK2 and DACLRCLK2 are inputs to WM8594 1 = Master mode, DACBCLK2 and DACLRCLK2 are outputs from WM8594
R14 ADC_CTRL2 0Eh	2:0	ADC_ SR[2:0]	000	**ADC MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = Reserved
	5:3	ADC_BCLK DIV[2:0]	000	**ADC BCLK Rate** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of ADC_BCLKDIV[2:0] are reserved
R15 ADC_CTRL3 0Fh	0	ADC_ MSTR	0	**ADC Master Mode Select** 0 = Slave mode, ADCBCLK and ADCLRCLK are inputs to WM8594 1 = Master mode, ADCBCLK and ADCLRCLK are outputs from WM8594

Table 12 ADC Master Mode Control

SLAVE MODE

In slave mode, the master clock to left/right clock ratio can be auto-detected or set manually by register write.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 DAC1_CTRL2 03h	2:0	DAC1_ SR[2:0]	000	**DAC MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
R8 DAC2_CTRL2 08h	2:0	DAC2_ SR[2:0]	000	
R14 ADC_CTRL2 0Eh	2:0	ADC_ SR[2:0]	000	**ADC MCLK:LRCLK Ratio** 000 = Auto detect 001 = reserved 010 = reserved 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = Reserved

Table 13 Slave Mode MCLK to LRCLK Ratio Control

DIGITAL AUDIO DATA SAMPLING RATES

In a typical digital audio system there is one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's master clock. The WM8594 uses independent master clocks for ADC and DACs. The external master clocks can be applied directly to the ADCMCLK, DACMCLK1 and DACMCLK2 input pins. In a system where there are a number of possible sources for the reference clock, it is recommended that the clock source with the lowest jitter be used for the master clock to optimise the performance of the WM8594.

In slave clocking mode the WM8594 has a master detection circuit that automatically determines the relationship between the master clock frequency (ADCMCLK, DACMCLK1, DACMCLK2) and the sampling rate (ADCLRCLK, DACLRCLK1, DACLRCLK2), to within +/- 32 system clock periods. The master clocks must be synchronised with the left/right clocks, although the device is tolerant of phase variations or jitter on the master clocks.

The ADC supports master clock to sampling clock ratios of 256fs to 768fs and sampling rates of 32kHz to 96kHz, provided the internal signal processing of the ADC is programmed to operate at the correct rate. The DACs support master clock to sampling clock ratios of 128fs to 1152fs and sampling rates of 32kHz to 192kHz, provided the internal signal processing of the DACs is programmed to operate at the correct rate.

Table 14 shows typical master clock frequencies and sampling rates supported by the WM8594 ADC. Table 15 shows typical master clock frequencies and sampling rates supported by the WM8594 DACs.

Sampling Rate (ADCLRCLK)	MASTER CLOCK FREQUENCY (MHZ)			
	256fs	384fs	512fs	768fs
32kHz	8.192	12.288	16.384	24.576
44.1kHz	11.2896	16.9344	22.5792	33.8688
48kHz	12.288	18.432	24.576	36.864
88.2kHz	22.5792	33.8688	Unavailable	Unavailable
96kHz	24.576	Unavailable	Unavailable	Unavailable

Table 14 ADC Master Clock Frequency Versus Sampling Rate

Sampling Rate (DACLRCLK1 DACLRCLK2)	MASTER CLOCK FREQUENCY (MHZ)						
	128fs	192fs	256fs	384fs	512fs	768fs	1152fs
32kHz	Unavailable	Unavailable	8.192	12.288	16.384	24.576	36.864
44.1kHz	Unavailable	8.4672	11.2896	16.9344	22.5792	33.8688	Unavailable
48kHz	Unavailable	9.216	12.288	18.432	24.576	36.864	Unavailable
88.2kHz	11.2896	16.9344	22.5792	33.8688	Unavailable	Unavailable	Unavailable
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable	Unavailable
176.4kHz	22.5792	33.8688	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable

Table 15 DAC Master Clock Frequency Versus Sampling Rate

DAC FEATURES

The WM8594 includes two 24-bit DACs with independent clocks and independent data inputs. The DACs include digital volume control with zero cross and soft mute, de-emphasis support, and the capability to select the output channels to be stereo or a range of mono options. The DACs are enabled by writing to DAC1_EN and DAC2_EN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	8	DAC1_EN	0	**DAC1 Enable** 0 = DAC disabled 1 = DAC enabled
R7 DAC2_CTRL1 07h	8	DAC2_EN	0	**DAC2 Enable** 0 = DAC2 disabled 1 = DAC2 enabled

Table 16 DAC Enable Control

DIGITAL VOLUME CONTROL

The WM8594 DACs include independent digital volume control, allowing the digital gain to be adjusted between -100dB and +12dB in 0.5dB steps. All four DAC channels can be controlled independently. Alternatively, global update bits allow the user to write all volume changes before the volume is updated.

Volume control includes optional zero cross functionality. When zero cross is enabled, volume changes are not applied until the output level crosses VMID. Zero cross helps to prevent pop and click noise when changing volume settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 DAC1L_VOL 05h	7:0	DAC1L _VOL[7:0]	11001000	**DAC Digital Volume** 0000 0000 = -100dB 0000 0001 = -99.5dB 0000 0010 = -99dB …0.5dB steps 1100 1000 = 0dB …0.5dB steps 1101 1111 = +11.5dB 111X XXXX = +12dB
R6 DAC1R_VOL 06h	7:0	DAC1R _VOL[7:0]		
R10 DAC2L_VOL 0Ah	7:0	DAC2L _VOL[7:0]		
R11 DAC2R_VOL 0Bh	7:0	DAC2R _VOL[7:0]		
R5 DAC1L_VOL 05h	8	DAC1L_VU	0	**DAC Digital Volume Update** 0 = Latch DAC volume setting into Register Map but do not update volume 1 = Latch DAC volume setting into Register Map and update left and right channels simultaneously
R6 DAC1R_VOL 06h	8	DAC1R_VU		
R10 DAC2L_VOL 0Ah	8	DAC2L_VU		
R11 DAC2R_VOL 0Bh	8	DAC2R_VU		

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	7	DAC1 _ZCEN	1	**DAC Digital Volume Control Zero Cross Enable** 0 = Do not use zero cross 1 = Use zero cross
R7 DAC2_CTRL1 07h	7	DAC2 _ZCEN		

Table 17 DAC Digital Volume Control

SOFTMUTE

A soft mute can be applied to DAC1 and DAC2 independently.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	9	DAC1_ MUTE	0	**DAC Softmute** 0 = Normal operation 1 = Softmute applied
R7 DAC2_CTRL1 07h	9	DAC2_ MUTE	0	

Table 18 DAC Softmute Control

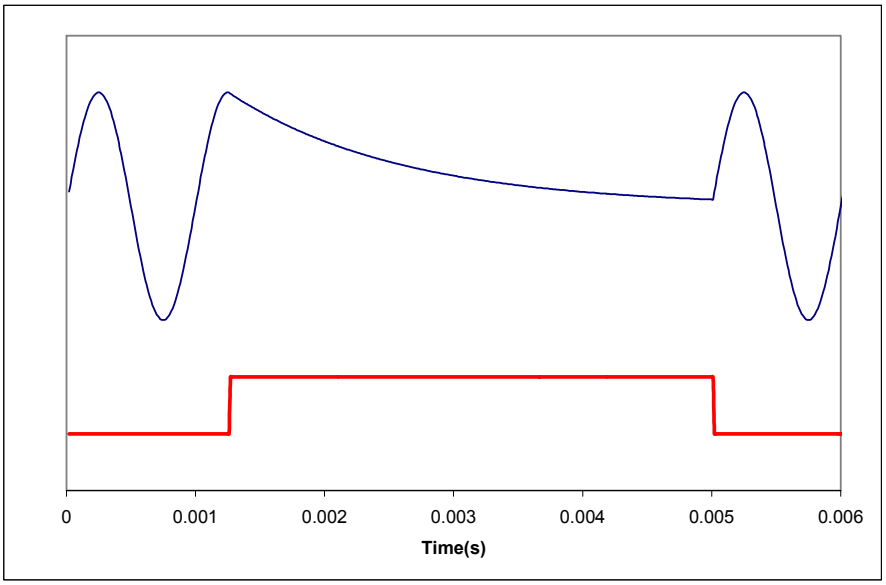


Figure 18 Application and Release of DAC Soft Mute

Figure 18 shows the applications and release of DAC soft mute whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When DACx_MUTE (lower trace) is asserted, the output (upper trace) of the appropriate DAC will decay exponentially from the DC level of the last input sample towards DACVMID with a time constant of approximately 64 input samples. When DACx_MUTE is de-asserted, the output will restart immediately from the current input sample.

DIGITAL MONOMIX CONTROL

Each DAC can be independently set to output a range of mono and stereo options. Each DAC output channel can output left channel data, right channel data or a mix of left and right channel data.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	11:10	DAC1_OP _MUX[1:0]	00	**DAC1 Digital Monomix** 00 = Stereo (Normal Operation) 01 = Mono (Left data to DAC1R) 10 = Mono (Right data to DAC1L) 11 = Digital Monomix, (L+R)/2
R7 DAC2_CTRL1 07h	11:10	DAC2_OP _MUX[1:0]	00	**DAC2 Digital Monomix** 00 = Stereo (Normal Operation) 01 = Mono (Left data to DAC2R) 10 = Mono (Right data to DAC2L) 11 = Digital Monomix, (L+R)/2

Table 19 Digital Monomix Control

DE-EMPHASIS

A digital de-emphasis filter may be applied to the DAC outputs when the sampling frequency is 44.1kHz. The de-emphasis filter for each DAC can be applied independently. The de-emphasis filter responses and error can be seen in Figure 58 to Figure 63.

Note: De-emphasis is not available when MCLK=192fs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	6	DAC1 _DEEMPH	0	**DAC1 De-emphasis** 0 = No de-emphasis 1 = Apply 44.1kHz de-emphasis
R7 DAC2_CTRL1 07h	6	DAC2 _DEEMPH	0	**DAC2 De-emphasis** 0 = No de-emphasis 1 = Apply 44.1kHz de-emphasis

Table 20 De-emphasis Control

SIMULATANEOUS DAC1 AND DAC2 CONTROL

If the same settings are required to both DAC1 and DAC2, it is possible to have the register settings of DAC2 copy the register settings made to DAC1. To use this feature, the user must ensure that DAC2_COPY_DAC1 is set before writes are made to DAC1. Any writes then made to R2-6 are automatically made to R7-11.

Example (When DAC2_COPY_DAC1=1):

REGISTER WRITE	ACTUAL REGISTER SETTING
R2 = 0x0001	R2 = 0x0001 & R7 = 0x0001
R3 = 0x0023	R3 = 0x0023 & R8 = 0x0023
R4 = 0x0045	R4 = 0x0045 & R9 = 0x0045
R5 = 0x0067	R5 = 0x0067 & R10 = 0x0067
R6 = 0x0089	R6 = 0x0089 & R11 = 0x0089

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 ENABLE 0Bh	1	DAC2_ COPY_ DAC1	0	**DAC2 Configuration Control** 0 = DAC2 settings independent of DAC1 1 = DAC2 settings are the same as DAC1

Table 21 DAC2 Configuration Control

ADC FEATURES

The WM8594 features a stereo 24-bit sigma-delta ADC, digital volume control with zero cross, a selectable high pass filter to remove DC offsets, and support for both master and slave clocking modes.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 ADC_CTRL1 0Dh	6	ADC_EN	0	**ADC Enable** 0 = ADC disabled 1 = ADC enabled

Table 22 ADC Enable Control

DIGITAL VOLUME CONTROL

The ADC digital volume can be adjusted between +30dB and -97dB in 0.5dB steps. Left and right channels can be controlled independently. Volume changes can be applied immediately to each channel, or volume changes can be written to both channels before writing to an update bit in order to change the volume in both channels simultaneously.

Volume control includes optional zero cross functionality. When zero cross is enabled, volume changes are not applied until the output level crosses the DC level of the ADC output. Zero cross helps to prevent pop and click noise when changing volume settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 ADCL_VOL 10h	7:0	ADCL _VOL[7:0]	11000011	**ADC Digital Volume** 0000 0000 = Digital mute 0000 0001 = -97dB 0000 0010 = -96.5dB …0.5dB steps 1100 0011 = 0dB …0.5dB steps 1111 1110 = +29.5dB 1111 1111 = +30dB
R17 ADCR_VOL 11h	7:0	ADCR _VOL[7:0]	11000011	
R16 ADCL_VOL 10h	8	ADCL_VU	0	**ADC Digital Volume Update** 0 = Latch ADC volume setting into Register Map but do not update volume 1 = Latch ADC volume setting into Register Map and update left and right channels simultaneously
R17 ADCR_VOL 11h	8	ADCR_VU	0	
R13 ADC_CTRL1 0Dh	13	ADC_ZC_ EN	1	**ADC Digital Volume Control Zero Cross Enable** 0 = Do not use zero cross, change volume instantly 1 = Use zero cross, change volume when data crosses zero

Table 23 ADC Digital Volume Control

CHANNEL SWAP AND INVERSION

The WM8594 ADC input channels can be inverted and swapped in a number of ways to provide maximum flexibility of input path to the ADC. The default configuration provides stereo output data with the left and right channel data in the left and right channels. It is possible to swap the left and right channels, invert them independently, or select the same data from both channels.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 ADC_CTRL1 0Dh	7	ADC_ LRSWAP	0	**ADC Left/Right Swap** 0 = Normal 1 = Swap left channel data into right channel and vice-versa
	8	ADCR_ INV	0	**ADCL and ADCR Output Signal Inversion** 0 = Output not inverted 1 = Output inverted
	9	ADCL_ INV	0	
	11:10	ADC_ DATA_ SEL[1:0]	00	**ADC Data Output Select** 00 = left data from ADCL, right data from ADCR 01 = left data from ADCL, right data from ADCL 10 = left data from ADCR, right data from ADCR 11 = left data from ADCR, right data from ADCL

Table 24 ADC Channel Swap Control

HIGH PASS FILTER

The WM8594 includes a high pass filter to remove DC offsets. The high pass filter response is shown on page 75. It is possible to disable the high pass filter by writing to ADC_HPD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13 ADC_CTRL1 0Dh	12	ADC_HPD	0	**ADC High Pass Filter Disable** 0 = High pass filter enabled 1 = High pass filter disabled

Table 25 High Pass Filter Disable Control

ANALOGUE ROUTING CONTROL

The WM8594 has a number of analogue paths, allowing flexible routing of a number of analogue input signals and DAC output signals at levels up to 2Vrms. The analogue paths include volume control with zero cross, optional soft ramp and soft mute, and flexible routing of analogue inputs and DAC outputs to analogue outputs.

There are a total of ten (five stereo) analogue input channels and four (two stereo) DAC output channels. Two of the ten input channels can be routed to the ADC. Any six of the 14 total channels can be routed to the analogue outputs.

Figure 19 illustrates the various blocks of the analogue routing paths within the WM8594. The following sections describe the control bits associated with the WM8594 analogue paths. Figure 19 also shows where these control bits take affect on the WM8594.

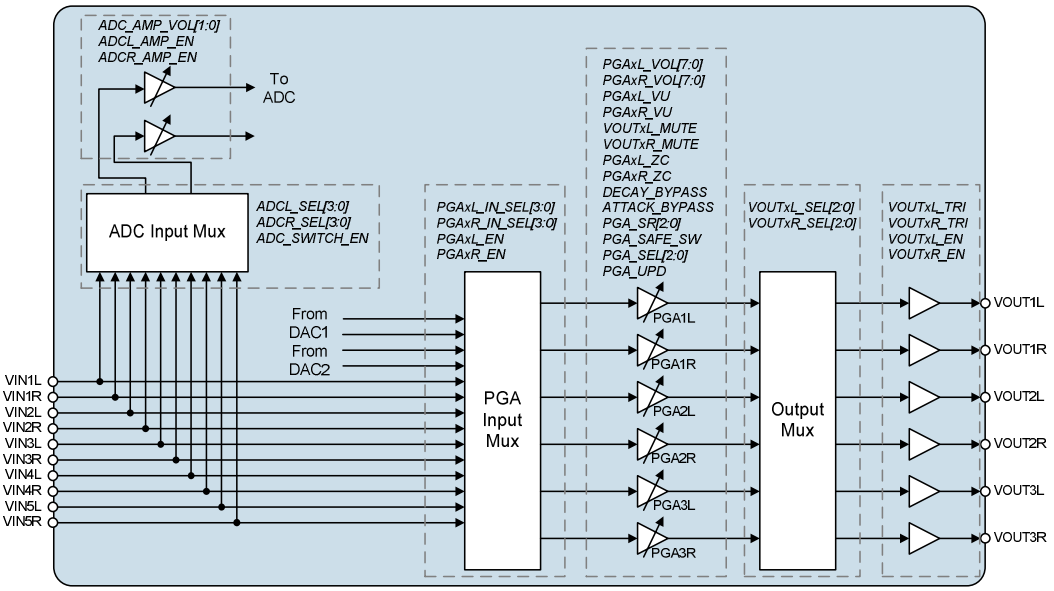


Figure 19 Analogue Routing Paths and Control

ANALOGUE VOLUME CONTROL

Each analogue bypass channel includes analogue volume control. Volume changes can be applied to each channel immediately as they are written. Alternatively, all volume changes can be written, and then all volume changes can be applied simultaneously using the volume update feature.

Volume control includes optional zero cross functionality. When zero cross is enabled, volume changes are not applied until the output level crosses the DC level of the analogue channel (VMID). Zero cross helps to prevent pop and click noise when changing volume settings.

The zero cross function includes a timeout which forces volume changes if a zero cross event does not occur. The timeout period is a maximum of 278ms.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 PGA1L_VOL 13h	7:0	PGA1L_ VOL[7:0]	00001100	**Input PGA Volume** 0000 0000 = +6dB 0000 0001 = +5.5dB …0.5dB steps 00001100 = 0dB … 1001 1111 = -73.5dB 101X XXXX = PGA Mute
R20 PGA1R_VOL 14h	7:0	PGA1R_ VOL[7:0]		
R21 PGA2L_VOL 15h	7:0	PGA2L_ VOL[7:0]		
R22 PGA2R_VOL 16h	7:0	PGA2R_ VOL[7:0]		
R23 PGA3L_VOL 17h	7:0	PGA3L_ VOL[7:0]		
R24 PGA3R_VOL 18h	7:0	PGA3R_ VOL[7:0]		
R19 PGA1L_VOL 13h	8	PGA1L_ VU	0	**Input PGA Volume Update** 0 = Latch corresponding volume setting into Register Map but do not update volume 1 = Latch corresponding volume setting into Register Map and update all channels simultaneously
R20 PGA1R_VOL 14h	8	PGA1R_ VU		
R21 PGA2L_VOL 15h	8	PGA2L_ VU		
R22 PGA2R_VOL 16h	8	PGA2R_ VU		
R23 PGA3L_VOL 17h	8	PGA3L_ VU		
R24 PGA3R_VOL 18h	8	PGA3R_ VU		
R25 PGA_CTRL1 19h	2	PGA1L_ ZC	0	**PGA Gain Zero Cross Enable** 0 = PGA gain updates occur immediately 1 = PGA gain updates occur on zero cross
	3	PGA1R_ ZC		
	4	PGA1L_ ZC		
	5	PGA1R_ ZC		
	6	PGA1L_ ZC		
	7	PGA1R_ ZC		

Table 26 Analogue Volume Control

VOLUME RAMP

Analogue volume can be adjusted by step change or by soft ramp. The ramp rate is dependent upon the sampling rate. The sampling rate upon which the volume ramp rate is based can be selected between the DAC sampling rate or the ADC sampling rate in either slave mode or master mode. The ramp rates for common audio sample rates are shown in Table 27:

SAMPLE RATE FOR PGA (kHz)	DIVIDE BY	PGA Ramp Rate (ms/dB)
32	8	0.50
44.1	8	0.36
48	8	0.33
88.2	16	0.36
96	16	0.33
176.4	32	0.36
192	32	0.33

Table 27 Analogue Volume Ramp Rate

For example, when using a sample rate of 48kHz, the time taken for a volume change from and initial setting of 0dB to -20dB is calculated as follows:

Volume Change (dB) x PGA Ramp Rate (ms/dB) = 20 x 0.33 = 6.6ms

When changing from one PGA ramp clock source to another, it is recommended that PGA_SAFE_SW is set to 0. This forces the clock switch over to occur at a point where all relevant clock signals are zero, ensuring glitch-free operation. This process can take up to 32 left/right clock cycles.

If a faster change in PGA ramp rate clock source is required, PGA_SAFE_SW can be set to 1. This forces the change in clock source to occur immediately regardless of the state of the relevant clock signals internally. Glitch-free operation is not guaranteed under these conditions.

If the volume ramp function is not required when increasing or decreasing volume, this block can be bypassed by setting ATTACK_BYPASS or DECAY_BYPASS to 1. Figure 20 shows the effect of these register settings:

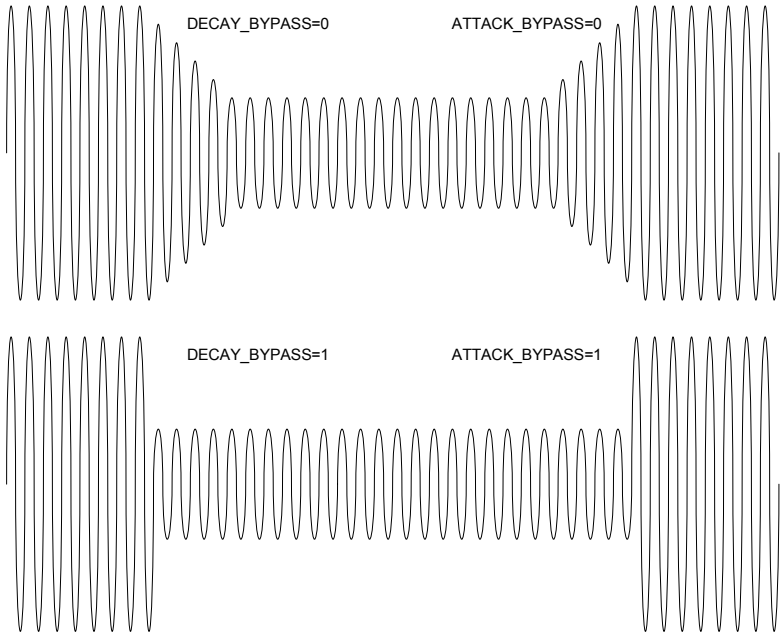


Figure 20 ATTACK_BYPASS and DECAY_BYPASS functionality

Note: When ATTACK_BYPASS=1 or DECAY_BYPASS=1, it is recommended that the zero cross function for the PGA is used to eliminate click noise when changing volume settings.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 PGA_CTRL1 19h	0	DECAY_ BYPASS	0	**PGA Gain Decay Mode** 0 = PGA gain will ramp down 1 = PGA gain will step down
	1	ATTACK_ BYPASS	0	**PGA Gain Attack Mode** 0 = PGA gain will ramp up 1 = PGA gain will step up
R27 ADD_CTRL1 1Bh	6:4	PGA_ SR[2:0]	001	**Sample Rate for PGA** 000 = 32kHz 001 = 44.1kHz 010 = 48kHz 011 = 88.2kHz 100 = 96kHz 101 = 176.4kHz 11X = 192kHz See Table 27 for further information on PGA sample rate versus volume ramp rate.
R36 PGA_CTRL3 24h	0	PGA_ SAFE_SW	0	**PGA Ramp Control Clock Source Mux Force Update** 0 = Wait until clocks are safe before switching PGA clock source 1 = Force PGA clock source to change immediately
	3:1	PGA_ SEL[2:0]	000	**PGA Ramp Control Clock Source** 000 = ADCLRCLK 001 = DACLRCLK1 010 = DACLRCLK2 011 = reserved 100 = reserved 101 = DACLRCLK1 (when DAC1 is being used in master mode) 110 = DACLRCLK2 (when DAC2 is being used in master mode) 111 = ADCLRCLK (when ADC is being used in master mode)
	10	PGA_UPD	0	**PGA Ramp Control Clock Source Mux Update** 0 = Do not update PGA clock source 1 = Update clock source

Table 28 Analogue Volume Ramp Control

ANALOGUE MUTE CONTROL

The analogue channel PGAs can be muted independently and are muted by default. Alternatively, all mute bits can be set using a master mute bit, MUTE_ALL.

Setting one of these mute bits is equivalent to setting the relevant PGAxx_VOL[7:0] register bits to mute as defined in Table 26.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 PGA_CTRL2 1Ah	0	MUTE_ ALL	0	**Master PGA Mute Control** 0 = Unmute all PGAs 1 = Mute all PGAs
	1	PGA1L_ MUTE	1	**Individual PGA Mute Control** 0 = Unmute PGA 1 = Mute PGA
	2	PGA1R_ MUTE	1	
	3	PGA2L_ MUTE	1	
	4	PGA2R_ MUTE	1	
	5	PGA3L_ MUTE	1	
	6	PGA3R_ MUTE	1	

Table 29 Analogue Mute Control

INPUT SELECTOR CONTROL

Each left channel input PGA can select between all left channel analogue inputs, and both left and right DAC inputs. Each right channel input PGA can select between all right channel analogue inputs, and both left and right DAC inputs. All PGAs can be enabled and disabled independently.

Note: It is recommended to mute the PGA before changing the input to the PGA to avoid pop/click noises when selecting a different input source.

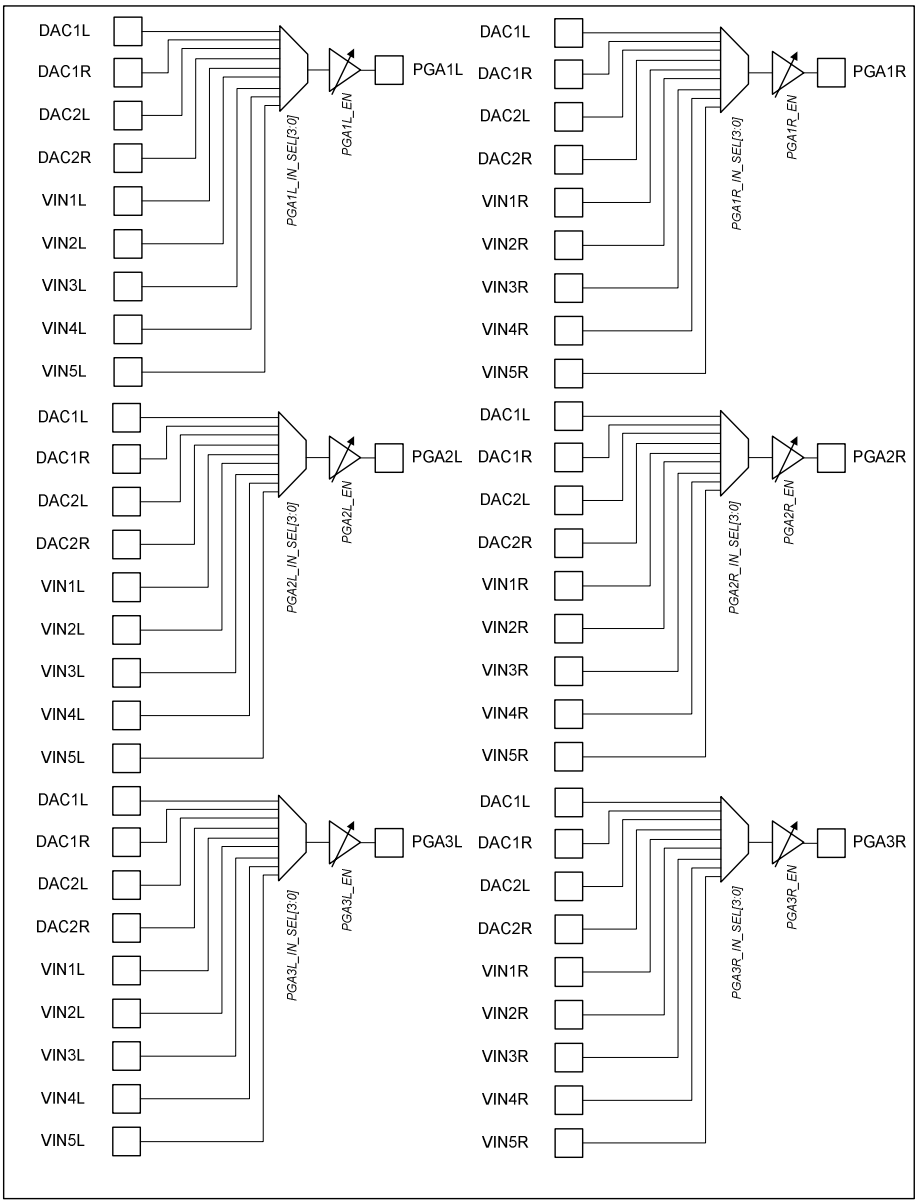


Figure 21 Input Selector Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 INPUT_CTRL1 1Ch	3:0	PGA1L_IN_SEL[3:0]	0000	**Left Input PGA Source Selection** 0000 = No input selected 0001 = VIN1L selected 0010 = VIN2L selected 0011 = VIN3L selected 0100 = VIN4L selected 0101 = VIN5L selected 0110 to 1000 = reserved 1001 = DAC1L output selected 1010 = DAC1R output selected 1011 = DAC2L output selected 1100 = DAC2R output selected 1101 to 1111 = reserved
	11:8	PGA2L_IN_SEL[3:0]	0000	
R29 INPUT_CTRL2 1Dh	7:4	PGA3L_IN_SEL[3:0]	0000	
R28 INPUT_CTRL1 1Ch	7:4	PGA1R_IN_SEL[3:0]	0000	**Right Input PGA Source Selection** 0000 = No input selected 0001 = VIN1R selected 0010 = VIN2R selected 0011 = VIN3R selected 0100 = VIN4R selected 0101 = VIN5R selected 0110 to 1000 = reserved 1001 = DAC1L output selected 1010 = DAC1R output selected 1011 = DAC2L output selected 1100 = DAC2R output selected 1101 to 1111 = reserved
R29 INPUT_CTRL2 1Dh	3:0	PGA2R_IN_SEL[3:0]	0000	
	11:8	PGA3R_IN_SEL[3:0]	0000	
R31 INPUT_CTRL4 1Fh	0	PGA1L_EN	0	**Input PGA Enable Controls** 0 = PGA disabled 1 = PGA enabled
	1	PGA1R_EN		
	2	PGA2L_EN		
	3	PGA2R_EN		
	4	PGA3L_EN		
	5	PGA3R_EN		

Table 30 PGA Input Select Control

ADC INPUT SELECTOR CONTROL

The ADC input switch can be configured to allow any combination of two inputs to be input to the ADC. Each input switch channel can be controlled independently.

The input switch also includes PGAs to provide a range of analogue gain settings between -6dB and +6dB prior to the ADC. These PGAs can be enabled and disabled independently.

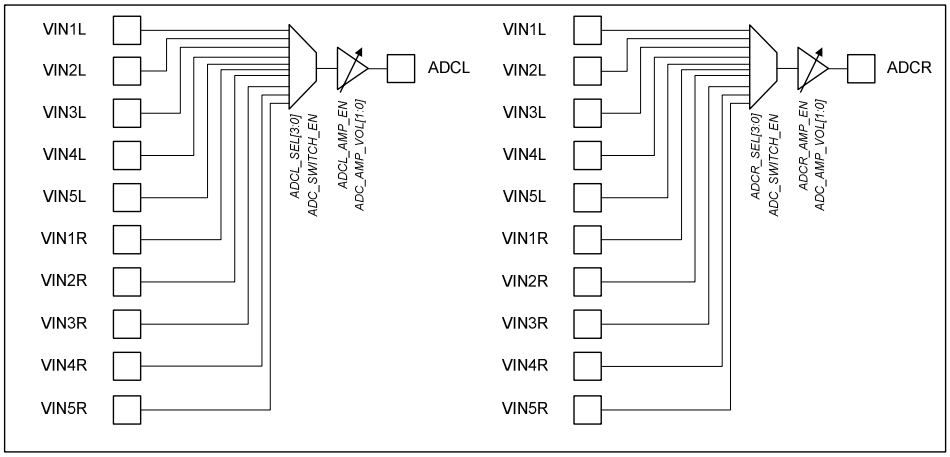


Figure 22 ADC Input Selector Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 INPUT_CTRL3 1Eh	3:0	ADCL_ SEL[3:0]	0000	**ADC Input Select** 0000 = VIN1L 0001 = VIN2L 0010 = VIN3L 0011 = VIN4L 0100 = VIN5L 0101 to 1000 = reserved 1000 = VIN1R 1001 = VIN2R 1010 = VIN3R 1011 = VIN4R 1100 = VIN5R 1101 to 1111 = reserved
	7:4	ADCR_ SEL[4:0]	0000	
	9:8	ADC_AMP _VOL[1:0]	10	**ADC Amplifier Gain Control** 00 = 0dB 01 = +3dB 10 = +6dB 11 = +12dB
	10	ADC_ SWITCH_ EN	0	**ADC Input Switch Control** 0 = ADC input switches open 1 = ADC input switches closed
R31 INPUT_CTRL4 1Fh	6	ADCL_ AMP_EN	0	**ADC Input Amplifier Enable Controls** 0 = Amplifier disabled 1 = Amplifier enabled
	7	ADCR_ AMP_EN	0	

Table 31 ADC Input Switch Control

OUTPUT SELECTOR CONTROL

Any analogue PGA channel can be routed to any analogue output. Care should be taken to ensure that each analogue output is routed to only one analogue input – it is not possible to route multiple inputs to one output through the output selector. All analogue outputs can be independently enabled and disabled. Additionally, all outputs can be tri-stated to allow the output to be connected to applications where ports can either be inputs or outputs.

Note: It is recommended to mute all the outputs before changing the output selector to avoid pop/click noises when selecting a different output source.

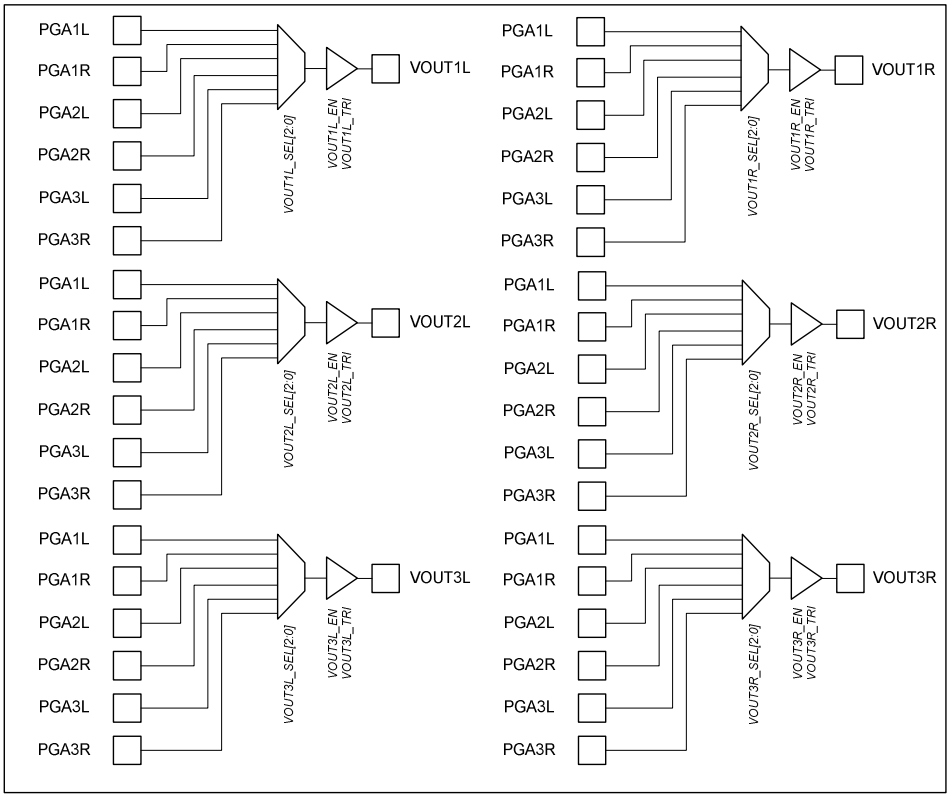


Figure 23 Output Selector Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 OUTPUT_ CTRL1 20h	2:0	VOUT1L_ SEL[2:0]	000	**Output Mux Selection** 000 = PGA1L 001 = PGA1R 010 = PGA2L 011 = PGA2R 100 = PGA3L 101 = PGA3R 11X = Reserved
	5:3	VOUT1R_ SEL[2:0]	001	
	8:6	VOUT2L_ SEL[2:0]	010	
R33 OUTPUT_ CTRL2 21h	2:0	VOUT2R_ SEL[2:0]	011	
	5:3	VOUT3L_ SEL[2:0]	100	
	8:6	VOUT3R_ SEL[2:0]	101	
R34 OUTPUT_ CTRL3 22h	0	VOUT1L_ TRI	0	**Output Amplifier Tristate Control** 0 = Normal operation 1 = Output amplifier tristate enable (Hi-Z)
	1	VOUT1R_ TRI		
	2	VOUT2L_ TRI		
	3	VOUT1R_ TRI		
	4	VOUT3L_ TRI		
	5	VOUT3R_ TRI		
	7	VOUT1L_ EN	0	**Output Amplifier Enables** 0 = Output amplifier disabled 1 = Output amplifier enabled
	8	VOUT1R_ EN		
	9	VOUT2L_ EN		
	10	VOUT2R_ EN		
	11	VOUT3L_ EN		
	12	VOUT3R_ EN		

Table 32 Output Selection

POP AND CLICK PERFORMANCE

The WM8594 includes a number of features designed to minimise pops and clicks in various phases of operation including power up, power down, changing analogue paths and starting/stopping clocks. In order to ensure optimum performance, the following sequences should be followed.

POWERUP SEQUENCE

1. Apply power to the WM8594 (see Power On Reset).
2. Set-up initial internal biases:
   - SOFT_ST=1
   - FAST_EN=1
   - POBCTRL=1
   - BUFIO_EN=1
3. Enable output drivers to allow the AC coupling capacitors at the output stage to be pre-charged to DACVMID:
   - VOUTxL_EN=1
   - VOUTxR_EN=1
4. Enable DACVMID. 750kΩ selected here for optimum pop reduction:
   - VMID_SEL=10
5. Wait until DACVMID has fully charged. The time is dependent on the capacitor values used to AC-couple the outputs and to decouple DACVMID, and the VMID_SEL value chosen. An approximate delay of 6xRCms can be used, where R is the DACVMID resistance and C is the decoupling capacitor on DACVMID. For DACVMID resistance of 50kΩ and C=4.7uF, the delay should be approximately 1.5 seconds.
   - Insert delay
6. Enable the master bias:
   - BIAS_EN=1
7. Switch the output drivers to use the master bias instead of the power up (fast) bias:
   - POBCTRL=0
8. Enable all functions (DACs, ADC, PGAs) required for use. PGAs are muted by default so the write order is not important.
9. Unmute the PGAs and switch DACVMID resistance to 75k for normal operation:
   - PGAxL_MUTE=0
   - PGAxR_MUTE=0
   - VMID_SEL=01

POWERDOWN SEQUENCE

1. Mute all PGAs:
   - MUTE_ALL=1
2. Set up biases for power down mode:
   - FAST_EN=1
   - VMID_SEL=01
   - BIAS_EN=1
   - BUFIO_EN=1
   - VMIDTOG=0
   - SOFT_ST=1
3. Switch outputs to use fast bias instead of master bias:
   - POBCTRL=1
4. Power down all WM8594 functions (ADC, DACs, PGAs etc.). The outputs are muted so the write order is not important.
5. Power down VMID to allow the analogue outputs to ramp gently to ground in a pop-free manner.
   - VMID_SEL=00
6. Wait until DACVMID has fully discharged. The time taken depends on system capacitance.
   - Insert delay
7. Clamp outputs to ground.
   - APE_B=0
8. Power down outputs.
   - VOUTxL_EN=0
   - VOUTxR_EN=0
9. Disable remaining bias control bits.
   - FAST_EN=0
   - POBCTRL=0
   - BIAS_EN=0

Power supplies can now be safely removed from the WM8594 if desired. Table 33 describes the various bias control bits for power up/down control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R35 BIAS 23h	0	POBCTRL	0	**Bias Source for Output Amplifiers** 0 = Output amplifiers use master bias 1 = Output amplifiers use fast bias
	1	VMIDTOG	0	**VMID Power Down Characteristic** 0 = Slow ramp 1 = Fast ramp
	2	FAST_EN	0	**Fast Bias Enable** 0 = Fast bias disabled 1 = Fast bias enabled
	3	BUFIO_ EN	0	**VMID Buffer Enable** 0 = VMID Buffer disabled 1 = VMID Buffer enabled
	4	SOFT_ST	1	**VMID Soft Ramp Enable** 0 = Soft ramp disabled 1 = Soft ramp enabled
	5	BIAS_EN	0	**Master Bias Enable** 0 = Master bias disabled 1 = Master bias enabled Also powers down ADCVMID
	7:6	VMID_ SEL[1:0]	00	**VMID Resistor String Value Selection (DACVMID only)** 00 = off (no VMID) 01 = 150kΩ 10 = 750kΩ 11 = 15kΩ The selection is the total resistance of the string from DACREFP to DACREFN. The ADCVMID resistance is fixed at 200kΩ.

Table 33 Bias Control

GLOBAL ENABLE CONTROL

The WM8594 includes a number of enable and disable mechanisms to allow the device to be powered on and off in a pop-free manner. A global enable control bit enables the ADC, DAC and analogue paths. For full details of pop-free operation, see 'Pop and Click Performance' on page 45.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 ENABLE 0Ch	0	GLOBAL_ EN	0	**Device Global Enable** 0 = ADC, DAC and PGA ramp control circuitry disabled 1 = ADC, DAC and PGA ramp control circuitry enabled

Table 34 Global Enable Control

EMERGENCY POWER DOWN

In the event of sudden power failure in a system, or any other emergency condition, the /PWDN pin may be used to power the device down from any state in a controlled manner. This may be useful in a system where there is no guarantee the power supplies will be available long enough to complete the recommended power down sequence using software writes.

When the /PWDN is pulled low, the device will mute and then power down the outputs quietly. If the WM8593 is still receiving clocks, the outputs will be softmuted. If the clocks have stopped, the outputs will be muted immediately. Figure 24 shows the operation of /PWDN and the effect on the outputs of the device:

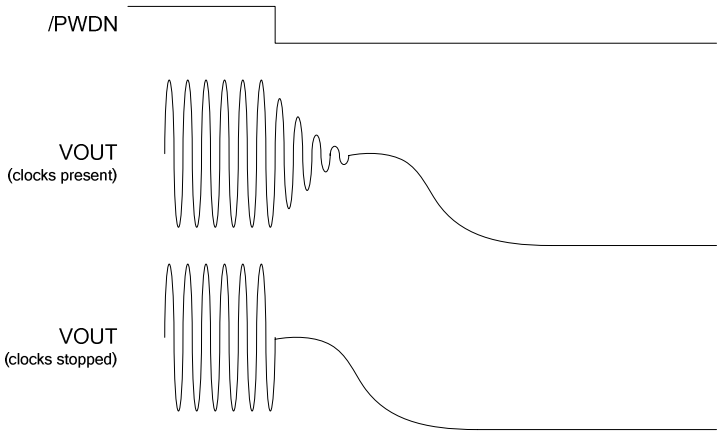


Figure 24 /PWDN Operation

It is expected that power is removed from the device before the device is used again, forcing the device to be reset via the POR. If this is not the case, the device must be manually reset by the customer (either by a software or hardware reset) once the /PWDN is pulled high again.

REGISTER MAP

Dec Addr	Hex Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Hex Default
0	00	DEVICE_ID	Read: DEVICE_ID[15:0] / Write: SW_RST																0x8594
1	01	REVISION	0	0	0	0	0	0	0	0	REVNUM[7:0]								0x0000
2	02	DAC1_CTRL1	0	0	0	0	DAC1_OP_MUX[1:0]		DAC1_MUTE	DAC1_EN	DAC1_ZCEN	DAC1_DEEMPH	DAC1_LRP	DAC1_BCP	DAC1_WL[1:0]		DAC1_FMT[1:0]		0x008A
3	03	DAC1_CTRL2	0	0	0	0	0	0	0	0	0	0	DAC1_BCLKDIV[2:0]			DAC1_SR[2:0]			0x0000
4	04	DAC1_CTRL3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAC1_MSTR	0x0000
5	05	DAC1L_VOL	0	0	0	0	0	0	0	DAC1L_VU	DAC1L_VOL[7:0]								0x00C8
6	06	DAC1R_VOL	0	0	0	0	0	0	0	DAC1R_VU	DAC1R_VOL[7:0]								0x00C8
7	07	DAC2_CTRL1	0	0	0	0	DAC2_OP_MUX[1:0]		DAC2_MUTE	DAC2_EN	DAC2_ZCEN	DAC2_DEEMPH	DAC2_LRP	DAC2_BCP	DAC2_WL[1:0]		DAC2_FMT[1:0]		0x008A
8	08	DAC2_CTRL2	0	0	0	0	0	0	0	0	0	0	DAC2_BCLKDIV[2:0]			DAC2_SR[2:0]			0x0000
9	09	DAC2_CTRL3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAC2_MSTR	0x0000
10	0A	DAC2L_VOL	0	0	0	0	0	0	0	DAC2L_VU	DAC2L_VOL[7:0]								0x00C8
11	0B	DAC2R_VOL	0	0	0	0	0	0	0	DAC2R_VU	DAC2R_VOL[7:0]								0x00C8
12	0C	ENABLE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DAC2_COPY_DAC	GLOBAL_EN	0x0000
13	0D	ADC_CTRL1	0	0	ADC_ZC_EN	ADC_HPD	ADC_DATA_SEL[1:0]		ADCL_INV	ADCR_INV	ADC_LRSWAP	ADC_EN	ADC_LRP	ADC_BCP	ADC_WL[1:0]		ADC_FMT[1:0]		0x200A
14	0E	ADC_CTRL2	0	0	0	0	0	0	0	0	0		ADC_BCLKDIV[2:0]			ADC_SR[2:0]			0x0000
15	0F	ADC_CTRL3	0	0	0	0	0	0	0	0	0	0	0	0	0	0		ADC_MSTR	0x0000
16	10	ADCL_VOL	0	0	0	0	0	0	0	ADCL_VU	ADCL_VOL[7:0]								0x00C3
17	11	ADCR_VOL	0	0	0	0	0	0	0	ADCR_VU	ADCR_VOL[7:0]								0x00C3
19	13	PGA1L_VOL	0	0	0	0	0	0	0	PGA1L_VU	PGA1L_VOL[7:0]								0x000C
20	14	PGA1R_VOL	0	0	0	0	0	0	0	PGA1R_VU	PGA1R_VOL[7:0]								0x000C
21	15	PGA2L_VOL	0	0	0	0	0	0	0	PGA2L_VU	PGA2L_VOL[7:0]								0x000C
22	16	PGA2R_VOL	0	0	0	0	0	0	0	PGA2R_VU	PGA2R_VOL7:0]								0x000C
23	17	PG3L_VOL	0	0	0	0	0	0	0	PGA3L_VU	PGA3L_VOL[7:0]								0x000C
24	18	PGA3R_VOL	0	0	0	0	0	0	0	PGA3R_VU	PGA3R_VOL[7:0]								0x000C
25	19	PGA_CTRL1	0	0	0	0	0	0	0	0	PGA3R_ZC	PGA3L_ZC	PGA2R_ZC	PGA2L_ZC	PGA1R_ZC	PGA1L_ZC	TTACK_BYPAS	ECAY_BYPAS	0x0003
26	1A	PGA_CTRL2	0	0	0	0	0	0	0	0	0	PGA3R_MUTE	PGA3L_MUTE	PGA2R_MUTE	PGA2L_MUTE	PGA1R_MUTE	PGA1L_MUTE	MUTE_ALL	0x007E
27	1B	GEN	0	0	0	0	0	0	0	0	0	PGA_SR[2:0]			AUTO_INC	0	0	0	0x0048
28	1C	INPUT_CTRL1	0	0	0	0	PGA2L_IN_SEL[3:0]				PGA1R_IN_SEL[3:0]				PGA1L_IN_SEL[3:0]				0x0000
29	1D	INPUT_CTRL2	0	0	0	0	PGA3R_IN_SEL[3:0]				PGA3L_IN_SEL[3:0]				PGA2R_IN_SEL[3:0]				0x0000
30	1E	INPUT_CTRL3	0	0	0	0	0	ADC_SWITCH_E	ADC_AMP_VOL[1:0]		ADCR_SEL[3:0]				ADCL_SEL[3:0]				0x0008
31	1F	INPUT_CTRL4	0	0	0	0	0	0	0	0	ADCR_AMP_EN	ADCL_AMP_EN	PGA3R_EN	PGA3L_EN	PGA2R_EN	PGA2L_EN	PGA1R_EN	PGA1L_EN	0x0000
32	20	OUTPUT_CTRL1	0	0	0	0	0	0	0	VOUT2L_SEL[2:0]			VOUT1R_SEL[2:0]			VOUT1L_SEL[2:0]			0x0088
33	21	OUTPUT_CTRL2	0	0	0	0	0	0	0	VOUT3R_SEL[2:0]			VOUT3L_SEL[2:0]			VOUT2R_SEL[2:0]			0x0163
34	22	OUTPUT_CTRL3	0	0	0	VOUT3R_EN	VOUT3L_EN	VOUT2R_EN	VOUT2L_EN	VOUT1R_EN	VOUT1L_EN	APE_B	VOUT3R_TRI	VOUT3L_TRI	VOUT2R_TRI	VOUT2L_TRI	VOUT1R_TRI	VOUT1L_TRI	0x0040
35	23	BIAS	0	0	0	0	0	0	0	0	VMID_SEL[1:0]		BIAS_EN	SOFT_ST	BUFIOEN	FAST_EN	VMIDTOG	POBCTRL	0x0010
36	24	PGA_CTRL_3	0	0	0	0	0	PGA_UPD	0	0	0	0	0	0	PGA_SEL[2:0]			PGA_SAFE_SW	0x0002

R0 (0h) – Software Reset / Device ID Register (DEVICE_ID)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	DEVICE_ID[15:8]							
Write	SW_RST							
Default	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DEVICE_ID[7:0]							
Write	SW_RST							
Default	**1**	**0**	**0**	**1**	**0**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DEVICEID[15:0]	**Device ID** A read of this register will return the device ID. In this case 0x8594.
SW_RST	**Software Reset** A write of any value to this register will generate a software reset.

Figure 25 R0 – Software Reset / Device ID

R1 (01h) – Device Revision Register (REVISION)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	REVNUM[7:0]							
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
N/A = Not Applicable (no function implemented)								

Function	Description
REVNUM[7:0]	**Device Revision** A read of this register will return the device revision number. This number is sequentially incremented if the device design is updated.

Figure 26 R1 – Device Revision Register

R2 (02h) – DAC Control Register 1 (DAC1_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	DAC1_OP_MUX[1:0]		DAC1_MUTE	DAC1_EN
Write	N/A	N/A	N/A	N/A				
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC1_ZCEN	DAC1_ DEEMPH	DAC1_LRP	DAC1_BCP	DAC1_WL[1:0]		DAC1_FMT[1:0]	
Write								
Default	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
DAC1_FMT[1:0]	**DAC1 Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
DAC1_WL[1:0]	**DAC1 Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
DAC1_BCP	**DAC1 BCLK Polarity** 0 = DACBCLK not inverted - data latched on rising edge of BCLK 1 = DACBCLK inverted - data latched on falling edge of BCLK
DAC1_LRP	**DAC1 LRCLK Polarity** 0 = DACLRCLK not inverted 1 = DACLRCLK inverted
DAC1_DEEMPH	**DAC1 Deemphasis** 0 = No deemphasis 1 = Apply 44.1kHz deemphasis
DAC1_ZCEN	**DAC1 Digital Volume Control Zero Cross Enable** 0 = Do not use zero cross 1 = Use zero cross
DAC1_EN	**DAC1 Enable** 0 = DAC disabled 1 = DAC enabled
DAC1_MUTE	**DAC1 Softmute** 0 = Normal operation 1 = Softmute applied
DAC1_OP_MUX[1:0]	**DAC1 Digital Monomix** 00 = Stereo (Normal Operation) 01 = Mono (Left data to DAC1R) 10 = Mono (Right data to DAC1L) 11 = Digital Monomix, (L+R)/2

Figure 27 R2 – DAC1 Control Register 1

R3 (03h) – DAC1 Control Register 2 (DAC1_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	DAC1_BCLKDIV[2:0]			DAC1_SR[2:0]		
Write	N/A	N/A						
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC1_SR[2:0]	**DAC1 MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
DAC1_ BCLKDIV [2:0]	**DAC1 BCLK Rate** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of DAC1_BCLKDIV[2:0] are reserved

Figure 28 R3 – DAC1 Control Register 2

R4 (04h) – DAC1 Control Register 3 (DAC1_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	0	0	0	0	0	DAC1_MSTR
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC1_MSTR	**DAC1 Master Mode Select** 0 = Slave mode, DACBCLK1 and DACLRCLK1 are inputs to WM8594 1 = Master mode, DACBCLK1 and DACLRCLK1 are outputs from WM8594

Figure 29 R4 – DAC1 Control Register 3

R5 (05h) – DAC1L Digital Volume Control Register (DAC1L_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	DAC1L_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC1L_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC1L_VOL[7:0]	**DAC1L Digital Volume** 0000 0000 = -100dB 0000 0001 = -99.5dB 0000 0010 = -99dB …0.5dB steps 1100 1000 = 0dB …0.5dB steps 1101 1111 = +11.5dB 111X XXXX = +12dB
DAC1L_VU	**DAC1L Digital Volume Update** 0 = Latch DAC1L_VOL[7:0] into Register Map but do not update volume 1 = Latch DAC1L_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 30 R5 – DAC1L Digital Volume Control Register

R6 (06h) – DAC1R Digital Volume Control Register (DAC1R_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	DAC1R_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC1R_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC1R_VOL[7:0]	**DAC1R Digital Volume** 0000 0000 = -100dB 0000 0001 = -99.5dB 0000 0010 = -99dB …0.5dB steps 1100 1000 = 0dB …0.5dB steps 1101 1111 = +11.5dB 111X XXXX = +12dB
DAC1R_VU	**DAC1R Digital Volume Update** 0 = Latch DACR_VOL[7:0] into Register Map but do not update volume 1 = Latch DACR_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 31 R6 – DAC1R Digital Volume Control Register

R7 (07h) – DAC2 Control Register 1 (DAC2_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	DAC2_OP_MUX[1:0]		DAC2_MUTE	DAC2_EN
Write	N/A	N/A	N/A	N/A				
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC2_ZCEN	DAC2_ DEEMPH	DAC2_LRP	DAC2_BCP	DAC2_WL[1:0]		DAC2_FMT[1:0]	
Write								
Default	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
DAC2_FMT[1:0]	**DAC2 Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
DAC2_WL[1:0]	**DAC2 Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
DAC2_BCP	**DAC2 BCLK Polarity** 0 = DACBCLK not inverted - data latched on rising edge of BCLK 1 = DACBCLK inverted - data latched on falling edge of BCLK
DAC2_LRP	**DAC2 LRCLK Polarity** 0 = DACLRCLK not inverted 1 = DACLRCLK inverted
DAC2_DEEMPH	**DAC2 Deemphasis** 0 = No deemphasis 1 = Apply 44.1kHz de-emphasis
DAC2_ZCEN	**DAC2 Digital Volume Control Zero Cross Enable** 0 = Do not use zero cross 1 = Use zero cross
DAC2_EN	**DAC2 Enable** 0 = DAC2 disabled 1 = DAC2 enabled
DAC2_MUTE	**DAC2 Softmute** 0 = Normal operation 1 = Softmute applied
DAC2_OP_MUX[1:0]	**DAC2 Digital Monomix** 00 = Stereo (Normal Operation) 01 = Mono (Left data to Right DAC2) 10 = Mono (Right data to Left DAC2) 11 = Digital Monomix, (L+R)/2

Figure 32 R7 – DAC2 Control Register 1

R8 (08h) – DAC2 Control Register 2 (DAC2_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	DAC2_BCLKDIV[2:0]			DAC2_SR[2:0]		
Write	N/A	N/A						
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC2_SR[2:0]	**DAC2 MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
DAC2_BCLKDIV[2:0]	**DAC2 BCLK Rate** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of DAC2_BCLKDIV[2:0] are reserved

Figure 33 R8 – DAC2 Control Register 2

R9 (09h) – DAC2 Control Register 3 (DAC2_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	0	0	0	0	0	DAC2_MSTR
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC2_MSTR	**DAC2 Master Mode Select** 0 = Slave mode, DACBCLK2 and DACLRCLK2 are inputs to WM8594 1 = Master mode, DACBCLK2 and DACLRCLK2 are outputs from WM8594

Figure 34 R9 – DAC2 Control Register 3

R10 (0Ah) – DAC2L Digital Volume Control Register (DAC2L_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	DAC2L_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC2L_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC2L_VOL[7:0]	**DAC2 Digital Volume** 0000 0000 = -100dB 0000 0001 = -99.5dB 0000 0010 = -99dB …0.5dB steps 1100 1000 = 0dB …0.5dB steps 1101 1111 = +11.5dB 111X XXXX = +12dB
DAC2L_VU	**DAC2 Digital Volume Update** 0 = Latch DAC2L_VOL[7:0] into Register Map but do not update volume 1 = Latch DAC2L_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 35 R10 – DAC2L Digital Volume Control Register

R11 (0Bh) – DAC2R Digital Volume Control Register (DAC2R_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	DAC2R_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	DAC2R_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DAC2R_VOL[7:0]	**DAC2R Digital Volume** 0000 0000 = -100dB 0000 0001 = -99.5dB 0000 0010 = -99dB …0.5dB steps 1100 1000 = 0dB …0.5dB steps 1101 1111 = +11.5dB 111X XXXX = +12dB
DAC2R_VU	**DAC2R Digital Volume Update** 0 = Latch DAC2R_VOL[7:0] into Register Map but do not update volume 1 = Latch DAC2R_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 36 R11 – DAC2R Digital Volume Control Register

R12 (0Ch) – Device Enable Register (ENABLE)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	0	0	0	0	DAC2_ COPY_DAC1	GLOBAL_EN
Write	N/A	N/A	N/A	N/A	N/A	N/A		
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
GLOBAL_EN	**Device Global Enable** 0 = ADC, DAC and PGA ramp control circuitry disabled 1 = ADC, DAC and PGA ramp control circuitry enabled
DAC2_COPY_DAC1	**DAC2 Configuration Control** 0 = DAC2 settings independent of DAC1 1 = DAC2 settings are the same as DAC1

Figure 37 R12 – Device Enable Register

R13 (0Dh) – ADC Control Register 1 (ADC_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	ADC_ZCEN	ADC_HPD	ADC_DATA_SEL[1:0]		ADCL_INV	ADCR_INV
Write	N/A	N/A						
Default	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	ADC_ LRSWAP	ADC_EN	ADC_LRP	ADC_BCP	ADC_WL[1:0]		ADC_FMT[1:0]	
Write								
Default	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
ADC_FMT[1:0]	**ADC Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
ADC_WL[1:0]	**ADC Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
ADC_BCP	**ADC BCLK Polarity** 0 = ADCBCLK not inverted - data latched on rising edge of BCLK 1 = ADCBCLK inverted - data latched on falling edge of BCLK
ADC_LRP	**ADC LRCLK Polarity** 0 = ADCLRCLK not inverted 1 = ADCLRCLK inverted

ADC_EN	**ADC Enable** 0 = ADC disabled 1 = ADC enabled
ADC_LRSWAP	**ADC Left/Right Swap** 0 = Normal 1 = Swap left channel data into right channel and vice-versa
ADCR_INV ADCL_INV	**ADCL and ADCR Output Signal Inversion** 0 = Output not inverted 1 = Output inverted
ADC_DATA_SEL[1:0]	**ADC Data Output Select** 00 = left data from ADCL, right data from ADCR (Normal Stereo) 01 = left data from ADCL, right data from ADCL (Mono Left) 10 = left data from ADCR, right data from ADCR (Mono Right) 11 = left data from ADCR, right data from ADCL (Reverse Stereo)
ADC_HPD	**ADC High Pass Filter Disable** 0 = High pass filter enabled 1 = High pass filter disabled
ADC_ZC_EN	**ADC Digital Volume Control Zero Cross Enable** 0 = Do not use zero cross, change volume instantly 1 = Use zero cross, change volume when data crosses zero

Figure 38 R13 – ADC Control Register 1

R14 (0Eh) – ADC Control Register 2 (ADC_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	ADC_BCLKDIV[2:0]			ADC_SR[2:0]		
Write	N/A	N/A						
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	**Description**
ADC_SR[2:0]	**ADC MCLK:LRCLK Ratio** 000 = Auto detect 001 = reserved 010 = reserved 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = Reserved
ADC_BCLKDIV[2:0]	**ADC BCLK Rate (when ADC in Master Mode)** 000 = MCLK / 4 001 = MCLK / 8 010 = 32fs 011 = 64fs 100 = 128fs All other values of ADC_BCLKDIV[2:0] are reserved

Figure 39 R14 – ADC Control Register 2

R15 (0Fh) – ADC Control Register 3 (ADC_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	0	0	0	0	0	ADC_MSTR
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
ADC_MSTR	**ADC Master Mode Select** 0 = Slave mode, ADCBCLK and ADCLRCLK are inputs to WM8594 1 = Master mode, ADCBCLK and ADCLRCLK are outputs from WM8594

Figure 40 R15 – ADC Control Register 3

R16 (10h) – Left ADC Digital Volume Control Register (ADCL_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	ADCL_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	ADCL_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
N/A = Not Applicable (no function implemented)								

Function	Description
ADCL_VOL[7:0]	**Left ADC Digital Volume** 0000 0000 = Digital mute 0000 0001 = -97dB 0000 0010 = -96.5dB …0.5dB steps 1100 0011 = 0dB …0.5dB steps 1111 1110 = +29.5dB 1111 1111 = +30dB
ADCL_VU	**Left DAC Digital Volume Update** 0 = Latch ADCL_VOL[7:0] into Register Map but do not update volume 1 = Latch ADCL_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 41 R10 – Left ADC Digital Volume Control Register

R17 (11h) – Right ADC Digital Volume Control Register (ADCR_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	ADCR_VU
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	ADCR_VOL[7:0]							
Write								
Default	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**

N/A = Not Applicable (no function implemented)

Function	Description
ADCR_VOL[7:0]	**Right ADC Digital Volume** 0000 0000 = Digital mute 0000 0001 = -97dB 0000 0010 = -96.5dB …0.5dB steps 1100 0011 = 0dB …0.5dB steps 1111 1110 = +29.5dB 1111 1111 = +30dB
ADCR_VU	**Right ADC Digital Volume Update** 0 = Latch ADCR_VOL[7:0] into Register Map but do not update volume 1 = Latch ADCR_VOL[7:0] into Register Map and update left and right channels simultaneously

Figure 42 R17 – Right ADC Digital Volume Control Register

R19 (13h) – PGA1L Volume Control Register (PGA1L_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA1L_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA1L_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								
R20 (14h) – PGA1R Volume Control Register (PGA1R_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA1R_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA1R_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								
R21 (15h) – PGA2L Volume Control Register (PGA2L_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA2L_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA2L_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								
R22 (16h) – PGA2R Volume Control Register (PGA2R_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA2R_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA2R_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

…Continued on next page

R23 (17h) – PGA3L Volume Control Register (PGA3L_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA3L_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA3L_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

R24 (18h) – PGA3R Volume Control Register (PGA3R_VOL)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	PGA3R_VU
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA3R_VOL[7:0]							
Write								
Default	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
N/A = Not Applicable (no function implemented)								

PGA1L_VOL[7:0] PGA1R_VOL[7:0] PGA2L_VOL[7:0] PGA2R_VOL[7:0] PGA3L_VOL[7:0] PGA3R_VOL[7:0]	**Input PGA Volume** 0000 0000 = +6dB 0000 0001 = +5.5dB …0.5dB steps 00001100 = 0dB … 1001 1111 = -73.5dB 101X XXXX = PGA Mute
PGA1L_VU PGA1R_VU PGA2L_VU PGA2R_VU PGA3L_VU PGA3R_VU	**Input PGA Volume Update** 0 = Latch corresponding volume setting into Register Map but do not update volume 1 = Latch corresponding volume setting into Register Map and update all channels simultaneously

Figure 43 R19-24 – PGA Volume Control Registers

R25 (19h) – PGA Control Register 1 (PGA_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA3R_ZC	PGA3L_ZC	PGA2R_ZC	PGA2L_ZC	PGA1R_ZC	PGA1L_ZC	ATTACK_ BYPASS	DECAY_ BYPASS
Write								
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
DECAY_BYPASS	**PGA Gain Decay Mode** 0 = PGA gain will ramp down 1 = PGA gain will step down
ATTACK_BYPASS	**PGA Gain Attack Mode** 0 = PGA gain will ramp up 1 = PGA gain will step up
PGA1L_ZC PGA1R_ZC PGA2L_ZC PGA2R_ZC PGA3L_ZC PGA3R_ZC	**PGA Gain Zero Cross Enable** 0 = PGA gain updates occur immediately 1 = PGA gain updates occur on zero cross Zero cross must be disabled to use gain ramp

Figure 44 R25 – PGA Control Register 1

R26 (1Ah) – PGA Control Register 2 (PGA_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	PGA3R_ MUTE	PGA3L_ MUTE	PGA2R_ MUTE	PGA2L_ MUTE	PGA1R_ MUTE	PGA1L_ MUTE	MUTE_ALL
Write	N/A							
Default	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
MUTE_ALL	**Master PGA Mute Control** 0 = Unmute all PGAs 1 = Mute all PGAs
PGA1L_MUTE PGA1R_MUTE PGA2L_MUTE PGA2R_MUTE PGA3L_MUTE PGA3R_MUTE	**Individual PGA Mute Control** 0 = Unmute PGA 1 = Mute PGA

Figure 45 R26 – PGA Control Register 2

R27 (1Bh) – Additional Control Register 1 (ADD_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	PGA_SR[2:0]			AUTO_INC	0	0	0
Write	N/A					N/A	N/A	N/A
Default	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
AUTO_INC	**2-wire Software Mode Auto Increment Enable** 0 = Auto increment disabled 1 = Auto increment enabled
PGA_SR[2:0]	**Sample Rate for PGA** 000 = 32kHz 001 = 44.1kHz 010 = 48kHz 011 = 88.2kHz 100 = 96kHz 101 = 176.4kHz 11X = 192kHz See Table 27 for further information on PGA sample rate versus volume ramp rate.

Figure 46 R27 – Additional Control Register 1

R28 (1Ch) – Input Control Register 1 (INPUT_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	PGA2L_IN_SEL[3:0]			
Write	N/A	N/A	N/A	N/A				
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA1R_IN_SEL[3:0]				PGA1L_IN_SEL[3:0]			
Write								
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

R29 (1Dh) – Input Control Register 2 (INPUT_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	PGA3R_IN_SEL[3:0]			
Write	N/A	N/A	N/A	N/A				
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	PGA3L_IN_SEL[3:0]				PGA2R_IN_SEL[3:0]			
Write								
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
PGA1L_IN_SEL[3:0] PGA2L_IN_SEL[3:0] PGA3L_IN_SEL[3:0]	**Left Input PGA Source Selection** 0000 = No input selected 0001 = VIN1L selected 0010 = VIN2L selected 0011 = VIN3L selected 0100 = VIN4L selected 0101 = VIN5L selected 0110 to 1000 = reserved 1001 = DAC1L output selected 1010 = DAC1R output selected 1011 = DAC2L output selected 1100 = DAC2R output selected 1101 to 1111 = reserved
PGA1R_IN_SEL[3:0] PGA2R_IN_SEL[3:0] PGA3R_IN_SEL[3:0]	**Right Input PGA Source Selection** 0000 = No input selected 0001 = VIN1R selected 0010 = VIN2R selected 0011 = VIN3R selected 0100 = VIN4R selected 0101 = VIN5R selected 0110 to 1000 = reserved 1001 = DAC1L output selected 1010 = DAC1R output selected 1011 = DAC2L output selected 1100 = DAC2R output selected 1101 to 1111 = reserved

Figure 47 R28-29 – Input Control Registers 1-2

R30 (1Eh) – Input Control Register 3 (INPUT_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	ADC_ SWITCH_EN	ADC_AMP_VOL[1:0]	
Write	N/A	N/A	N/A	N/A	N/A			
Default	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	ADCR_SEL[3:0]				ADCL_SEL[3:0]			
Write								
Default	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
ADCL_SEL[3:0] ADCR_SEL[3:0]	**ADC Input Select** 0000 = VIN1L 0001 = VIN2L 0010 = VIN3L 0011 = VIN4L 0100 = VIN5L 0101 to 1000 = reserved 1000 = VIN1R 1001 = VIN2R 1010 = VIN3R 1011 = VIN4R 1100 = VIN5R 1101 to 1111 = reserved
ADC_AMP_VOL[1:0]	**ADC Amplifier Gain Control** 00 = 0dB 01 = +3dB 10 = +6dB 11 = +12dB
ADC_SWITCH_EN	**ADC Input Switch Control** 0 = ADC input switches open 1 = ADC input switches closed

Figure 48 R30 – Input Control Register 3

R31 (1Fh) – Input Control Register 4 (INPUT_CTRL4)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	ADCR_AMP_	ADCL_AMP_	PGA3R_EN	PGA3L_EN	PGA2R_EN	PGA2L_EN	PGA1R_EN	PGA1L_EN
Write	EN	EN						
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

Function	Description
PGA1L_EN PGA1R_EN PGA2L_EN PGA2R_EN PGA3L_EN PGA3R_EN	**Input PGA Enable Controls** 0 = PGA disabled 1 = PGA enabled
ADCL_AMP_EN ADCR_AMP_EN	**ADC Input Amplifier Enable Controls** 0 = Amplifier disabled 1 = Amplifier enabled

Figure 49 R31 – Input Control Register 4

R32 (20h) – Output Control Register 1 (OUTPUT_CTRL1)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	VOUT2L_ SEL[2]
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	VOUT2L_SEL[1:0]		VOUT1R _SEL[2:0]			VOUT1L_SEL[2:0]		
Write								
Default	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
N/A = Not Applicable (no function implemented)								

R33 (21h) – Output Control Register 2 (OUTPUT_CTRL2)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	VOUT3R_ SEL[2]
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	VOUT3R_SEL [1:0]		VOUT3L_SEL [2:0]			VOUT2R_SEL[2:0]		
Write								
Default	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**
N/A = Not Applicable (no function implemented)								

Function	Description
VOUT1L_SEL[3:0] VOUT1R_SEL [3:0] VOUT2L_SEL [3:0] VOUT2R_SEL [3:0] VOUT3L_SEL [3:0] VOUT3R_SEL [3:0]	**Output Mux Selection** 000 = PGA1L 001 = PGA1R 010 = PGA2L 011 = PGA2R 100 = PGA3L 101 = PGA3R 11X = Reserved

Figure 50 R32-33 – Output Control Registers 1-2

R34 (22h) – Output Control Register 3 (OUTPUT_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	VOUT3R_EN	VOUT3L_EN	VOUT2R_EN	VOUT2L_EN	VOUT1R_EN
Write	N/A	N/A	N/A					
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	VOUT1L_EN	APE_B	VOUT3R_TRI	VOUT3L_TRI	VOUT2R_TRI	VOUT2L_TRI	VOUT1R_TRI	VOUT1L_TRI
Write								
Default	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
VOUT1L_TRI VOUT1R_TRI VOUT2L_TRI VOUT2R_TRI VOUT3L_TRI VOUT3R_TRI	**Output Amplifier Tristate Control** 0 = Normal operation 1 = Output amplifier tristate enable (Hi-Z)
APE_B	**Clamp Outputs to Ground** 0 = clamp active 1 = clamp not active
VOUT1L_EN VOUT1R_EN VOUT2L_EN VOUT2R_EN VOUT3L_EN VOUT3R_EN	**Output Amplifier Enables** 0 = Output amplifier disabled 1 = Output amplifier enabled

Figure 51 R34 – Output Control Register 3

R35 (23h) – Bias Control Register (BIAS)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	0	0	0
Write	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	VMID_SEL[1:0]		BIAS_EN	SOFT_ST	BUFIO_EN	FAST_EN	VMIDTOG	POBCTRL
Write								
Default	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
POBCTRL	**Bias Source for Output Amplifiers** 0 = Output amplifiers use master bias 1 = Output amplifiers use fast bias
VMIDTOG	**VMID Power Down Characteristic** 0 = Slow ramp 1 = Fast ramp
FAST_EN	**Fast Bias Enable** 0 = Fast bias disabled 1 = Fast bias enabled
BUFIO_EN	**VMID Buffer Enable** 0 = VMID Buffer disabled 1 = VMID Buffer enabled
SOFT_ST	**VMID Soft Ramp Enable** 0 = Soft ramp disabled 1 = Soft ramp enabled
BIAS_EN	**Master Bias Enable** 0 = Master bias disabled 1 = Master bias enabled Also powers down ADCVMID
VMID_SEL[1:0]	**VMID Resistor String Value Selection (DACVMID only)** 00 = off (no VMID) 01 = 150kΩ 10 = 750kΩ 11 = 15kΩ The selection is the total resistance of the string from DACREFP to DACREFN. The ADCVMID resistance is fixed at 200kΩ.

Figure 52 R35 – Bias Control Register

R36 (24h) – PGA Control Register 3 (PGA_CTRL3)								
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	0	0	0	0	0	PGA_UPD	0	0
Write	N/A	N/A	N/A	N/A	N/A		N/A	N/A
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Bit #	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	0	0	0	0	PGA_SEL[2:0]			PGA_ SAFE_SW
Write	N/A	N/A	N/A	N/A				
Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

N/A = Not Applicable (no function implemented)

Function	Description
PGA_SAFE_SW	**PGA Ramp Control Clock Source Mux Force Update** 0 = Wait until clocks are safe before switching PGA clock source 1 = Force PGA clock source to change immediately See page 38 for details of use.
PGA_SEL[2:0]	**PGA Ramp Control Clock Source** 000 = ADCLRCLK 001 = DACLRCLK1 010 = DACLRCLK2 011 = reserved 100 = reserved 101 = DACLRCLK1 (when DAC1 is being used in master mode) 110 = DACLRCLK2 (when DAC2 is being used in master mode) 111 = ADCLRCLK (when ADC is being used in master mode)
PGA_UPD	**PGA Ramp Control Clock Source Mux Update** 0 = Do not update PGA clock source 1 = Update clock source

Figure 53 R36 – PGA Control Register 3

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	± 0.05dB			0.454fs	
Passband Ripple				0.05	dB
Stopband		0.546fs			
Stopband Attenuation		-60			dB
Group Delay			16		fs
DAC Filter – 32kHz to 96kHz					
Passband	± 0.1dB			0.454fs	
Passband Ripple				0.1	dB
Stopband		0.546fs			
Stopband attenuation	f > 0.546fs	-50			dB
Group Delay			10		Fs
DAC Filter – 176.4kHz to 192kHz					
Passband	± 0.1dB			0.247fs	
Passband Ripple				0.1	dB
Stopband		0.753fs			
Stopband attenuation	f > 0.546fs	-50			dB
Group Delay			10		Fs

DAC FILTER RESPONSES

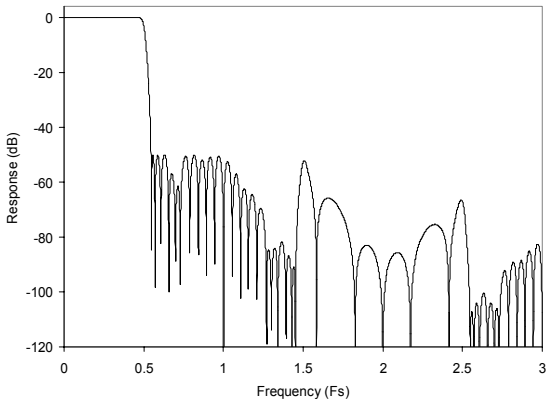


Figure 54 DAC Digital Filter Frequency Response – 32kHz to 96kHz

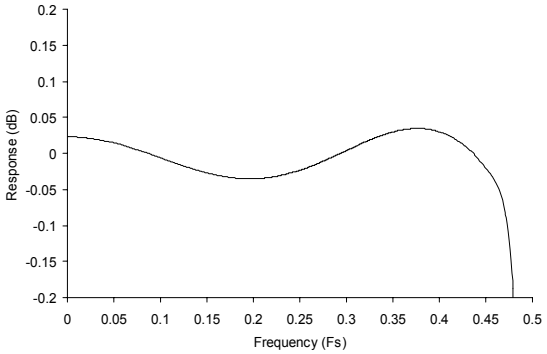


Figure 55 DAC Digital Filter Ripple –32kHz to 96kHz

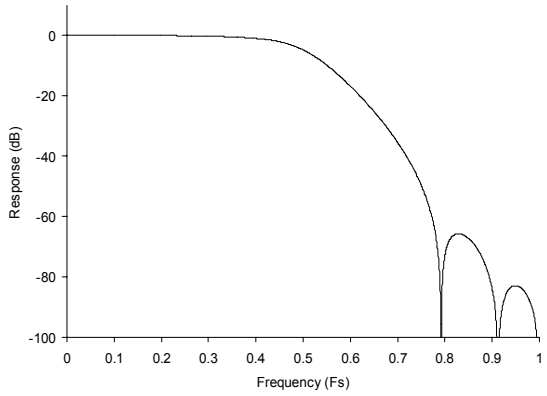


Figure 56 DAC Digital Filter Frequency Response – 176.4kHz to 192kHz

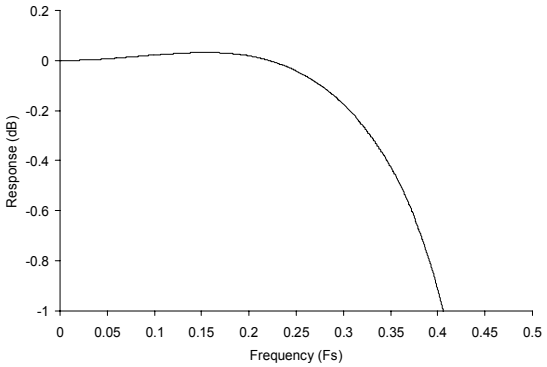


Figure 57 DAC Digital Filter Ripple – 176.4kHz to 192kHz

DIGITAL DE-EMPHASIS CHARACTERISTICS

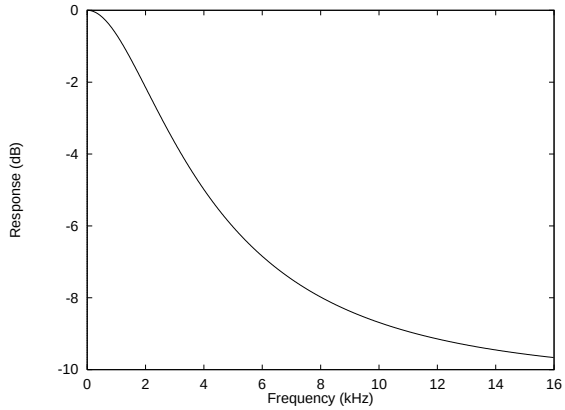


Figure 58 De-Emphasis Frequency Response (32kHz)

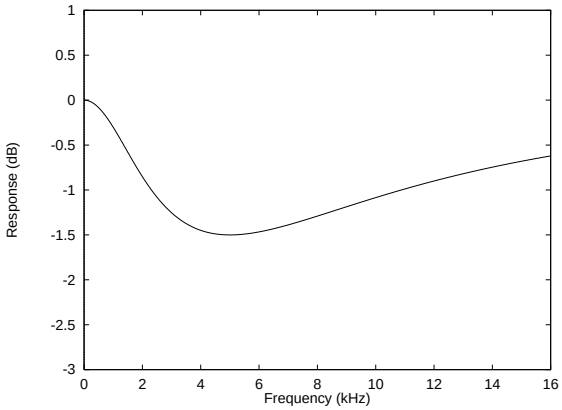


Figure 59 De-Emphasis Error (32kHz)

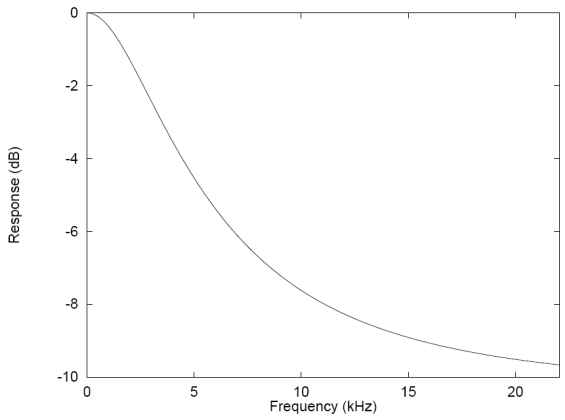


Figure 60 De-Emphasis Frequency Response (44.1KHz)

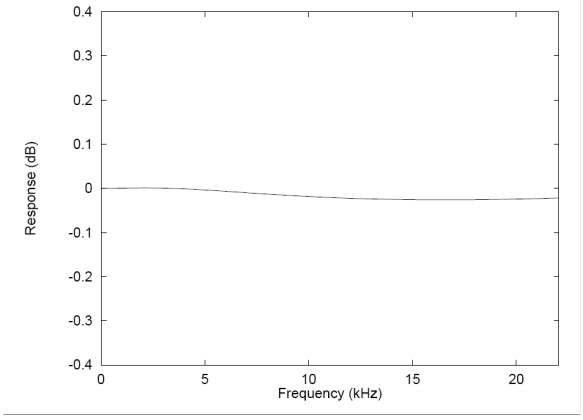


Figure 61 De-Emphasis Error (44.1KHz)

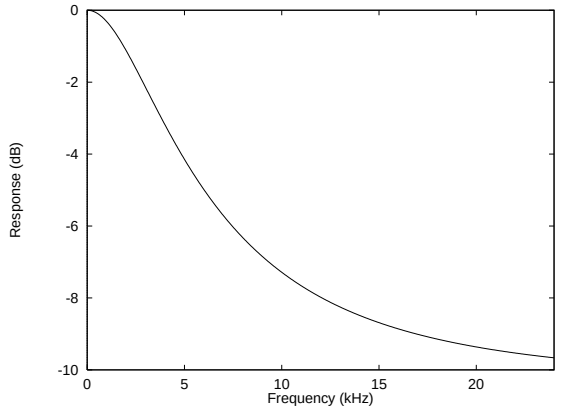


Figure 62 De-Emphasis Frequency Response (48kHz)

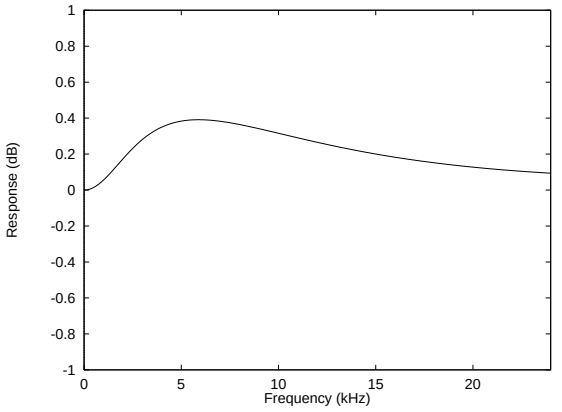


Figure 63 De-Emphasis Error (48kHz)

ADC FILTER RESPONSES

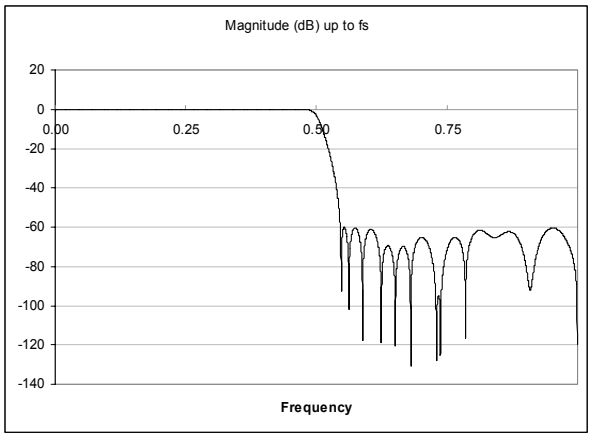


Figure 64 ADC Digital Filter Frequency Response

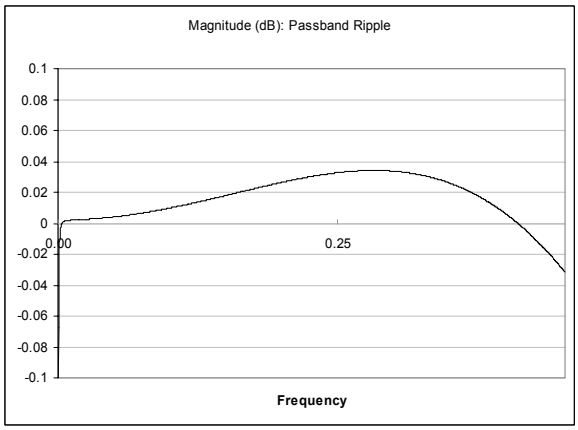


Figure 65 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8594 has a selectable digital high pass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

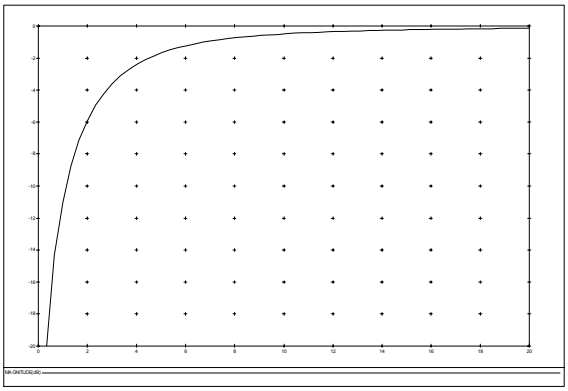
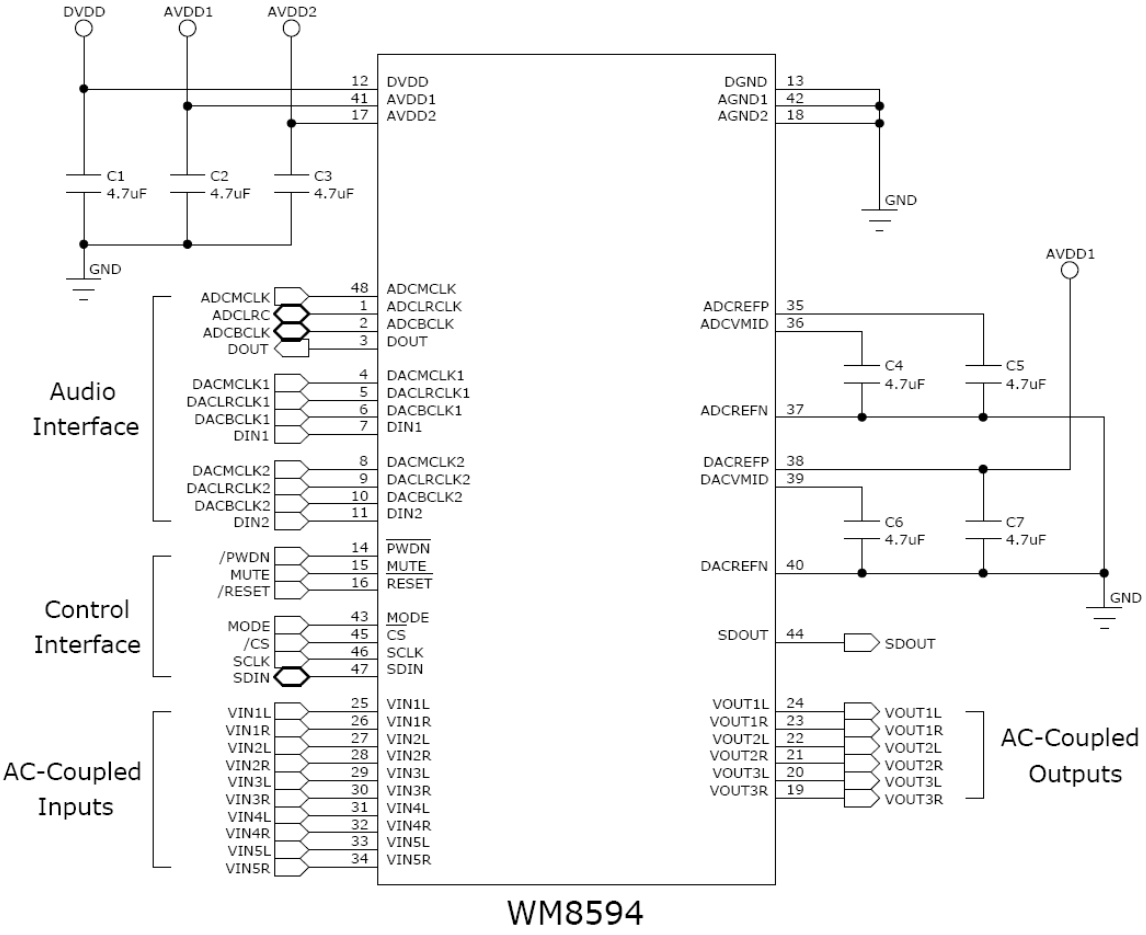


Figure 66 ADC Highpass Filter Response

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



Notes:

1. AGND and DGND should ideally share a continuous ground plane. Where this is not possible, it is recommended that AGND and DGND are connected as close to the WM8594 as possible.
2. Decoupling capacitors shown are very low-ESR, multilayer ceramic capacitors and should be placed as near to the WM8594 as possible. Equally good results may be obtained using 0.1µF ceramic capacitors near to the WM8594, with a 10µF electrolytic capacitor nearby.

RECOMMENDED ANALOGUE LOW PASS FILTER

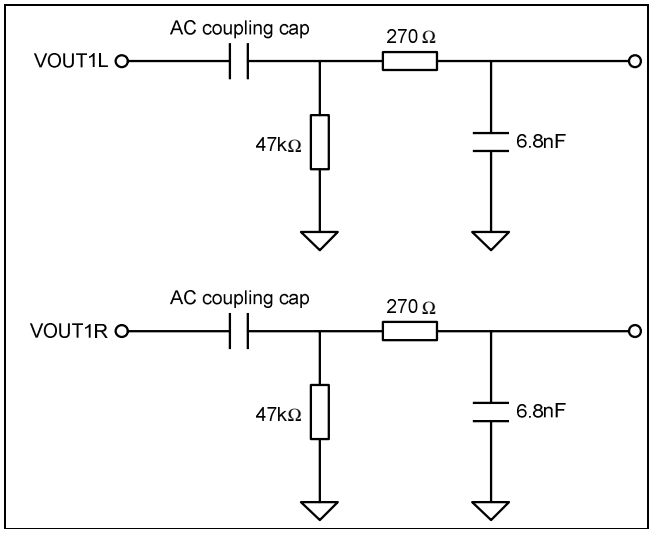


Figure 67 Recommended Analogue Low Pass Filter (shown for VOUT1L/R)

Note: See WAN0176 for AC coupling capacitor selection information.

An external single pole RC filter is recommended (see Figure 67) if the device is driving a wideband amplifier. Other filter architectures may provide equally good results.

EXTENDED INPUT IMPEDANCE CONFIGURATION

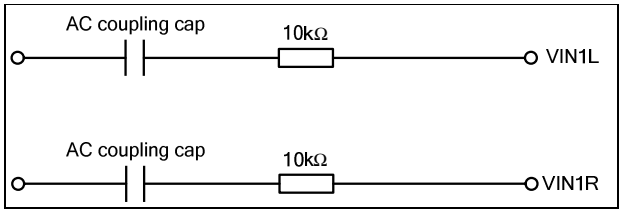


Figure 68 Extended Input Impedance Configuration

Note: See WAN0176 for AC coupling capacitor selection information.

The input impedance to the WM8594 is specified in the Electrical Characteristics section beginning on p8, and is fixed across gain setting and signal routing options. If this input impedance is not enough for the intended application, an alternative input configuration (Figure 68) is possible.

This configuration increases the input impedance to the WM8594 by 10kΩ, but reduces the overall gain in the ADC and Bypass paths by -6dB. In order to compensate for this reduction in gain, +6dB of gain should be set in the ADC Input PGA (by using ADC_AMP_VOL[1:0]) and in the bypass PGA (by using PGAxx_VOL[7:0]).

Examples:

- If a $2V_{RMS}$ signal is applied to VIN1L and VIN1R and routed to VOUT1L and VOUT1R using PGA1L and PGA1R, then setting PGA1L_VOL[7:0] and PGA1R_VOL[7:0] =0x00 is necessary to see $2V_{RMS}$ at VOUT1L and VOUT1R.
- If a $2V_{RMS}$ signal is applied to VIN1L and VIN1R and routed to ADCL and ADCR, then setting ADC_AMP_VOL[1:0]=10 is necessary to see 0dBFS at the ADC outputs.

RELEVANT APPLICATION NOTES

The following application notes, available from www.wolfsonmicro.com, may provide additional guidance for the use of the WM8594.

DEVICE PERFORMANCE:

WAN0129 – Decoupling and Layout Methodology for Wolfson DACs, ADCs and CODECs

WAN0144 – Using Wolfson Audio DACs and CODECs with Noisy Supplies

WAN0176 – AC Coupling Capacitor Selection

GENERAL:

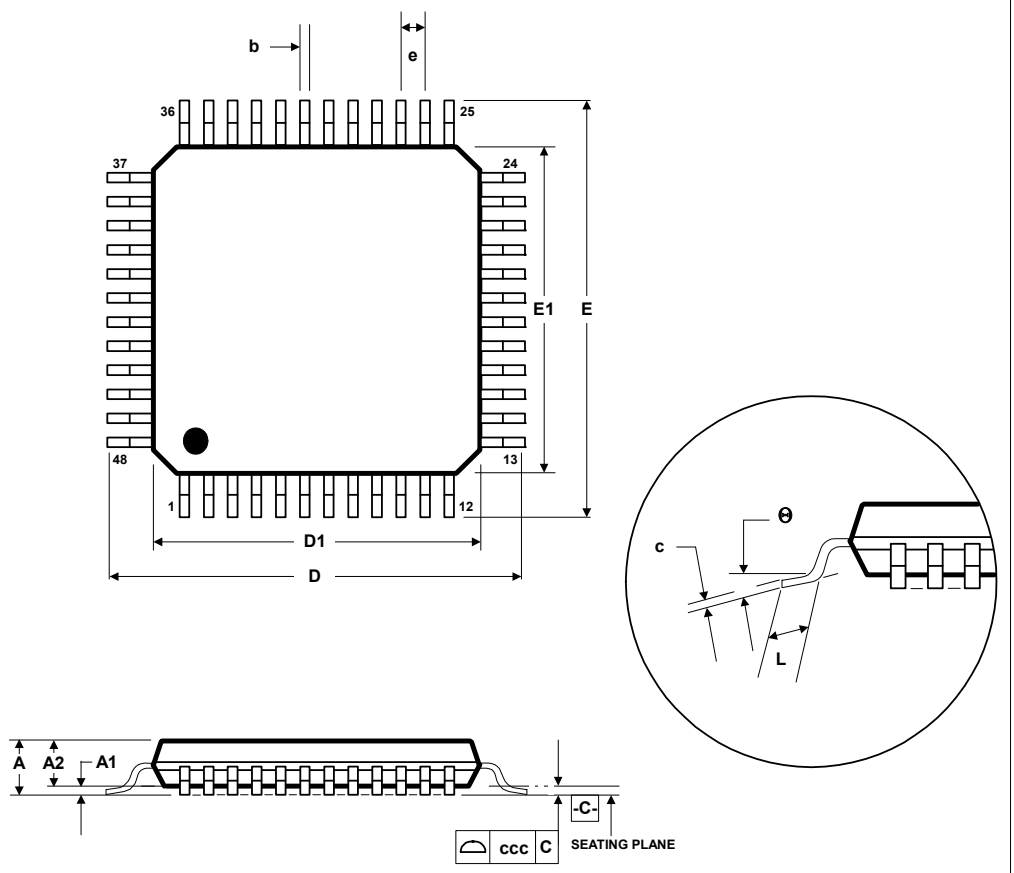
WAN0108 – Moisture Sensitivity Classification and Plastic IC Packaging

WAN0109 – ESD Damage in Integrated Circuits: Causes and Prevention

WAN0158 – Lead-Free Solder Profiles for Lead-Free Components

PACKAGE DIMENSIONS

FT: 48 PIN TQFP (7 x 7 x 1.0 mm) **DM004.C**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
Θ	0^o	3.5^o	7^o
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = ABC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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ADDRESS:

Wolfson Microelectronics plc

Westfield House

26 Westfield Road

Edinburgh

EH11 2QB

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com

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