280MHz, 2.9ns Comparator Family with Rail-to-Rail Inputs and CMOS Outputs

FEATURES

- **Very High Toggle Rate: 280MHz**
- **Low Propagation Delay: 2.9ns**
- Rail-to-Rail Inputs Extend Beyond Both Rails
- Output Current Capability: ±22mA
- Low Quiescent Current: 4.5mA
- Features within the LTC6752 Family:
  - 2.45V to 5.25V Input Supply and 1.71V to 3.5V Output Supply (Separate Supply Option)
  - 2.45V to 3.5V Supply (Single Supply Option)
  - Shutdown Pin for Reduced Power
  - Output Latch and Adjustable Hysteresis
  - Complementary Outputs
- Packages: TSOT-23, MSOP, 3mm × 3mm QFN
- Direct Replacement for ADCMP60X Family
- Operating Temperature Range: –40°C to 125°C

APPLICATIONS

- Clock and Data Recovery
- Level Shifting
- High Speed Data Acquisition Systems
- Window Comparators
- High Speed Line Receivers
- Fast Crystal Oscillators
- Time of Flight Measurements
- Time Domain Reflectometry

DESCRIPTION

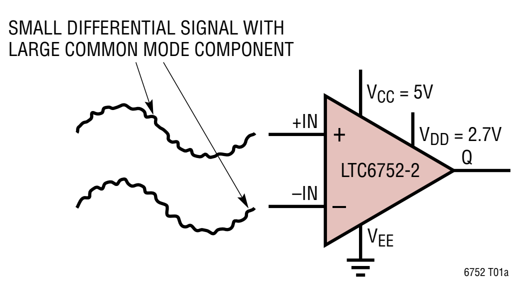
The LTC®6752 is a family of very high speed comparators capable of supporting toggle rates up to 280MHz. These comparators exhibit low propagation delays of 2.9ns, and fast rise/fall times of 1.2ns. There are a total of 3 members in the LTC6752 family, with different options for separate input and output supplies, shutdown, output latch, adjustable hysteresis, complementary outputs, and package.

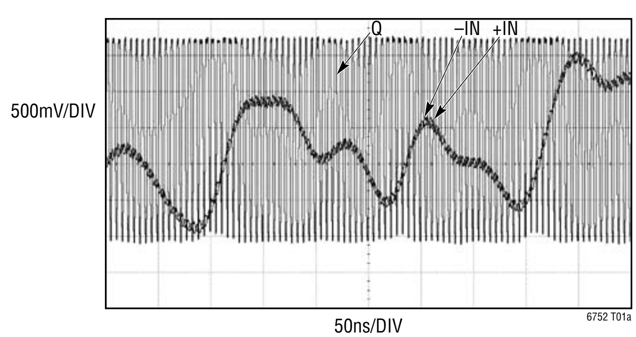
All of the LTC6752 comparators have rail-to-rail inputs that operate from 2.45V, up to 3.5V or 5.25V, depending on the option. The outputs are CMOS and the separate supply options can operate down to 1.71V

The low propagation delay of only 2.9ns combined with low dispersion of only 1.8ns (10mV to 125mV overdrive variation) makes these comparators an excellent choice for critical timing applications. Similarly, the fast toggle rate and the low jitter of 4.5ps RMS (100mV$_{P-P}$, 100MHz input) make the LTC6752 family ideally suited for high frequency line driver and clock recovery circuits.

TYPICAL APPLICATION

High Speed Differential Line Receiver with Excellent Common Mode Rejection





ABSOLUTE MAXIMUM RATINGS

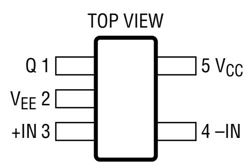
(Note 1)

Total Supply Voltage (V_{CC} to V_{EE})
(LTC6752-2/LTC6752-3) 5.5V
(LTC6752)..3.6V
Total Supply Voltage (V_{DD} to V_{EE})...........................3.6V
Input Current (+IN, –IN, $\overline{\text{SHDN}}$, $\overline{\text{LE}}$/HYST)
(Note 2)..±10mA
Output Current (Q, $\overline{\text{Q}}$) (Note 3)........................... ±50mA

Specified Temperature Range (Note 4)
LTC6752I ....–40°C to 85°C
LTC6752H ....–40°C to 125°C
Storage Temperature Range .... –65°C to 125°C
Maximum Junction Temperature (Note 3)............. 150°C
Lead Temperature Soldering (10s) ....300°C

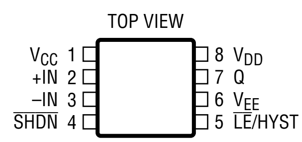
PIN CONFIGURATION

LTC6752



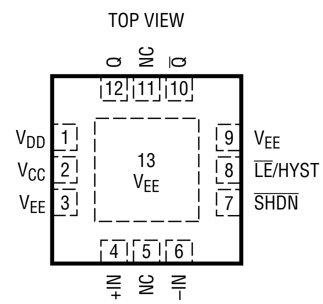
S5 PACKAGE
5-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 215°C/W (NOTE 3)

LTC6752-2



MS8 PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 163°C/W (NOTE 3)

LTC6752-3



UD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 68°C/W (NOTE 3)
EXPOSED PAD (PIN 13) IS V_{EE}, MUST BE SOLDERED TO PCB

Table 1. Features and Part Numbers

PART#	LATCHING/ADJUSTABLE HYSTERESIS	SEPARATE INPUT/ OUTPUT SUPPLIES	SHUTDOWN	COMPLEMENTARY OUTPUTS	PACKAGE OFFERING
LTC6752					TSOT-23-5
LTC6752-2	●	●	●		MS8
LTC6752-3	●	●	●	●	3mm × 3mm QFN

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6752IS5#TRMPBF	LTC6752IS5#TRPBF	LTGKT	5-Lead Plastic TSOT-23	–40°C to 85°C
LTC6752HS5#TRMPBF	LTC6752HS5#TRPBF	LTGKT	5-Lead Plastic TSOT-23	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6752IMS8-2#PBF	LTC6752IMS8-2#TRPBF	LTGKW	8-Lead Plastic MSOP	–40°C to 85°C
LTC6752HMS8-2#PBF	LTC6752HMS8-2#TRPBF	LTGKW	8-Lead Plastic MSOP	–40°C to 125°C
LTC6752IUD-3#PBF	LTC6752IUD-3#TRPBF	LGKV	12-Lead Plastic QFN (3mm × 3mm)	–40°C to 85°C
LTC6752HUD-3#PBF	LTC6752HUD-3#TRPBF	LGKV	12-Lead Plastic QFN (3mm × 3mm)	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5V, V_{DD} = 2.5V, V_{EE} = 0). The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, C_L = 5pF, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} - V_{EE}	Supply Voltage (Note 5)	LTC6752 (Total Supply) LTC6752-2/LTC6752-3 (Input Stage)	● ●	2.45 2.45		3.5 5.25	V V
V_{DD} - V_{EE}	Output Stage Supply Voltage (Note 5)	LTC6752-2/LTC6752-3	●	1.71		3.5	V
V_{CMR}	Input Voltage Range (Note 7)		●	V_{EE} – 0.2		V_{CC} + 0.1	V
V_{OS}	Input Offset Voltage (Note 6)		 ●	–5.5 –8.5	±1.2	5.5 8.5	mV mV
TCV_{OS}	Input Offset Voltage Drift		●		18		µV/°C
V_{HYST}	Input Hysteresis Voltage (Note 6)	$\overline{LE}$/HYST Pin Floating			5		mV
C_{IN}	Input Capacitance				1.1		pF
R_{DM}	Differential Mode Resistance				57		kΩ
R_{CM}	Common Mode Resistance				6.4		MΩ
I_B	Input Bias Current	V_{CM} = V_{EE} + 0.3V	 ●	–3.8 –4	–1.35		µA µA
		V_{CM} = V_{CC} – 0.3V	 ●		0.3	1.25 2.1	µA µA
I_{OS}	Input Offset Current		●	–0.75	±0.1	0.75	µA
CMRR_LVCM	Common Mode Input Range, Low V_{CM} Region	V_{EE} – 0.2V to V_{CC} – 1.5V	 ●	51 46	69		dB dB

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5V, V_{DD} = 2.5V, V_{EE} = 0). The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, C_L = 5pF, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR_FR	Common Mode Rejection Ratio (Measured at Extreme Ends of V_{CMR})	V_{CM} = V_{EE} – 0.2V to V_{CC} + 0.1V	 ●	50 45.5	65		dB dB
PSRR_V_{CC}	Input Power Supply Rejection Ratio	V_{CM} = 0.3V, V_{DD} = 2.5V, V_{CC} Varied from 2.45V to 5.25V (LTC6752-2/LTC6752-3)	 ●	59 57	74		dB dB
	Total Power Supply Rejection Ratio	V_{CM} = 0.3V, V_{CC} Varied from 2.45V to 3.5V (LTC6752)	 ●	53 51	73		dB dB
PSRR_V_{DD}	Output Power Supply Rejection Ratio	V_{CM} = 0.3V, V_{DD} Varied from 1.71V to 3.5V (LTC6752-2/LTC6752-3)	 ●	56 51	71		dB dB
A_{VOL}	Open Loop Gain	LTC6752-2/LTC6752-3, Hysteresis Removed (Note 12)			6000		V/V
V_{OH}	Output High Voltage (Amount Below V_{DD} (LTC6752-2/LTC5752-3), V_{CC} (LTC6752))	I_{SOURCE} = 8mA	 ●		130	260 340	mV mV
V_{OL}	Output Low Voltage (Referred to V_{EE})	I_{SINK} = 8mA	 ●		200	340 400	mV mV
I_{SC}	Output Short-Circuit Current	Source	 ●	16 12	30		mA mA
		Sink	 ●	15 9	22		mA mA
I_{VCC}	V_{CC} Supply Current, Device On	LTC6752	 ●		4.5	5.0 5.9	mA mA
		LTC6752-2/LTC6752-3	 ●		1.9	2.25 2.5	mA mA
I_{VDD}	V_{DD} Supply Current, Device On	LTC6752-2	 ●		2.6	3.2 3.4	mA mA
		LTC6752-3	 ●		4.3	4.75 5.2	mA mA
I_{TOTAL}	Total Supply Current, Device On	LTC6752/LTC6752-2	 ●		4.5	5.0 5.9	mA mA
		LTC6752-3	 ●		6.2	6.65 7.7	mA mA
t_R, t_F	Rise/Fall time	10% to 90%			1.2		ns
t_{PD}	Propagation Delay (Note 8)	$V_{OVERDRIVE}$ = 50mV	 ●		2.9	5 5.5	ns ns
t_{SKEW}	Propagation Delay Skew, Rising to Falling Transition (Note 9)				300		ps
t_{ODD}	Overdrive Dispersion (Note 8)	Overdrive Varied from 10mV to 125mV			1.8		ns
t_{CMD}	Common Mode Dispersion	V_{CM} Varied from V_{EE} – 0.2V to V_{CC} + 0.1V			240		ps
TR	Toggle Rate (Note 11)	100mV_{P-P} Input, LTC6752/LTC6752-2 100mV_{P-P} Input, LTC6752-3			280 250		MHz MHz
t_{JITTER}	RMS Jitter	V_{IN} = 100mV_{P-P}, f_{IN} = 100MHz, Jitter BW = 10Hz – 50MHz f_{IN} = 61.44MHz, Jitter BW = 10Hz – 30.72MHz f_{IN} = 10MHz, Jitter BW = 10Hz – 5MHz			 4.5 6.0 30		 ps ps ps
Latching/Adjustable Hysteresis Characteristics (LTC6752-1/LTC6752-2/LTC6752-3 Only)							
$V_{\overline{LE}/HYST}$	$\overline{LE}$/HYST Pin Voltage	Open Circuit		1.05	1.25	1.45	V
R_{HYST}	Resistance Looking Into $\overline{LE}$/HYST	$\overline{LE}$/HYST Pin Voltage < Open Circuit Value	●	15	20	25	kΩ
V_{HYST_LARGE}	Hysteresis Voltage	$V_{\overline{LE}/HYST}$ = 800mV			40		mV

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.5V, V_{DD} = 2.5V, V_{EE} = 0). The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, C_L = 5pF, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IL\_\overline{LE}}$	Latch Pin Voltage, Latch Guaranteed		●			0.3	V
$V_{IH\_\overline{LE}}$	Latch Pin Voltage, Hysteresis Disabled	Output Not Latched	●	1.7			V
$I_{IH\_\overline{LE}}$	Latch Pin Current High	$V_{\overline{LE}/HYST}$ = 1.7V	●		30	72	µA
$I_{IL\_\overline{LE}}$	Latch Pin Current Low	$V_{\overline{LE}/HYST}$ = 0.3V	●	–70	–47		µA
t_{SETUP}	Latch Setup Time (Note 10)				–2		ns
t_{HOLD}	Latch Hold Time (Note 10)				2		ns
t_{PL}	Latch to Output Delay				7		ns
Shutdown Characteristics (LTC6752-2/LTC6752-3 Only)							
I_{SD_VCC}	Shutdown Mode Input Stage Supply Current	$V_{\overline{SHDN}}$ = 0.6V	 ●		400	585 620	µA µA
I_{SD_VDD}	Shutdown Mode Output Stage Supply Current	$V_{\overline{SHDN}}$ = 0.6V, LTC6752-2	 ●		185	340 380	µA µA
		$V_{\overline{SHDN}}$ = 0.6V, LTC6752-3	 ●		250	650 680	µA µA
t_{SD}	Shutdown Time	Output Hi-Z			80		ns
V_{IH_SD}	Shutdown Pin Voltage High	Part Guaranteed to Be Powered On	●	1.3			V
V_{IL_SD}	Shutdown Pin Voltage Low	Part Guaranteed to Be Powered Off	●			0.6	V
t_{WAKEUP}	Wake-Up Time from Shutdown	V_{OD} = 100mV, Output Valid			100		ns

(V_{CC} = 3.3V, V_{DD} = 3.3V, V_{EE} = 0). The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, C_L = 5pF, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} - V_{EE}	Supply Voltage (Note 5)	LTC6752 (Total Supply) LTC6752-2/LTC6752-3 (Input Stage)	● ●	2.45 2.45		3.5 5.25	V V
V_{DD} - V_{EE}	Output Supply Voltage (Note 5)	LTC6752-2/LTC6752-3	●	1.71		3.5	V
V_{CMR}	Input Voltage Range (Note 7)		●	V_{EE} – 0.2		V_{CC} + 0.1	V
V_{OS}	Input Offset Voltage (Note 6)		 ●	–5.5 –9	±1.2	5.5 9	mV mV
TCV_{OS}	Input Offset Voltage Drift		●		18		µV/°C
V_{HYST}	Input Hysteresis Voltage (Note 6)	$\overline{LE}$/HYST Pin Floating			4.7		mV
C_{IN}	Input Capacitance				1.1		pF
R_{DM}	Differential Mode Resistance				57		kΩ
R_{CM}	Common Mode Resistance				6.4		MΩ
I_B	Input Bias Current	V_{CM} = V_{EE} + 0.3V	 ●	–3.8 –4.1	–1.4		µA µA
		V_{CM} = V_{CC} – 0.3V	 ●		0.33	1.5 2.3	µA µA
I_{OS}	Input Offset Current		●	–0.75	±0.1	0.75	µA
CMRR_LVCM	Common Mode Input Range, Low V_{CM} Region	V_{EE} – 0.2V to V_{CC} – 1.5V	 ●	52 48	70		dB dB
CMRR_FR	Common Mode Rejection Ratio (Measured at Extreme Ends of V_{CMR})	V_{CM} = V_{EE} – 0.2V to V_{CC} + 0.1V	 ●	50 46	66		dB dB

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V, V_{DD} = 3.3V, V_{EE} = 0). The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, C_L = 5pF, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$PSRR\_V_{CC}$	Input Power Supply Rejection Ratio Total Power Supply Rejection Ratio	V_{CM} = 0.3V, V_{DD} = 3.3V,V_{CC} Varied from 2.45V to 5.25V (LTC6752-2/LTC6752-3)	●	59 57	75		dB
		V_{CM} = 0.3V,V_{CC} Varied from 2.45V to 3.5V (LTC6752)	●	53 51	73		dB dB
$PSRR\_V_{DD}$	Output Power Supply Rejection Ratio	V_{CM} = 0.3V, V_{DD} Varied from 1.71V to 3.5V (LTC6752-2/LTC6752-3)	●	56 51	71		dB dB
A_{VOL}	Open Loop Gain	LTC6752-2/LTC6752-3,Hysteresis Removed (Note 12)			7000		V/V
V_{OH}	Output High Voltage (Amount Below V_{DD} (LTC6752-2/LTC5752-3), V_{CC} (LTC6752))	I_{SOURCE} = 8mA	●		81	200 300	mV mV
V_{OL}	Output Low Voltage (Referred to V_{EE})	I_{SINK} = 8mA	●		155	320 350	mV mV
I_{SC}	Output Short-Circuit Current	Source	●	35 30	70		mA mA
		Sink	●	20 15	39		mA mA
I_{VCC}	V_{CC} Supply Current, Device On	LTC6752	●		4.8	5.8 6.2	mA mA
		LTC6752-2/LTC6752-3	●		1.9	2.35 2.55	mA mA
I_{VDD}	V_{DD} Supply Current, Device On	LTC6752-2	●		2.9	3.45 3.65	mA mA
		LTC6752-3	●		4.75	5.35 5.75	mA mA
I_{TOTAL}	Total Supply Current, Device On	LTC6752/LTC6752-2	●		4.8	5.8 6.2	mA mA
		LTC6752-3	●		6.6	7.7 8.3	mA mA
t_R, t_F	Rise/Fall Time	10% to 90%			1.35		ns
t_{PD}	Propagation Delay (Note 8)	$V_{OVERDRIVE}$ = 50mV	●		3.00	5 5.5	ns ns
t_{SKEW}	Propagation Delay Skew, Rising to Falling Transition (Note 9)				600		ps
t_{ODD}	Overdrive Dispersion (Note 8)	Overdrive Varied from 10mV to 125mV			1.8		ns
t_{CMD}	Common Mode Dispersion	V_{CM} Varied from V_{EE}—0.2V to V_{CC} + 0.1V			240		ps
TR	Toggle Rate (Note 11)	100mV_{P-P} Input			215		MHz
t_{JITTER}	RMS jitter	V_{IN} = 100mV_{P-P}, f_{IN} = 100MHz, Jitter BW = 10Hz – 50MHz f_{IN} = 61.44MHz, Jitter BW = 10Hz – 30.72MHz f_{IN} = 10MHz, Jitter BW = 10Hz – 5MHz			4.8 5.8 29		ps ps ps

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V, V_{DD} = 3.3V, V_{EE} = 0). The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, C_L = 5pF, $V_{OVERDRIVE}$ = 50mV –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Latching/Adjustable Hysteresis Characteristics (LTC6752-1/LTC6752-2/LTC6752-3 Only)							
$V_{\overline{LE}/HYST}$	$\overline{LE}$/HYST Pin Voltage	Open Circuit	●	1.05	1.25	1.45	V
R_{HYST}	Resistance Looking Into $\overline{LE}$/HYST	$\overline{LE}$/HYST Pin Voltage < Open Circuit Value		15	20	25	kΩ
V_{HYST_LARGE}	Hysteresis Voltage	$V_{\overline{LE}/HYST}$ = 800mV			40		mV
$V_{IL\_\overline{LE}}$	Latch Pin Voltage, Latch Guaranteed		●			0.3	V
$V_{IH\_\overline{LE}}$	Latch Pin Voltage, Hysteresis Disabled	Output Not Latched	●	1.7			V
$I_{IH\_\overline{LE}}$	Latch Pin Current High	$V_{\overline{LE}/HYST}$ = 1.7V			30	72	µA
$I_{IL\_\overline{LE}}$	Latch Pin Current Low	$V_{\overline{LE}/HYST}$ = 0.3V		–70	–47		µA
t_{SETUP}	Latch Setup Time (Note 10)				–2		ns
t_{HOLD}	Latch Hold Time (Note 10)				2		ns
t_{PL}	Latch to Output Delay				7		ns
Shutdown Characteristics (LTC6752-2/LTC6752-3 Only)							
I_{SD_VCC}	Shutdown Mode Input Stage Supply Current	$V_{\overline{SHDN}}$ = 0.6V	 ●		430	600 660	µA µA
I_{SD_VDD}	Shutdown Mode Output Stage Supply Current	$V_{\overline{SHDN}}$ = 0.6V, LTC6752-2	 ●		200	420 450	µA µA
		$V_{\overline{SHDN}}$ = 0.6V, LTC6752-3	 ●		300	700 800	µA µA
t_{SD}	Shutdown Time	Output Hi-Z			80		ns
V_{IH_SD}	Shutdown Pin Voltage High	Part Guaranteed to Be Powered On	●	1.3			V
V_{IL_SD}	Shutdown Pin Voltage Low	Part Guaranteed to Be Powered Off	●			0.6	V
t_{WAKEUP}	Wake-Up Time from Shutdown	V_{OD} = 100mV, Output Valid			100		ns

(V_{CC} = 5V, V_{DD} = 1.8V, V_{EE} = 0, LTC6752-2/LTC6752-3 only). The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, C_L = 5pF, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} - V_{EE}	Input Supply Voltage (Note 5)		●	2.45		5.25	V
V_{DD} - V_{EE}	Output Supply Voltage (Note5)		●	1.71		3.5	V
V_{CMR}	Input Voltage Range (Note 7)		●	V_{EE} – 0.2		V_{CC} + 0.1	V
V_{OS}	Input Offset Voltage (Note 6)		 ●	–5.5 –9	±1.2	5.5 9	mV mV
TCV_{OS}	Input Offset Voltage Drift		●		14		µV/°C
V_{HYST}	Input Hysteresis Voltage (Note 6)	$\overline{LE}$/HYST Pin Floating			5.2		mV
C_{IN}	Input Capacitance				1.1		pF
R_{DM}	Differential Mode Resistance				57		kΩ
R_{CM}	Common Mode Resistance				6.4		MΩ
I_B	Input Bias Current	V_{CM} = V_{EE} + 0.3V	 ●	–3.9 –4.2	–1.5		µA µA
		V_{CM} = V_{CC} – 0.3V	 ●		0.36	1.6 2.5	µA µA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V_{DD} = 1.8V, V_{EE} = 0, LTC6752-2/LTC6752-3 only). The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, C_L = 5pF, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OS}	Input Offset Current		●	–0.9	±0.1	0.9	µA
CMRR_LVCM	Common Mode Input Range, Low V_{CM} Region	V_{EE} – 0.2V to V_{CC} – 1.5V	 ●	54 51	70		dB dB
CMRR_FR	Common Mode Rejection Ratio (Measured at Extreme Ends of V_{CMR})	V_{CM} = V_{EE} – 0.2V to V_{CC} + 0.1V	 ●	53 48	68		dB dB
PSRR_V_{CC}	Input Power Supply Rejection Ratio	V_{CM} = 0.3V, V_{DD} = 1.8V,V_{CC} Varied from 2.45V to 5.25V	 ●	59 57	75		dB
PSRR_V_{DD}	Output Power Supply Rejection Ratio	V_{CM} = 0.3V, V_{DD} Varied from 1.71V to 3.5V	 ●	57 51	71		dB dB
A_{VOL}	Open Loop Gain	Hysteresis Removed (Note 12)			3500		V/V
V_{OH}	Output High Voltage (Amount Below V_{DD})	I_{SOURCE} = 5.5mA	 ●		200	400 450	mV mV
V_{OL}	Output Low Voltage (Referred to V_{EE})	I_{SINK} = 5.5mA	 ●		200	400 550	mV mV
I_{SC}	Output Short-Circuit Current	Source	 ●	9 6.2	17		mA mA
		Sink	 ●	11 6.2	19		mA mA
I_{VCC}	V_{CC} Supply Current, Device On		 ●		2.1	2.65 2.85	mA mA
I_{VDD}	V_{DD} Supply Current, Device On	LTC6752-2	 ●		2.5	3 3.25	mA mA
		LTC6752-3	 ●		3.4	4.4 4.8	mA mA
I_{TOTAL}	Total Supply Current, Device On	LTC6752-2	 ●		4.5	5.65 6.1	mA mA
		LTC6752-3	 ●		6	7.05 7.65	mA mA
t_R, t_F	Rise/Fall Time	10% to 90%			1.25		ns
t_{PD}	Propagation Delay (Note 8)	$V_{OVERDRIVE}$ = 50mV	 ●		3.4	5.3 5.7	ns ns
t_{SKEW}	Propagation Delay Skew, Rising to Falling Transition (Note 9)				400		ps
t_{ODD}	Overdrive Dispersion (Note 8)	Overdrive Varied from 10mV to 125mV			1.8		ns
t_{CMD}	Common Mode Dispersion	V_{CM} Varied from V_{EE} – 0.2V to V_{CC} + 0.1V			240		ps
TR	Toggle Rate (Note 11)	100mV$_{P-P}$ Input, LTC6752-2 100mV$_{P-P}$ Input, LTC6752-3			230 185		MHz MHz
t_{JITTER}	RMS Jitter	V_{IN} = 100mV$_{P-P}$, f_{IN} = 100MHz, Jitter BW = 10Hz – 50MHz f_{IN} = 61.44MHz, Jitter BW = 10Hz – 30.72MHz f_{IN} = 10MHz, Jitter BW = 10Hz – 5MHz			4.3 5.8 28		ps ps ps

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{DD} = 1.8V, V_{EE} = 0, LTC6752-2/LTC6752-3 only).

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at T_A = 25°C. $\overline{LE}$/HYST, $\overline{SHDN}$ pins floating, C_L = 5pF, $V_{OVERDRIVE}$ = 50mV, –IN = V_{CM} = 300mV, +IN = –IN + $V_{OVERDRIVE}$, 150mV step size unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Latching/Adjustable Hysteresis Characteristics (LTC6752-2/LTC6752-3 Only)							
$V_{\overline{LE}/HYST}$	$\overline{LE}$/HYST Pin Voltage	Open Circuit		1.05	1.25	1.45	V
R_{HYST}	Resistance Looking Into $\overline{LE}$/HYST	$\overline{LE}$/HYST Pin Voltage < Open Circuit Value		15	20	25	kΩ
V_{HYST_LARGE}	Modified Input Hysteresis Voltage (Note 2)	$V_{\overline{LE}/HYST}$ = 800mV			40		mV
$V_{IL\_\overline{LE}}$	Latch Pin Voltage, Latch Guaranteed		●			0.3	V
$V_{IH\_\overline{LE}}$	Latch Pin Voltage, Hysteresis Disabled	Output Not Latched	●	1.7			V
$I_{IH\_\overline{LE}}$	Latch Pin Current High	$V_{\overline{LE}/HYST}$ = 1.7V			30	72	µA
$I_{IL\_\overline{LE}}$	Latch Pin Current Low	$V_{\overline{LE}/HYST}$ = 0.3V		–70	–47		µA
t_{SETUP}	Latch Setup Time (Note 10)				–2		ns
t_{HOLD}	Latch Hold Time (Note 10)				2		ns
t_{PL}	Latch To Output Delay				7		ns
Shutdown Characteristics							
I_{SD_VCC}	Shutdown Mode Input Stage Supply Current	$V_{\overline{SHDN}}$ = 0.6V	 ●		500	650 750	µA µA
I_{SD_VDD}	Shutdown Mode Output Stage Supply Current	$V_{\overline{SHDN}}$ = 0.6V, LTC6752-2	 ●		170	400 450	µA µA
		$V_{\overline{SHDN}}$ = 0.6V, LTC6752-3	 ●		240	600 650	µA µA
t_{SD}	Shutdown Time	Output Hi-Z			80		ns
V_{IH_SD}	Shutdown Pin Voltage High	Part Guaranteed to Be Powered On	●	1.3			V
V_{IL_SD}	Shutdown Pin Voltage Low	Part Guaranteed to Be Powered Off	●			0.6	V
t_{WAKEUP}	Wake-Up Time from Shutdown	V_{OD} = 100mV, Output Valid			100		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Reverse biased ESD protection diodes exist on all input, shutdown, latching/hysteresis and output pins. If the voltage on these pins goes 300mV beyond either supply rail, the current should be limited to less than 10mA. This parameter is guaranteed to meet specification through design and/or characterization. It is not production tested.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating. This parameter is guaranteed to meet specified performance through design and/or characterization. It is not production tested.

Note 4: The LTC6752I/LTC6752-2I/LTC6752-3I are guaranteed to meet specified performance from –40°C to 85°C. The LTC6752H/LTC6752-2H/LTC6752-3H are guaranteed to meet specified performance from –40°C to 125°C.

Note 5: Total output supply voltage range is guaranteed by the PSRR_V_{DD} test. Total input supply voltage range for the LTC6752-2 and LTC6752-3 is guaranteed by the PSRR_V_{CC} test. For the LTC6752, the supply voltage range is guaranteed by the PSRR_V_{CC} test.

Note 6: Both hysteresis and offset are measured by determining positive and negative trip points (input values needed to change the output in the opposite direction). Hysteresis is defined as the difference of the two trip points and offset as the average of the two trip points.

Note 7: Guaranteed by CMRR test.

Note 8: Propagation delays are measured with a step size of 150mV.

Note 9: Propagation delay skew is defined as the difference of the propagation delays for positive and negative steps for the LTC6752 and LTC6752-2, and the difference in propagation delays between the complementary outputs for the LTC6752-3.

Note 10: Latch setup time is defined as the minimum time before the $\overline{LE}$/HYST pin is asserted low for an input signal change to be acquired and held at the output. Latch hold time is defined as the minimum time before an input signal change for a high to low transition on the $\overline{LE}$/HYST pin to prevent the output from changing. See Figure 7 for a graphical definition of these terms.

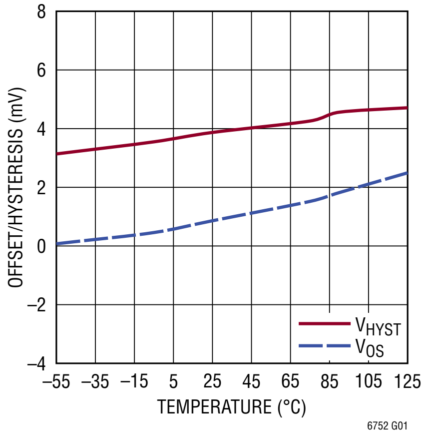
Note 11: Toggling is defined to be valid if the output swings as follows: from 10% of V_{DD} - V_{EE} to 90% of V_{DD} - V_{EE} for the LTC6752-2/LTC6752-3, and from 10% of V_{CC} - V_{EE} to 90% of V_{CC} - V_{EE} for the LTC6752. It is tested with a 1kΩ load to V_{CM}

Note 12: The devices have effectively infinite gain when hysteresis is enabled.

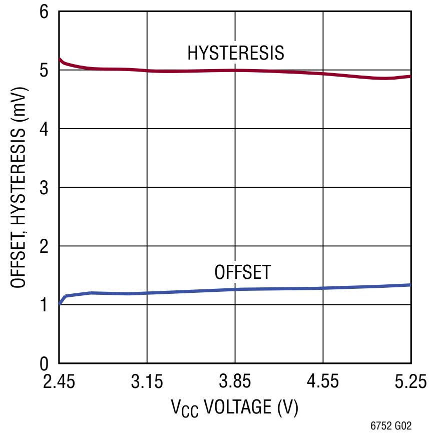
TYPICAL PERFORMANCE CHARACTERISTICS DC

$V_{CC} = V_{DD} = 2.5V$, $C_{LOAD} = 5pF$, $V_{OVERDRIVE} = 50mV$, $V_{CM} = 300mV$, $T_A = 25°C$ unless otherwise noted. $V_{CC} \neq V_{DD}$ conditions applicable only to the LTC6752-2/ LTC6752-3.

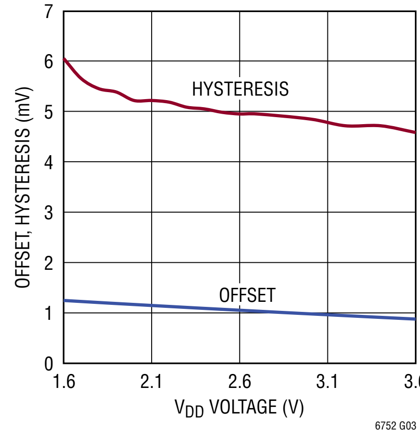
Input Offset Voltage and Hysteresis vs Temperature



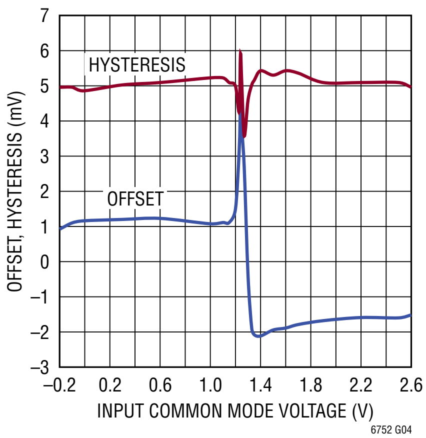
Input Offset Voltage and Hysteresis vs V_{CC} Voltage



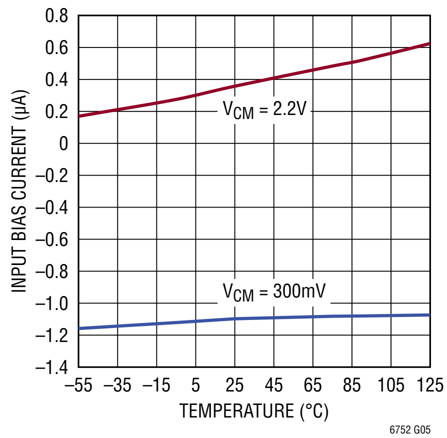
Input Offset Voltage and Hysteresis vs V_{DD} Voltage



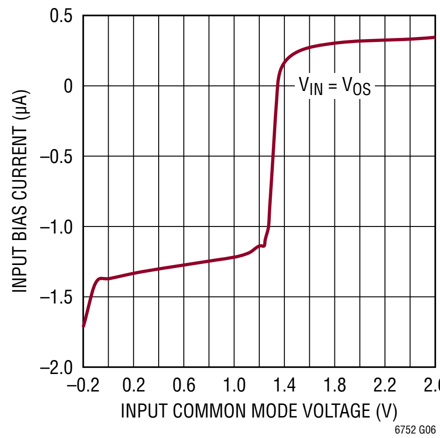
Input Offset Voltage and Hysteresis vs Input Common Mode



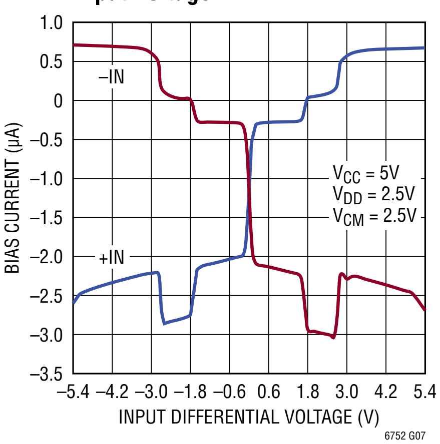
Input Bias Current vs Temperature



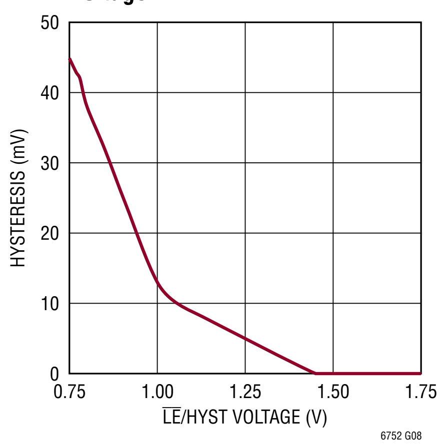
Input Bias Current vs Common Mode Voltage



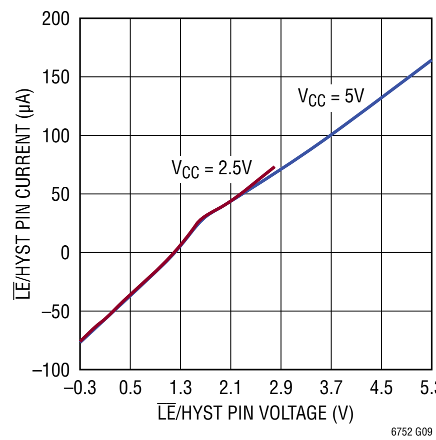
Input Bias Current vs Differential Input Voltage



Input Hysteresis vs $\overline{LE}$/HYST Pin Voltage



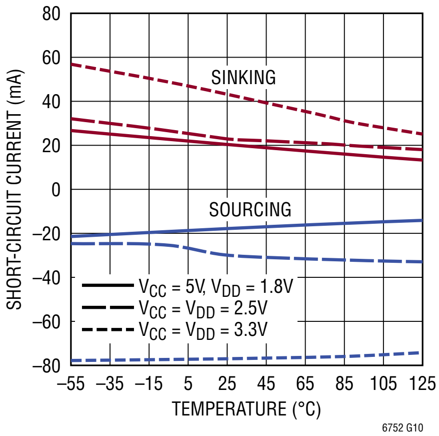
$\overline{LE}$/HYST Pin I-V Characteristics



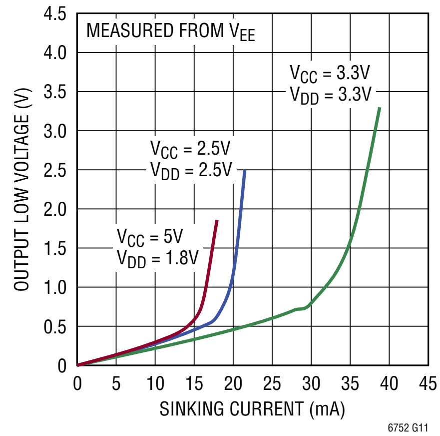
TYPICAL PERFORMANCE CHARACTERISTICS DC

$V_{CC} = V_{DD} = 2.5V$, $C_{LOAD} = 5pF$, $V_{OVERDRIVE} = 50mV$, $V_{CM} = 300mV$, $T_A = 25°C$ unless otherwise noted. $V_{CC} \neq V_{DD}$ conditions applicable only to the LTC6752-2/ LTC6752-3.

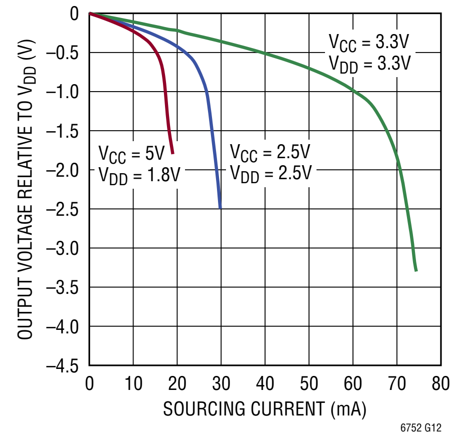
Output Short-Circuit Current vs Temperature



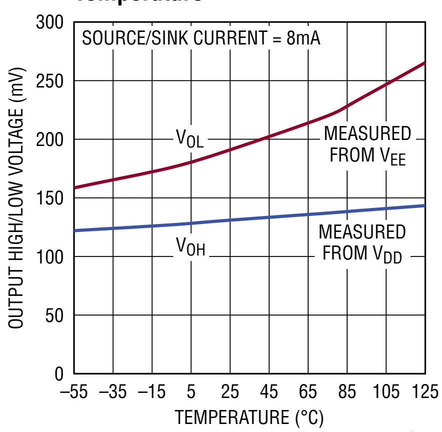
Output Low Voltage vs Load Current



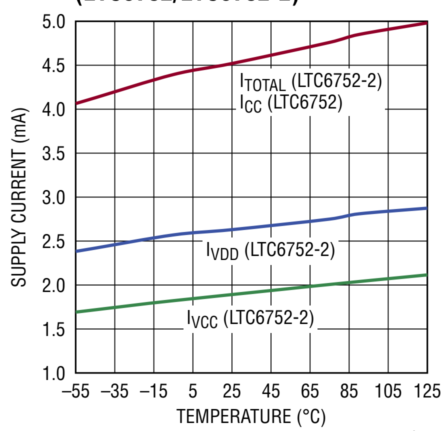
Output High Voltage vs Sourcing Current



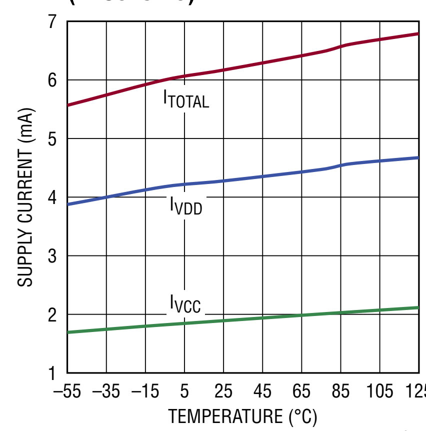
Output High/Low Voltage vs Temperature



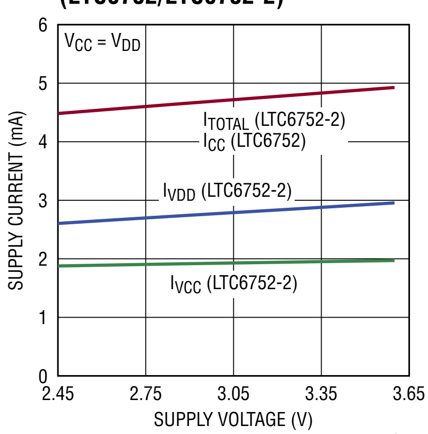
Supply Current vs Temperature (LTC6752/LTC6752-2)



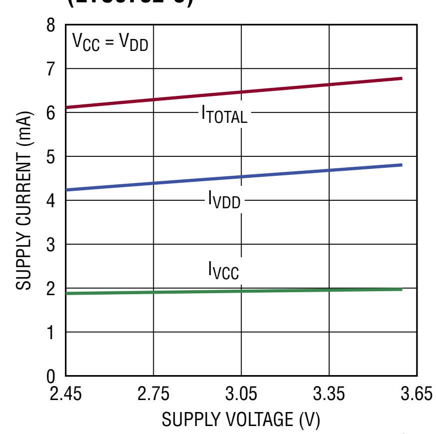
Supply Current vs Temperature (LTC6752-3)



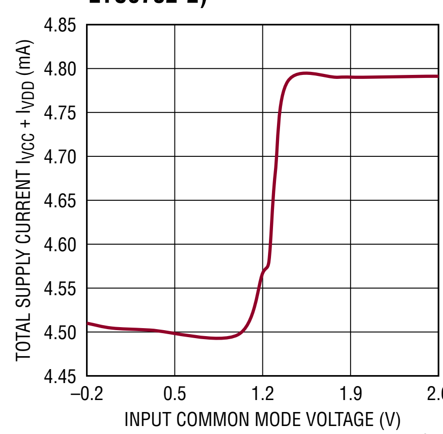
Supply Current vs Supply Voltage (LTC6752/LTC6752-2)



Supply Current vs Supply Voltage (LTC6752-3)



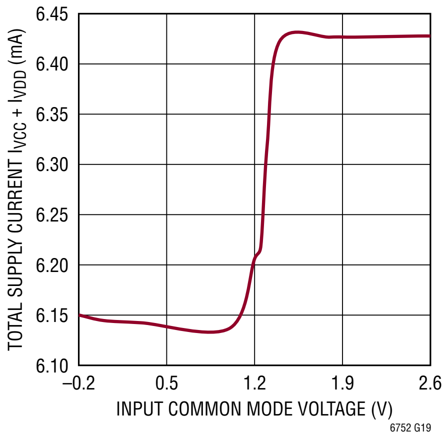
Supply Current vs Input Common Mode Voltage (LTC6752/ LTC6752-2)



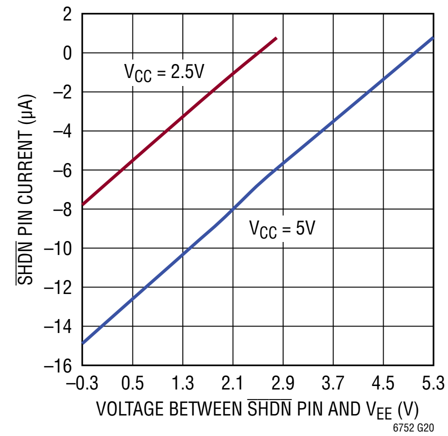
TYPICAL PERFORMANCE CHARACTERISTICS DC

$V_{CC} = V_{DD} = 2.5V$, $C_{LOAD} = 5pF$, $V_{OVERDRIVE} = 50mV$, $V_{CM} = 300mV$, $T_A = 25°C$ unless otherwise noted. $V_{CC} \neq V_{DD}$ conditions applicable only to the LTC6752-2/ LTC6752-3.

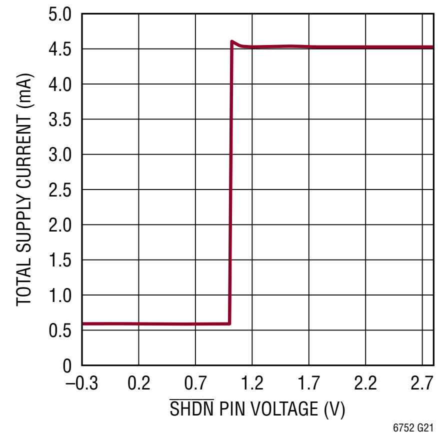
Supply Current vs Input Common Mode Voltage (LTC6752-3)



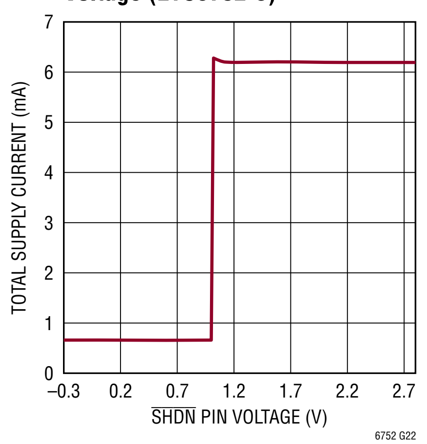
SHDN Pin I-V Characteristics



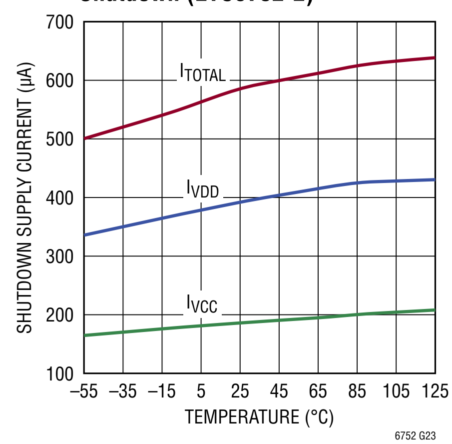
Total Supply Current vs SHDN Pin Voltage (LTC6752/LTC6752-2)



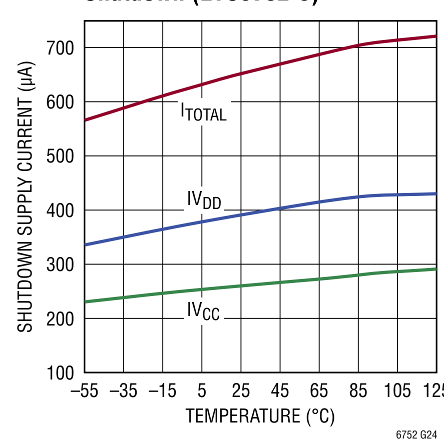
Total Supply Current vs SHDN Pin Voltage (LTC6752-3)



Supply Current vs Temperature, Shutdown (LTC6752-2)



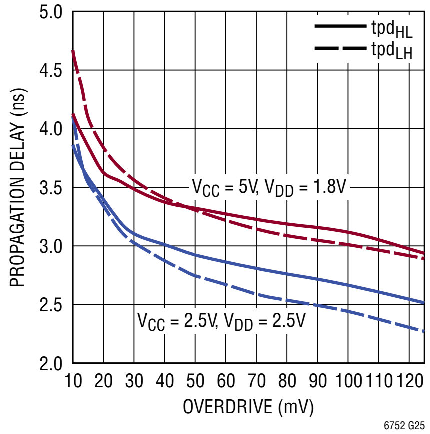
Supply Current vs Temperature, Shutdown (LTC6752-3)



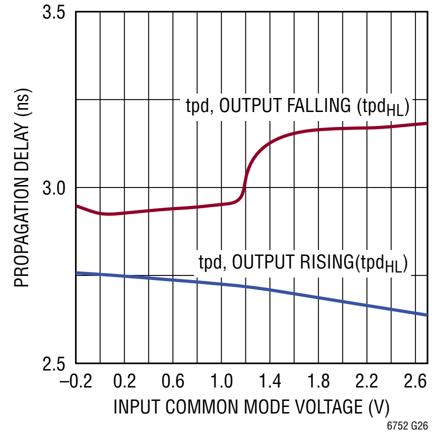
TYPICAL PERFORMANCE CHARACTERISTICS AC

$V_{CC} = V_{DD} = 2.5V$, $C_{LOAD} = 5pF$, $V_{OVERDRIVE} = 50mV$, $V_{CM} = 300mV$, $T_A = 25°C$, transient input voltage 10MHz, $150mV_{P-P}$ square wave unless otherwise noted. $V_{CC} \neq V_{DD}$ conditions applicable only to the LTC6752-2/ LTC6752-3.

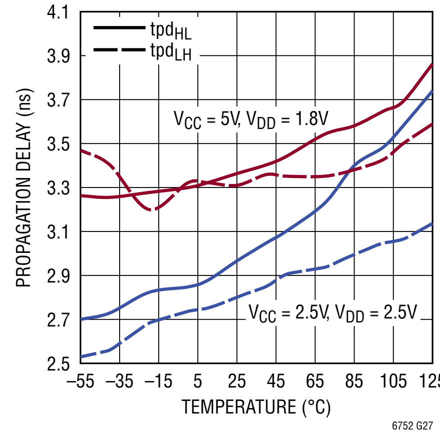
Propagation Delay vs Input Overdrive



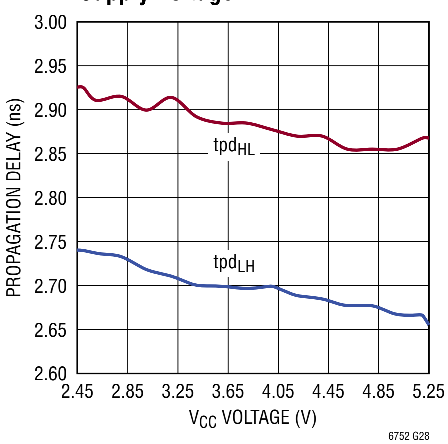
Propagation Delay vs Common Mode Voltage



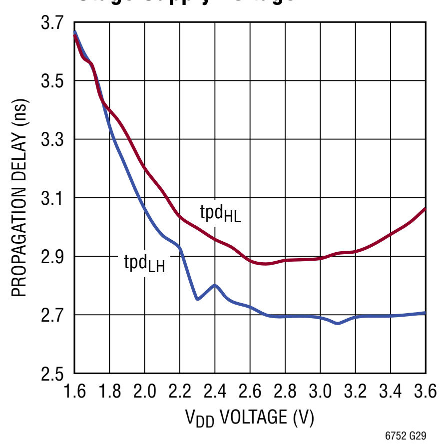
Propagation Delay vs Temperature



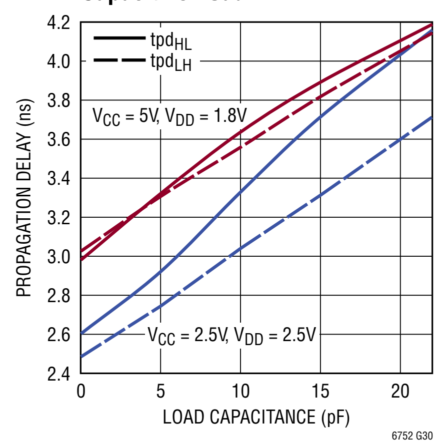
Propagation Delay vs Input Stage Supply Voltage



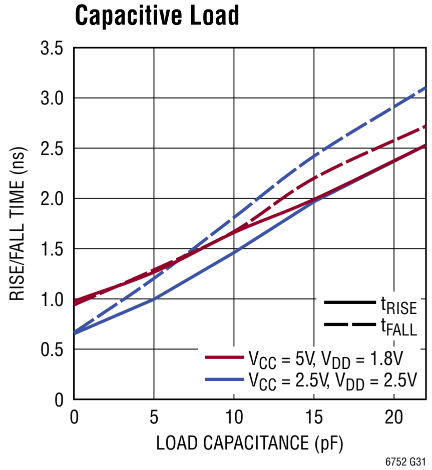
Propagation Delay vs Output Stage Supply Voltage



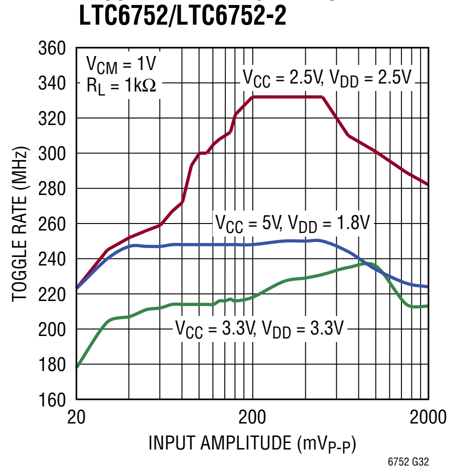
Propagation Delay vs Capacitive Load



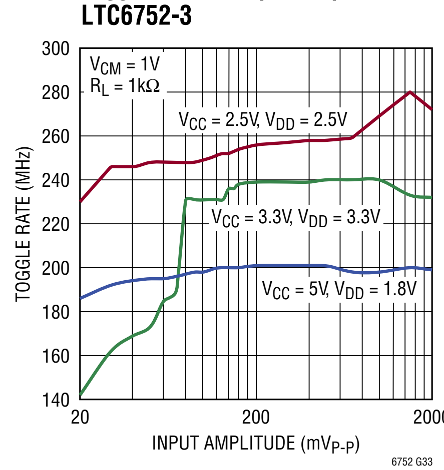
Rise/Fall times vs Capacitive Load



Toggle Rate vs Input Amplitude, LTC6752/LTC6752-2

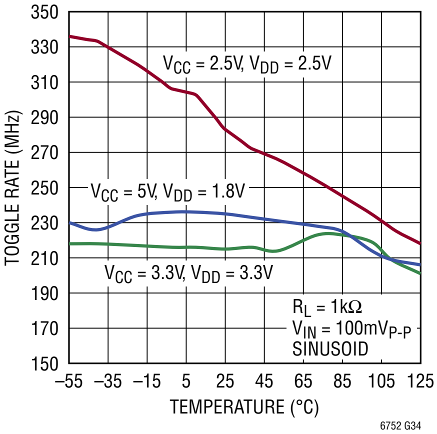


Toggle Rate vs Input Amplitude, LTC6752-3

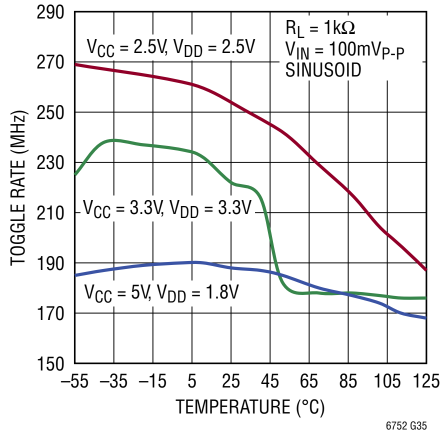


TYPICAL PERFORMANCE CHARACTERISTICS AC $V_{CC} = V_{DD} = 2.5V$, $C_{LOAD} = 5pF$, $V_{OVERDRIVE} = 50mV$, $V_{CM} = 300mV$, $T_A = 25°C$, transient input voltage 10MHz, $150mV_{P-P}$ square wave unless otherwise noted. $V_{CC} \neq V_{DD}$ conditions applicable only to the LTC6752-2/ LTC6752-3.

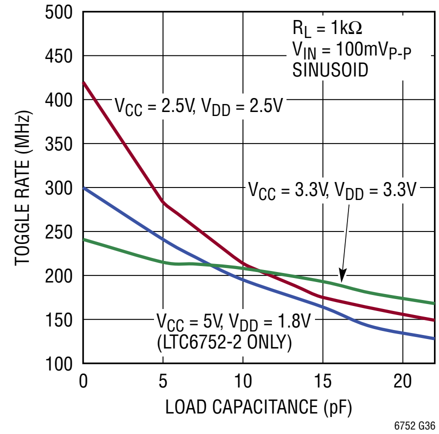
Toggle Rate vs Temperature, (LTC6752/LTC6752-2)



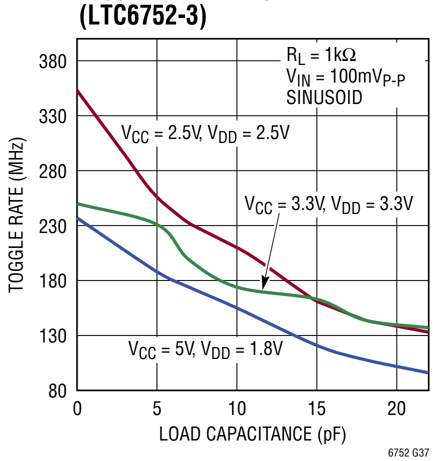
Toggle Rate vs Temperature, (LTC6752-3)



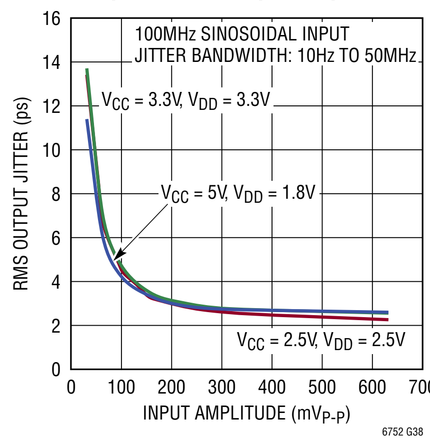
Toggle Rate vs Capacitive Load, (LTC6752/LTC6752-2)



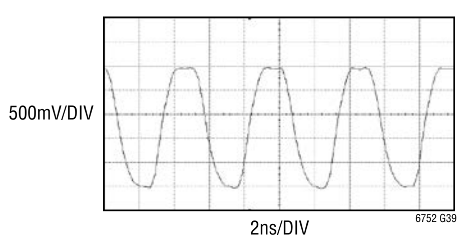
Toggle Rate vs Capacitive Load, (LTC6752-3)



Output Jitter vs Input Amplitude

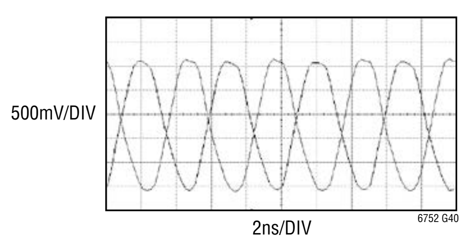


Output Toggle Waveform, LTC6752-2



LTC6752-2
$V_{CC} = V_{DD} = 2.5V$
$C_L = 5pF$
200MHz

Output Toggle Waveforms Q and $\overline{Q}$, LTC6752-3



LTC6752-3
$V_{CC} = V_{DD} = 2.5V$
$C_L = 5pF$
200MHz

PIN FUNCTIONS

+IN: Positive Input of the Comparator. The voltage range of this pin can go from V_{EE} to V_{CC}.

–IN: Negative Input of the Comparator. The voltage range of this pin can go from V_{EE} to V_{CC}.

V_{CC}: Positive Supply Voltage for the LTC6752, Positive Supply Voltage for the Input Stage of the LTC6752-2/LTC6752-3.

V_{DD}: Positive Supply Voltage for the Output Stage of the LTC6752-2/LTC6752-3. Typically the voltage is from 1.71V to 3.5V. See the section High Speed Board Design Techniques for proper power supply layout and bypassing.

V_{EE}: Negative power supply, normally tied to ground. This can be tied to a voltage other than ground as long as the constraints for total supply voltage relative to V_{CC} (and V_{DD} for separate supply operation) are maintained.

$\overline{\text{SHDN}}$: Active low comparator shutdown, threshold is 0.6V above V_{EE}. The comparator is enabled when this pin is left unconnected.

$\overline{\text{LE}}$/HYST: This pin allows the user to adjust the comparator's hysteresis as well as latch the output state if the pin voltage is taken within 300mV above V_{EE}. Hysteresis can be increased or disabled by voltage, current or a resistor to V_{EE}. Leaving the pin unconnected results in a typical hysteresis of 5mV.

Q: Comparator Output. Q is driven high when +IN > –IN and driven low when +IN < –IN.

$\overline{\text{Q}}$: Comparator Complementary Output (Available on LTC6752-3 Only). Logical inversion of Q.

BLOCK DIAGRAM

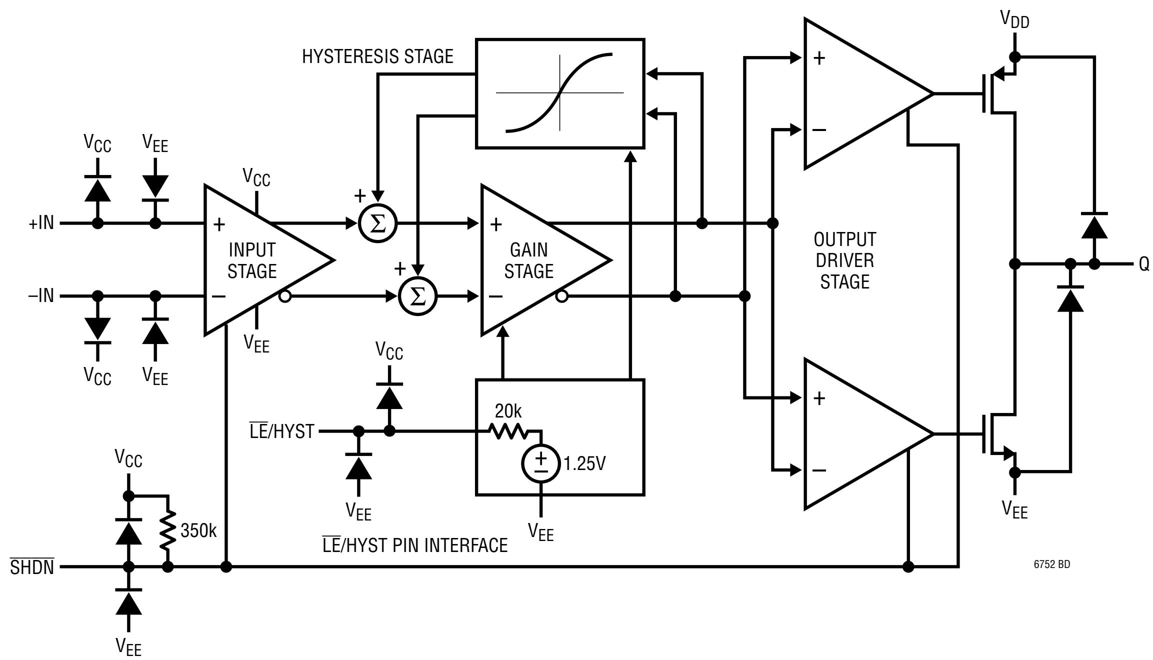


Figure 1. LTC6752/LTC6752-2 Block Diagram

APPLICATIONS INFORMATION

Circuit Description

The block diagram is shown in Figure 1. There are differential inputs (+IN, –IN), a negative power supply (V_{EE}), two positive supply pins: V_{CC} for the input stage and V_{DD} for the output stage, an output pin (Q), a pin for latching and adjusting hysteresis ($\overline{LE}$/HYST), and a pin to put the device in a low power mode ($\overline{SHDN}$). In the LTC6752, the two positive supply pins are bonded together and referred to as V_{CC}. The signal path consists of a rail-to-rail input stage, an intermediate gain stage, and an output stage driving a pair of complementary FETs capable of taking the output pin to either supply rail. A Latching/Hysteresis interface block allows the user to latch the output state and/or remove or adjust the comparator input hysteresis. All of the internal signal paths make use of low voltage swings for high speed at low power.

The LTC6752-3 has an additional inverted output stage (not shown) for a complementary logic output signal.

Power Supply Configurations

The LTC6752-2/LTC6752-3 have separate positive supply pins for the input and output stages that allow for separate voltage ranges for the analog input, and the output logic. Figure 2 shows a few possible configurations. For reliable and proper operation, the input supply pin should be between 2.45V and 5.25V above the negative supply pin, and the output supply pin should be between 1.71V and 3.5V above the negative supply pin. There are no restrictions regarding the sequence in which the supplies are applied, as long as the absolute-maximum ratings are not violated.

The LTC6752 has only one positive supply pin. The supply voltage should be between 2.45V and 3.5V for proper and reliable operation.

Input Voltage Range and Offset

The LTC6752 family uses a rail-to-rail input stage that consists of a pnp pair and an npn pair that are active over different input common mode ranges. The pnp pair is active for inputs between V_{EE} – 0.2V and approximately V_{CC} – 1.5V (low common mode region of operation). The npn pair is active for inputs between approximately V_{CC} – 1V and V_{CC} + 0.1V (high common mode region of operation). Partial activation of both pairs occurs when one input is in the low common mode region of operation and the other input is in the high common mode region of operation, or either of the inputs is between approximately V_{CC} – 1.5V and V_{CC} – 1V (transition region). The device has small, trimmed offsets as long as both inputs are completely in the low or high common mode region of operation. In the transition region, the offset voltage may increase. Applications that require good DC precision should avoid the transition region.

Input Bias Current

When both inputs are in the low common mode region, the input bias current is negative, with current flowing out of the input pins. When both inputs are in the high common mode region, the input bias current is positive, with current flowing into the input pins.

The input stage has been designed to accommodate large differential input voltages without large increases in input bias current. With one input at the positive input supply rail and the other input at the negative supply rail, the magnitude of the input bias currents at either pin is typically less than 3.5µA.

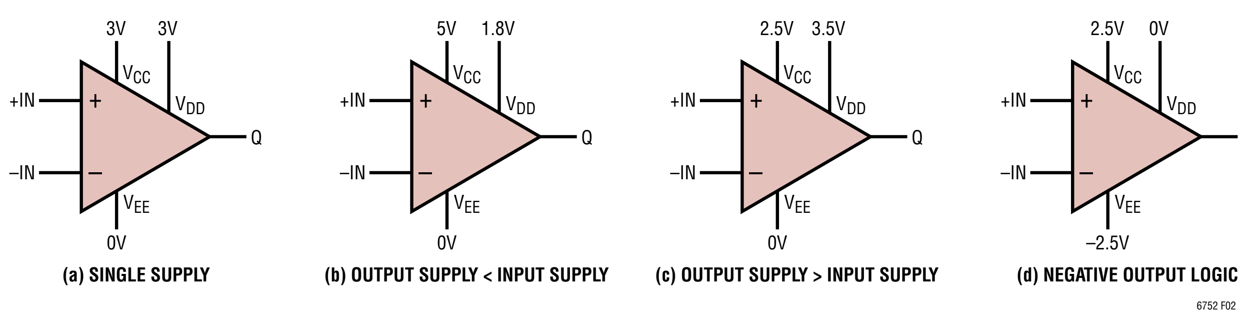


Figure 2. Typical Power Supply Configurations (Applicable to the LTC6752-2/LTC6752-3)

APPLICATIONS INFORMATION

Input Protection

The input stage is protected against damage from conditions where the voltage on either pin exceeds the supply voltage (V_{CC} to V_{EE}) without external protection. External input protection circuitry is only needed if input currents can exceed the absolute maximum rating. For example, if an input is taken beyond 300mV of either the positive or negative supply, an internal ESD protection diode will conduct and an external resistor should be used to limit the current to less than 10mA.

Outputs

The LTC6752 family has excellent drive capability. The comparators can deliver typically ±22mA output current for an output supply of 2.5V, and ±39mA output current for a 3.3V output supply. Attention must be paid to keep the junction temperature of the IC below 150°C should the output have a continuous short-circuit condition.

Logic Drive Capability

The LTC6752 family has been designed to drive CMOS logic with a supply of 3.3V, 2.5V and 1.8V. For device reliability, the output power supply (V_{DD}) should not be higher than 3.6V above the negative supply. When V_{DD} is 3V or higher the CMOS outputs of the LTC6752 family provide valid TTL logic threshold levels and can easily interface with TTL logic devices operating with a 5V supply. This is possible because all of the threshold levels associated with TTL logic (V_{IH}/V_{IL}/V_{OH}/V_{OL}) are less than or equal to 2.4V

Capacitive Loads

The LTC6752 family can drive capacitive loads. Transient performance parameters in the Electrical Characteristics Tables and Typical Characteristics section are for a load of 5pF, corresponding to a standard TTL/CMOS load. The devices are fully functional for larger capacitive loads, however speed performance will degrade. The graphs titled Propagation Delay vs Capacitive Load and Toggle Rate vs Capacitive Load illustrate the impact of changes to the total capacitive load. For optimal speed performance, output load capacitance should be reduced as much as possible.

ESD

The LTC6752 family members have reverse-biased ESD protection diodes on pins as shown in Figure 1.

There are additional clamps between the positive and negative supplies that further protect the device during ESD strikes. Hot-plugging of the device into a powered socket is not recommended since this can trigger the clamp resulting in large currents flowing between the supply pins.

Hysteresis

Comparators have very high open-loop gain. With slow input signals that are close to each other, input noise can cause the output voltage to switch randomly. This can be addressed by hysteresis which is positive feedback that increases the trip point in the direction of the input signal transition when the output switches. This pulls the inputs away from each other, and prevents continuous switching back and forth. The addition of positive feedback also has the effect of making the small signal gain infinite around the trip points. Hysteresis is designed into most comparators and the LTC6752 family has adjustable hysteresis with a default hysteresis of 5mV.

The input-output transfer characteristic is illustrated in Figure 3 showing the definitions of V_{OS} and HYST based upon the two measurable trip points.

In some cases, additional noise immunity is required above what is provided by the nominal 5mV hysteresis. Conversely, when processing small or fast differential signals,

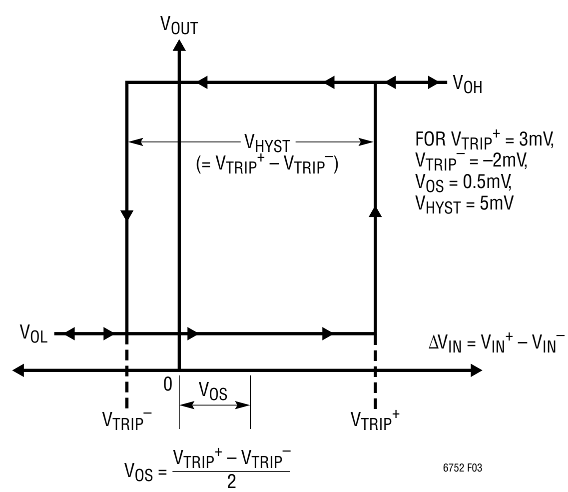


Figure 3

APPLICATIONS INFORMATION

hysteresis may need to be eliminated. The LTC6752-2/LTC6752-3 provide a hysteresis pin, $\overline{\text{LE}}$/HYST, that can be used to increase the internal hysteresis, completely remove it, or enable the output to latch. For these 2 options of the LTC6752, the internal hysteresis is disabled when the $\overline{\text{LE}}$/HYST pin voltage is above 1.7V. Although eliminating hysteresis does reduce the voltage gain of the comparator to a finite value, in many cases it will be high enough (typically 6000V/V) to process small input signals. The output will latch when the $\overline{\text{LE}}$/HYST pin voltage is below 0.3V. The internal hysteresis will increase as the voltage of the pin is adjusted from its default open circuit value of 1.25V to 800mV.

The $\overline{\text{LE}}$/HYST pin can be modeled as a 1.25V voltage source in series with a 20k resistor. The simplest method to increase the internal hysteresis is to connect a single resistor as shown in Figure 4 between the $\overline{\text{LE}}$/HYST pin and V_{EE} to adjust hysteresis. Figure 5 shows how hysteresis typically varies with the value of the resistor.

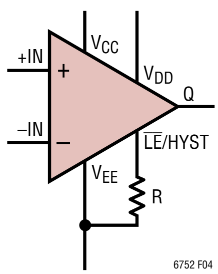


Figure 4. Adjusting Hysteresis Using an External Resistor at the $\overline{\text{LE}}$/HYST Pin

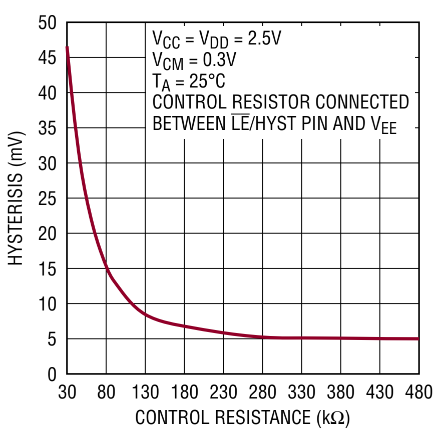


Figure 5. Hysteresis vs Control Resistor

In addition to adjusting hysteresis using the $\overline{\text{LE}}$/HYST pin, additional hysteresis can be added using positive feedback from the output back to the positive input, as shown in Figure 6.

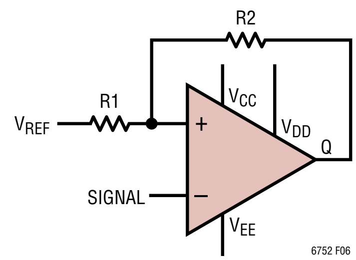


Figure 6. Additional Hysteresis Using Positive Feedback

The offset (with respect to the input signal) and hysteresis become

$$V_{OS\_FB} = \frac{(V_{DD}+V_{EE})}{2}\frac{R1}{R1+R2} + V_{REF}\frac{R2}{R1+R2} - V_{OS} - \frac{V_{OH}}{2}\frac{R1}{R1+R2} + V_{OL}\frac{R2}{R1+R2} \longrightarrow (1)$$

$$V_{HYST\_FB} = (V_{DD}-V_{EE})\frac{R1}{R1+R2} + V_{OL}\frac{R2}{R1+R2} + V_{OH}\frac{R1}{R1+R2} + V_{HYST} \longrightarrow (2)$$

V_{OS_FB} and V_{HYST_FB} denote the values of offset and hysteresis with positive feedback present. V_{HYST} denotes the hysteresis of the device without positive feedback. For light loads, V_{OH} (output swing high) and V_{OL} (output swing low) are typically a few mV (typically are less than 10mV for a 500µA load).

On a 3.0V total supply with V_{EE} = 0V, an increase in hysteresis of approximately 300mV can be obtained with V_{REF} = 1.25V, R2 = 4.53kΩ , R1 = 511Ω, with an induced offset of approximately 1.275V.

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Latching

The internal latch of the LTC6752-2/LTC6752-3 retains the output state when the $\overline{\text{LE}}$/HYST pin is taken to less than 300mV above the negative supply.

Figures 7a to 7e illustrate the latch timing definitions. The latch setup time is defined as the time for which the input should be stable before the latch pin is asserted low to ensure that the correct state will be held at the output. The latch hold time is the interval after which the latch pin is asserted in which the input signal must remain stable for the output to be the correct state at the time latch was asserted. The latch propagation delay (t_{PDL}) is the time taken for the output to return to input control after the latch pin is released. Latching is disabled if the $\overline{\text{LE}}$/HYST pin is left floating. Both outputs of the LTC6752-3 are latch controlled simultaneously.

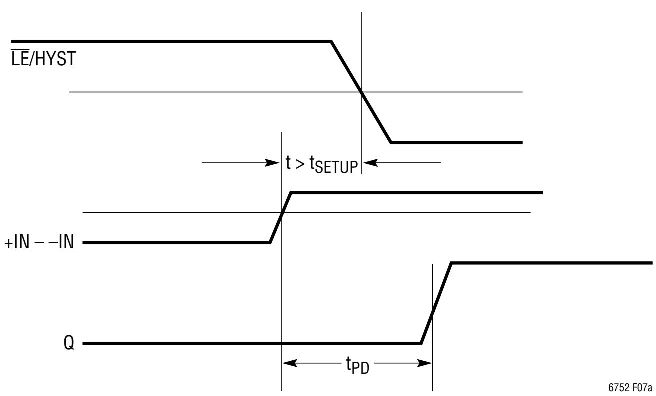


Figure 7a. Input State Change Properly Latched

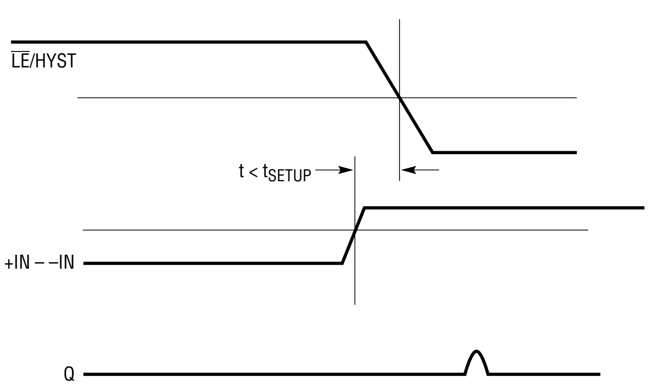


Figure 7b. Input Change Setup Time Too Short

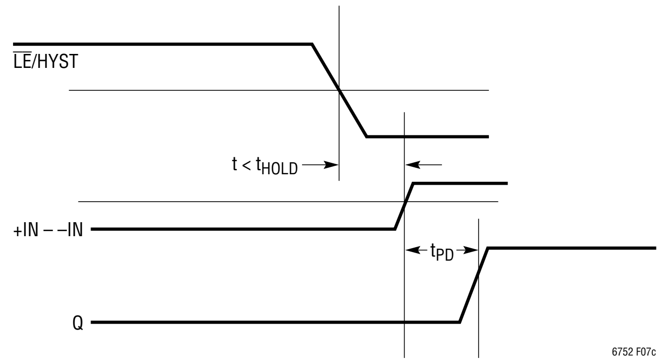


Figure 7c. Input State Not Held Long Enough. Wrong Output State Latched

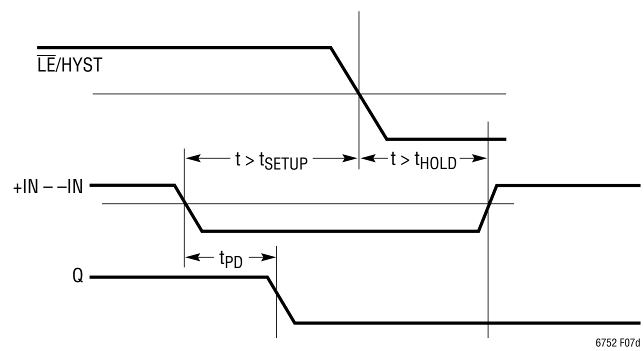


Figure 7d. Short Input Pulse Properly Captured and Latched

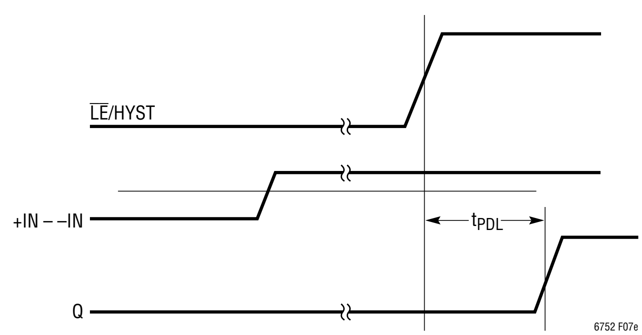


Figure 7e. Latched Output Disabled

Shutdown

The LTC6752-2 and LTC6752-3 have shutdown pins ($\overline{\text{SHDN}}$, active low) that can reduce the total supply current to a typical value of 580µA for the LTC6752-2 and 650µA for the LTC6752-3 (2.5V supply). When the part is in shutdown, the outputs are placed in a high-impedance state, since PFET and NFET output transistors whose drains

APPLICATIONS INFORMATION

are tied to the output pins are cut off and cannot source/sink any current. The shutdown pin needs to be taken to within 600mV of the negative supply for the part to shut down. When left floating, the shutdown pin is internally pulled towards the positive supply, and the comparator remains fully biased on.

Dispersion

Dispersion is defined as the change in propagation delay for different input conditions. It becomes very crucial in timing sensitive applications. Overdrive dispersion from 10mV overdrive to 125mV overdrive is typically less than 1.8ns (150mV total step size). The graph titled Propagation Delay vs Common Mode Voltage shows the dispersion due to shifts in input common mode voltage.

Jitter

The LTC6752 family has been designed for low phase noise and jitter. This allows it to be used in applications where high frequency low amplitude sine waves need to be converted to full-logic level square waves with minimal additive jitter. The graph titled Jitter vs Input Frequency demonstrates the additive jitter of the LTC6752 family for different amplitudes of a sinusoidal input. Refer to the Electrical Characteristics table to see how jitter varies with signal frequency.

High Speed Board Design Techniques

Being very high speed devices, members of the LTC6752 family are prone to output oscillations if certain guidelines are not followed at the board level. Low impedance supply planes, especially for the V_{DD} and V_{EE} pins, help to reduce supply bounce related oscillations. Supply bounce tends to worsen at higher output supply voltages due to larger swings and higher output current drive capability. Parasitic feedback between the output and input pins should be minimized. The pinouts of the LTC6752 family members have been arranged to minimize parasitic feedback. Input and output traces on the board should be placed away from each other. If that is not possible a ground or supply trace should be used as a guard to isolate them. If possible, a supply/ground trace that is not directly connected to the supply pins of the device, but rather directly connected to the supply terminal of the board, should be used for such a purpose.

The positive supply pins should be adequately bypassed to the V_{EE} pin to minimize transients on the supply. Low ESR and ESL capacitors are required due to the high speed nature of the device. Even a few nanohenries of parasitic trace inductance in series with the supply bypassing can cause several hundred millivolts of disturbance on the supply pins during output transitions. A 2.2µF capacitor in parallel with multiple low ESL, low ESR 100nF capacitors connected as close to the supply pins as possible to minimize trace impedance is recommended. In many applications the V_{EE} pin will be connected to ground. In applications where the V_{EE} pin is not connected to ground, the positive supplies should still be bypassed to V_{EE}. The V_{EE} pin should also then be bypassed to a ground plane with a 2.2µF capacitor in parallel with low ESL, low ESR 100nF capacitors if possible.

For devices with separate positive input and output supplies, capacitors should not be placed between the two positive supplies; otherwise disturbances due to output switching can couple back to the inputs.

To minimize supply bounce, the board layout must be made with careful consideration of the supply current return paths. The output current will return back to the supply via the lowest impedance path available. If the terminating connection of the load is easily available on the board, V_{EE} should be bypassed to the terminating connection using 2.2µF and 100nF capacitors as described previously.

Due to the fast rise and fall times of the LTC6752/LTC6752-2/LTC6752-3, output traces should be shielded with a low impedance ground plane to minimize electromagnetic interference. Due to the complementary nature of its outputs, the LTC6752-3 can provide a first order cancellation of EMI effects.

When the input slew rate is small, sustained oscillations can occur at the output pin while the input is transitioning due to even one millivolt of ground bounce. For applications where the input slew rate is low, internal hysteresis should not be removed by taking the $\overline{LE}$/HYST pin high, as the addition of hysteresis makes the comparators more immune to disturbances such as ground bounce. Increasing hysteresis by adjusting the $\overline{LE}$/HYST pin voltage or by adding positive feedback as discussed in the section on hysteresis can further improve noise immunity.

TYPICAL APPLICATIONS

High Speed Clock Restoration/Level Translation Circuit

High speed comparators are often used in digital systems to recover distorted clock waveforms. The separate input/output supplies feature of the LTC6752-2 allows it to be used in applications where signals need to be shifted from one voltage domain to another. Figure 8 shows a circuit that can perform both recovery and level translation functions.

In this application, the input clock signal comes from a source operating from 5V, and the signal is required to drive a receiver operating on 1.8V. The 5V input supply/1.8V output supply feature of this part is ideal for such a situation. If the input signal gets distorted and its amplitude severely reduced due to stray capacitance, stray inductance or due to reflections on the transmission line, the LTC6752-2 can be used to convert it into a full scale digital output signal that can drive the receiver.

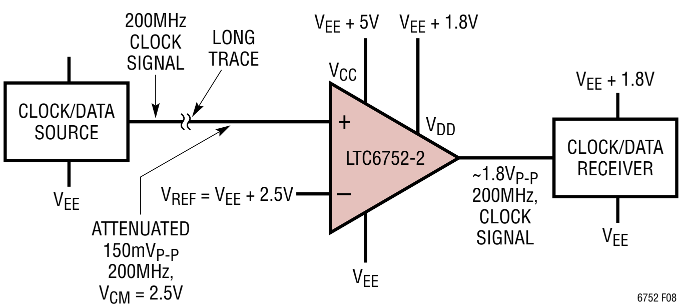


Figure 8. High Speed Clock Restoration/Level Translation/Level Shifting Circuit

Figure 9 shows the input and output waveforms of the LTC6752-2, used to recover a distorted 150mV_{P-P} 200MHz signal at a common mode of 2.5V with respect to its negative supply, into a full scale 1.8V output signal. AC-coupling could have been used at the input of the comparator, however to preserve input duty cycle information DC-coupling may be preferable, and that is where having a wide input common mode range is an advantage.

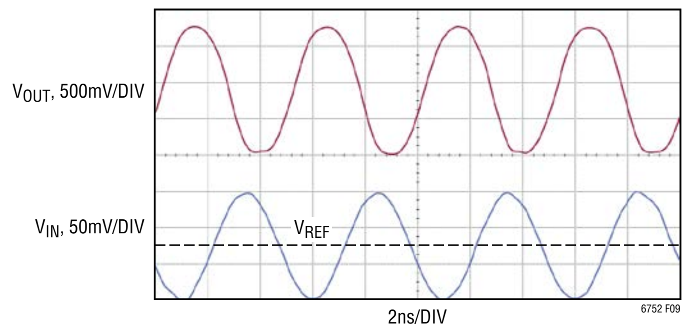


Figure 9

Optical Receiver Circuit

The LTC6752, along with a high speed high performance FET input operational amplifier like the LTC6268, can be used to implement an optical receiver as shown in Figure 10.

Figure 11 shows the output of the LTC6268 driving the –IN pin of the LTC6752-2, the +IN pin of the LTC6752-2, and the LTC6752 output. The photodiode is being driven by a light source of sinusoidally varying intensity.

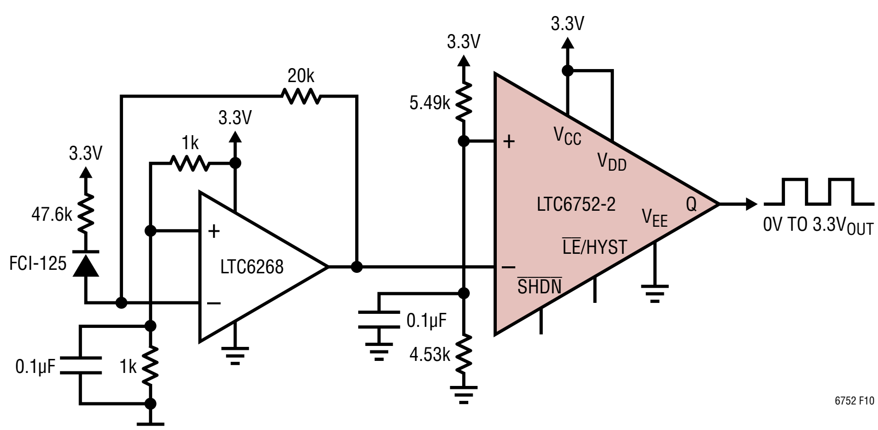


Figure 10. Optical Receiver Circuit

TYPICAL APPLICATIONS

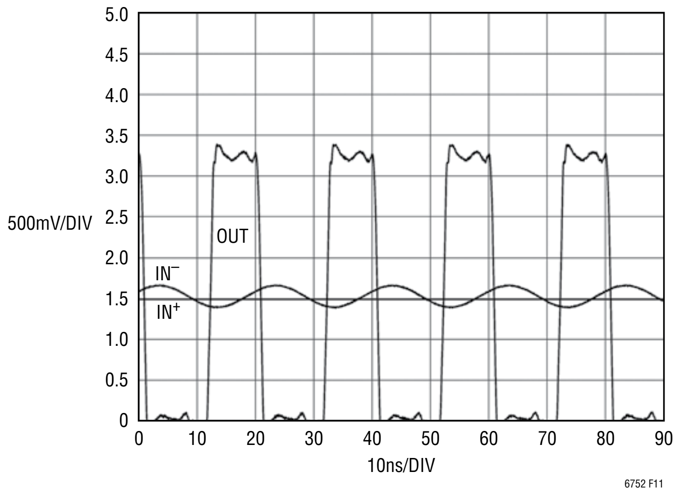


Figure 11

Pulse Stretcher Circuit/Monostable Multivibrator

For detecting short pulses from a single sensor, a pulse stretcher is often required. The circuit of Figure 12 acts as a one-shot, stretching the width of an incoming pulse to a consistent ~100ns. The circuit works as follows: Comparator U1 functions as a threshold detector, and Comparator U2 functions as a one-shot. Comparator U1 is biased with a threshold of 11mV to overcome comparator and system offsets, and establish a low output in the absence of an input signal. An input pulse causes the output of U1 to go high, which then causes the output of U2 to go high. The output of U2 is fed back to the input of the 1st comparator, Timing Capacitor C now begins charging through R. After 100ns, U2 goes low, allowing U1 also to go low. A new pulse at the input of U2 can now restart the process. Timing capacitor C can be increased without limit for longer output pulses.

Figure 13 shows input and output waveforms for the pulse stretcher circuit.

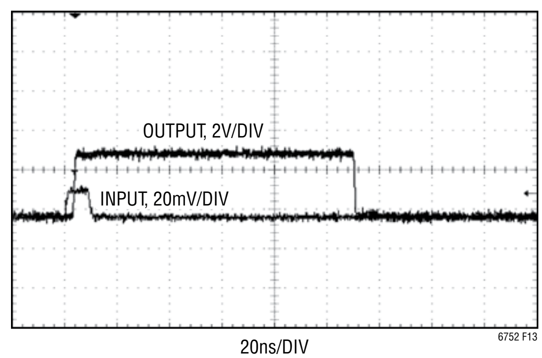


Figure 13

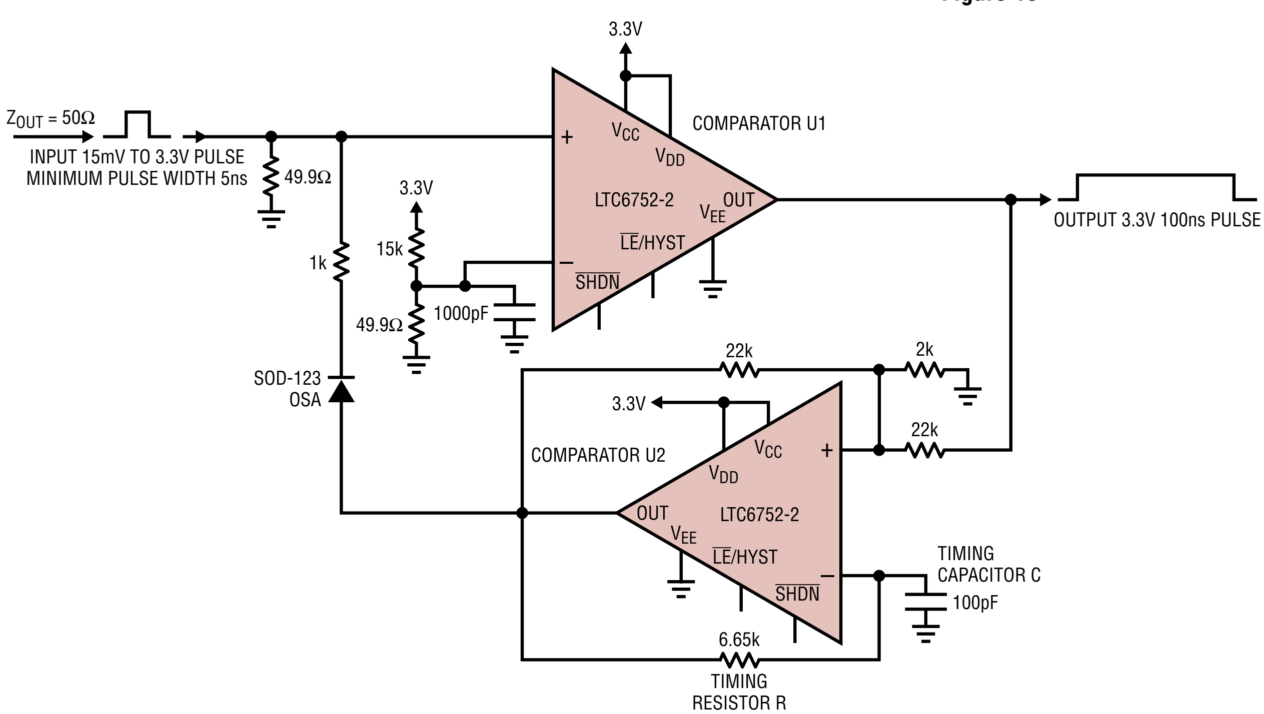


Figure 12

TYPICAL APPLICATIONS

Common Mode Rejecting Line Receiver

Differential electrical signals being transmitted over long cables are often attenuated. Electrical noise on the cables can take the form of common mode signals.

The LTC6752 comparators can be used to retrieve attenuated differential signals that have been corrupted by high frequency common mode noise, as shown in Figure 14.

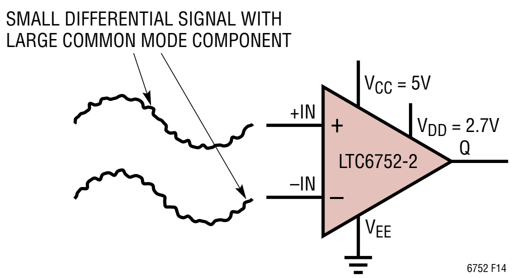


Figure 14

Figure 15 shows an LTC6752-2 retrieving a 200MHz, $200mV_{P-P}$ differential input signal that has 2.5V of random, common mode noise superimposed on it. The input supply (V_{CC}) used was 5V and the output supply used was 2.7V. A small amount of modulation is seen at the output due to a small amount of differential modulation at the inputs, which causes cycle to cycle variations in propagation delay.

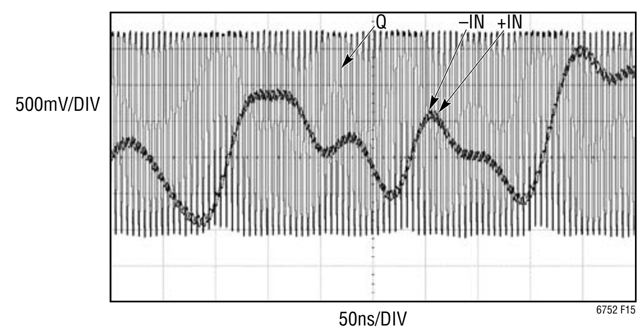
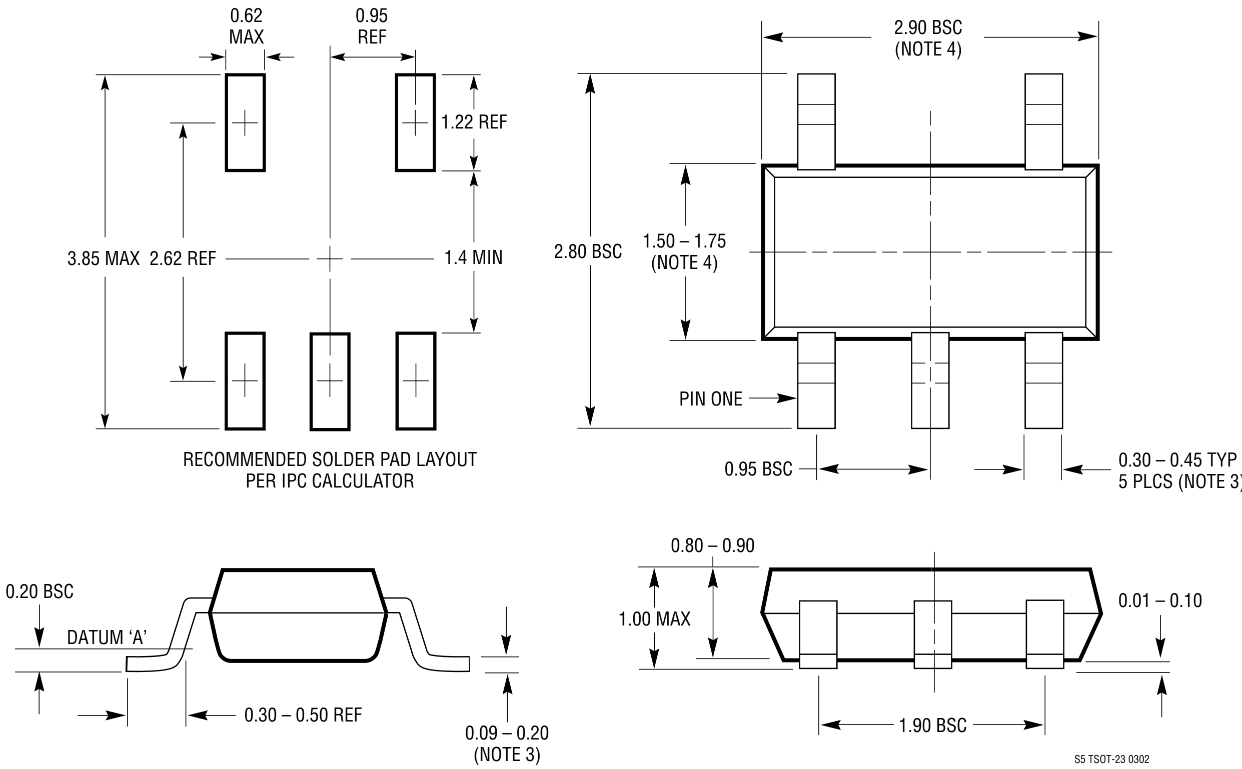


Figure 15

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)

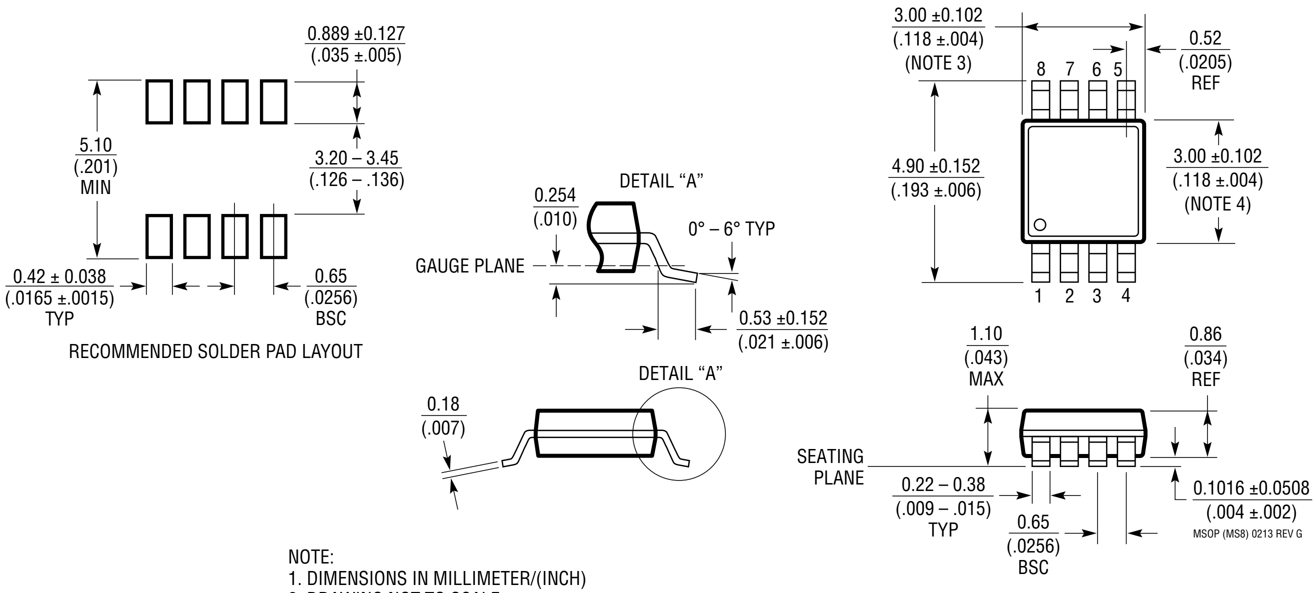


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)

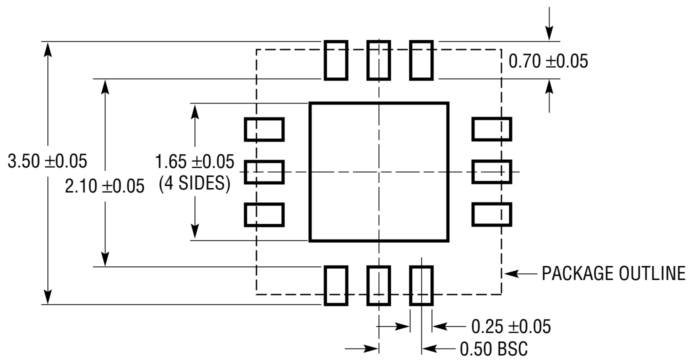


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

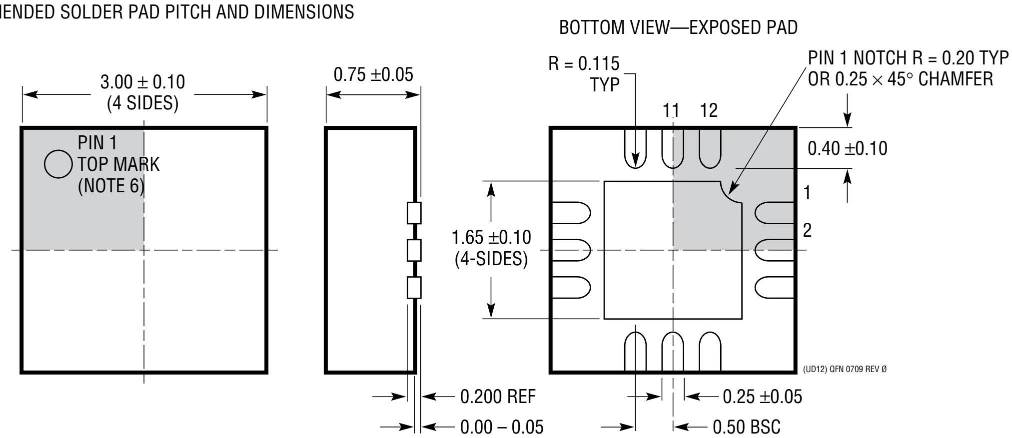
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UD Package
12-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1855 Rev Ø)



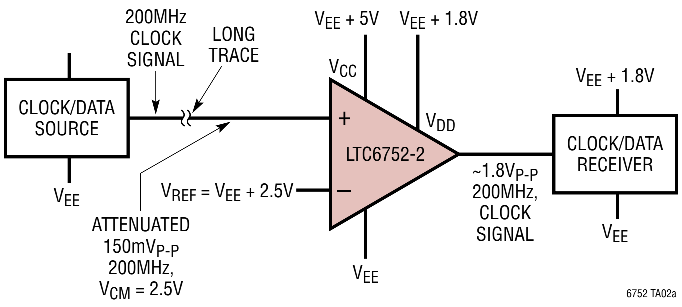
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

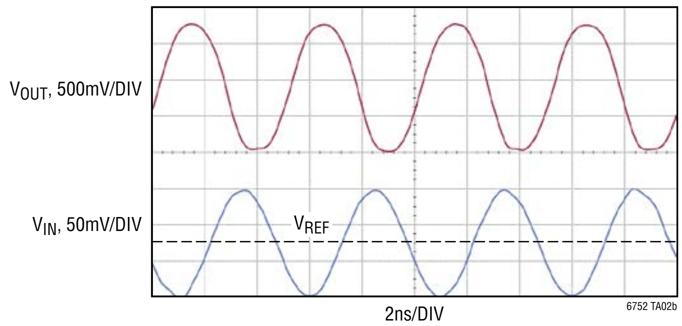


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

200MHz Clock Restoration/Level shifting





RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
High Speed Comparators		
LT1715	4ns 150MHz Dual Comparators	4.6mA at 3V
LT1711	High Speed Rail-to-Rail Comparators	3V/5V/±5V, 4.5ns at 20mV Overdrive
LT1713/LT1714	Single/Dual Low Power Rail-to-Rail Comparators	2.7V/5V/±5V, 7ns at 20mV Overdrive
LT1719/LT1720	Dual/Quad 4.5ns Rail-to-Rail Output Comparators	4mA/Comparator, 7ns at 5mV Overdrive
LT1394	7ns Single Supply Ground Sensing Comparator	6mA, 800μV Offset
LT1671	60ns Low Power Ground Sensing Comparator	5V/±5V, 450μA, 800μV Offset
LT1016	Precision 10ns Comparator	
LT1116	12ns Single Supply Ground Sensing Comparator	Inputs Can Exceed Positive Supply Up to 15V without Damaging Device
Clock Buffers/Logic Converters		
LTC6957-1/LTC6957-2/ LTC6957-3/LTC6957-4	Low Phase Noise, Dual Output Buffer/Driver/Logic Converter	LVPECL/LVDS/CMOS Outputs, Additive Jitter $45f_{SRMS}$ (LTC6957-1)
High Speed Operational Amplifiers		
LTC6252/LTC6253/ LTC6254	Single/Dual/Quad 3.5mA 720MHz	280V/μs, 2.75nV/$\sqrt{Hz}$, Rail-to-Rail I/O
LTC6246/LTC6247/ LTC6248	Single/Dual/Quad 1mA, 180MHz	90V/μs, 4.2nV/$\sqrt{Hz}$,Rail-to-Rail I/O
LTC6255/LTC6256/ LTC6257	Single/Dual/Quad 65μA, 6.5MHz	
LTC6240/LTC6241/ LTC6242	18MHz, Low Noise, CMOS	Rail-to-Rail Outputs
LTC6406	3GHz, Differential Amplifier/Driver	Rail-to-Rail Inputs
LTC6409	10GHz Differential Amplifier/ADC Driver	1.1nV/$\sqrt{Hz}$

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