0.25ppm Noise, Low Drift Precision Buffered Reference Family

FEATURES

- **Low Noise: 0.25ppm$_{P-P}$ (0.1Hz to 10Hz)**
- **Low Drift: 2ppm/°C Max**
- **High Accuracy: ±0.025% Max**
- **Fully Specified Over –40°C to 125°C**
- 100% Tested at –40°C, 25°C and 125°C
- Load Regulation: <10ppm/mA
- Sinks and Sources Current: ±5mA
- Low Dropout: 500mV
- Wide Supply Range to 13.2V
- Low Power Shutdown: <20µA Max
- Available Output Voltage Options: 2.5V
- 1.25V, 2.048V, 3V, 3.3V, 4.096V, 5V Options in Development. Contact LTC for Status
- Available in an 8-Lead MSOP Package

APPLICATIONS

- Instrumentation and Test Equipment
- High Resolution Data Acquisition Systems
- Weigh Scales
- Precision Battery Monitors
- High Temperature Applications
- Precision Regulators
- Medical Equipment

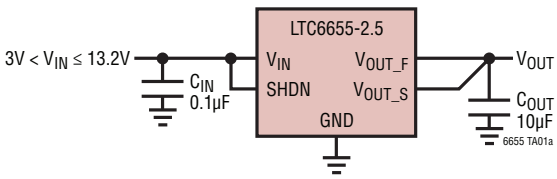
DESCRIPTION

The LTC®6655 family of bandgap references are low noise, low drift, precision voltage references that are fully specified over the –40°C to 125°C temperature range. The low noise and drift are ideally suited for the high resolution measurements required by instrumentation and test equipment, while the wide temperature range supports automotive and industrial applications. Advanced curvature compensation allows this bandgap reference to achieve a drift of less than 2ppm/°C with a predictable temperature characteristic and an output voltage accurate to ±0.025%, reducing or eliminating the need for calibration.

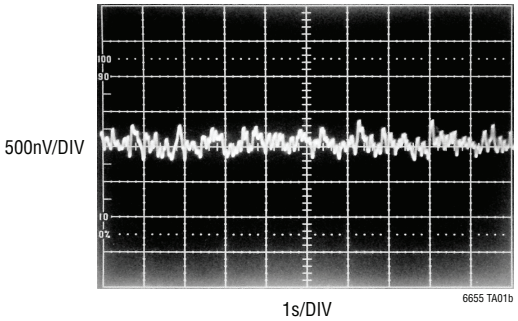
The LTC6655 low dropout series references can be powered from as little as 500mV above the output voltage or as much as 13.2V. Superior load regulation and source and sink capabilities coupled with exceptional line rejection give consistent performance over a wide range of line and load conditions. A shutdown mode is provided for low power applications. Available in a small MSOP package, the LTC6655 family of references is an excellent choice for demanding precision applications.

TYPICAL APPLICATION

Basic Connection



Low Frequency 0.1Hz to 10Hz Noise



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage

V_{IN} to GND ..... –0.3V to 13.2V

$\overline{SHDN}$ to GND ..... –0.3V to (V_{IN} + 0.3V)

Output Voltage:

V_{OUT_F} ..... –0.3V to (V_{IN} + 0.3V)

V_{OUT_S} ..... –0.3V to 6V

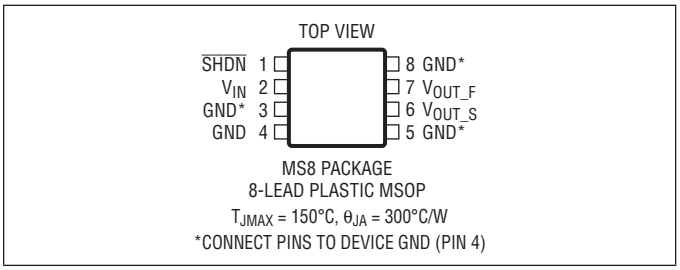
Output Short-Circuit Duration..... Indefinite

Operating Temperature Range (Note 2) . –40°C to 125°C

Storage Temperature Range (Note 2)..... –65°C to 150°C

Lead Temperature Range (Soldering, 10 sec) (Note 3)..... 300°C

PIN CONFIGURATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 300°C/W

*CONNECT PINS TO DEVICE GND (PIN 4)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6655BHMS8-2.5#PBF	LTC6655BHMS8-2.5#TRPBF	LTFCY	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655CHMS8-2.5#PBF	LTC6655CHMS8-2.5#TRPBF	LTFCY	8-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AVAILABLE OPTIONS

OUTPUT VOLTAGE	INITIAL ACCURACY	TEMPERATURE COEFFICIENT	PART NUMBER†
2.500	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHMS8-2.5 LTC6655CHMS8-2.5

†See order information section for complete part number listing. Note: Other voltage options are in development. Contact LTC for status.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} + 0.5V, V_{OUT_S} connected to V_{OUT_F}, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	LTC6655B LTC6655C		–0.025 –0.05		0.025 0.05	% %
Output Voltage Temperature Coefficient (Note 4)	LTC6655B LTC6655C	● ●		1 2.5	2 5	ppm/°C ppm/°C
Line Regulation	V_{OUT} + 0.5V ≤ V_{IN} ≤ 13.2V, $\overline{SHDN}$ = V_{IN}	 ●		5	25 50	ppm/V ppm/V
Load Regulation (Note 5)	I_{SOURCE} = 5mA	 ●		3	 25	ppm/mA ppm/mA
	I_{SINK} = 5mA	 ●		10	 50	ppm/mA ppm/mA
Operating Voltage	I_{SOURCE} = 5mA, V_{OUT} Error ≤ 0.1%	●	3		13.2	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} + 0.5V, V_{OUT_S} connected to V_{OUT_F}, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current	Short V_{OUT} to GND Short V_{OUT} to V_{IN}			20 20		mA mA
Shutdown Pin ($\overline{SHDN}$)	Logic High Input Voltage Logic High Input Current, $\overline{SHDN}$ = 2V	● ●	2	 1	 12	V µA
	Logic Low Input Voltage Logic Low Input Current, $\overline{SHDN}$ = 0.8V	● ●		 1.5	0.8 15	V µA
Supply Current	No Load	 ●		5	6.3 7	mA mA
Shutdown Supply Current	$\overline{SHDN}$ Tied to GND	●		2	20	µA
Output Voltage Noise (Note 6)	0.1Hz ≤ f ≤ 10Hz 10Hz ≤ f ≤ 1kHz			0.25 0.67		ppm_{P-P} ppm_{RMS}
Turn-On Time	0.1% Settling, C_{OUT} = 2.7µF			400		µs
Long-Term Drift of Output Voltage (Note 7)				60		ppm/$\sqrt{khr}$
Hysteresis (Note 8)	ΔT = –40°C to 125°C			60		ppm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Precision may be affected if the parts are stored outside of the specified temperature range. Large temperature changes may cause changes in device performance due to thermal hysteresis. For best performance, extreme temperatures should be avoided whenever possible.

Note 3: The stated temperature is typical for soldering of the leads during manual rework. For detailed IR reflow recommendations, refer to the Applications Information section.

Note 4: Temperature coefficient is measured by dividing the maximum change in output voltage by the specified temperature range.

Note 5: Load regulation is measured on a pulse basis from no load to the specified load current. Load current is in addition to the 2mA sense current. Output changes due to die temperature change must be taken into account separately.

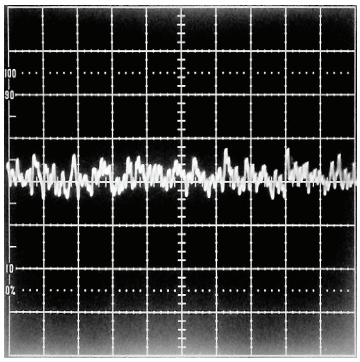
Note 6: Peak-to-peak noise is measured with a 2-pole highpass filter at 0.1Hz and 2-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads, and the test time is 10 seconds. Due to the statistical nature of noise, repeating noise measurements will yield larger and smaller peak values in a given measurement interval. By repeating the measurement for 1000 intervals, each 10 seconds long, it is shown that there are time intervals during which the noise is higher than in a typical single interval, as predicted by statistical theory. In general, typical values are considered to be those for which at least 50% of the units may be expected to perform similarly or better. For the 1000 interval test, a typical unit will exhibit noise that is less than the typical value listed in the Electrical Characteristics table in more than 80% of its measurement intervals. See Application Note 124 for noise testing details. RMS noise is measured with a spectrum analyzer in a shielded environment.

Note 7: Long-term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one-third that of the first thousand hours with a continuing trend toward reduced drift with time. Long-term stability is also affected by differential stresses between the IC and the board material created during board assembly.

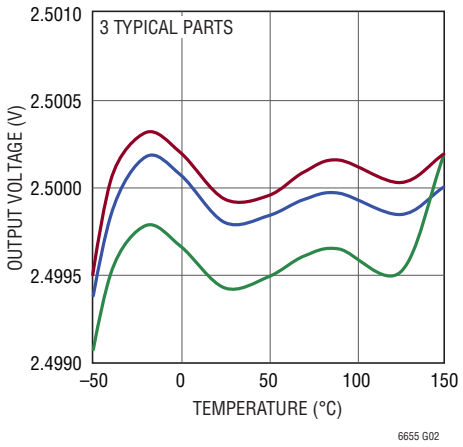
Note 8: Hysteresis in output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. Hysteresis is roughly proportional to the square of the temperature change. For instruments that are stored at well controlled temperatures (within 20 or 30 degrees of operational temperature), hysteresis is usually not a significant error source.

TYPICAL PERFORMANCE CHARACTERISTICS

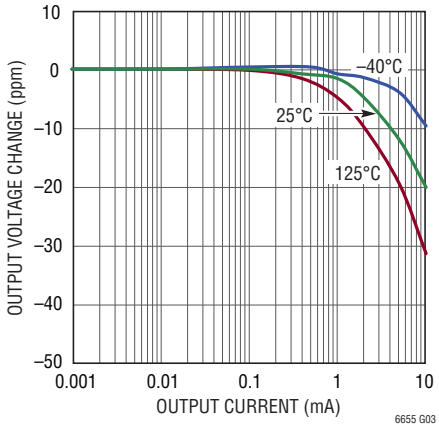
Low Frequency 0.1Hz to 10Hz Noise



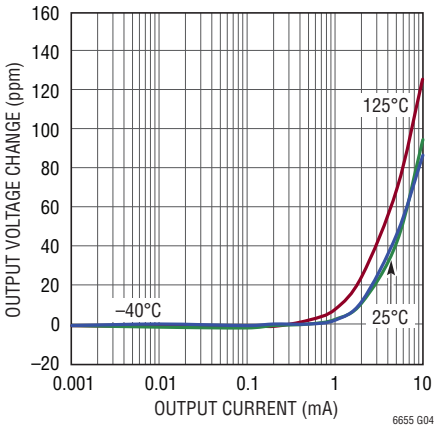
Output Voltage Temperature Drift



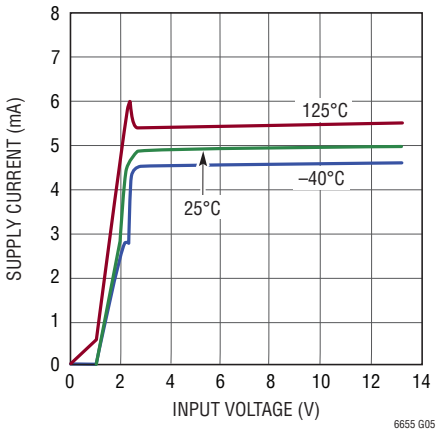
Load Regulation (Sourcing)



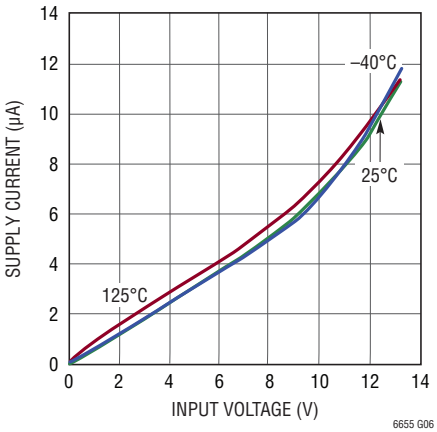
Load Regulation (Sinking)



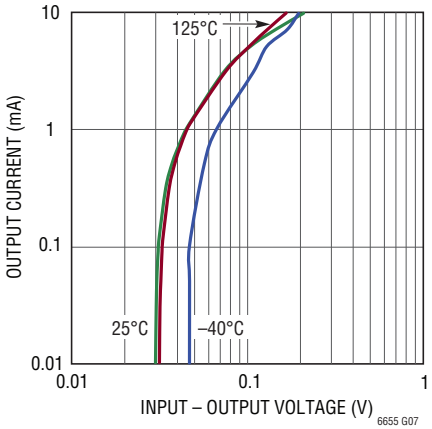
Supply Current vs Input Voltage



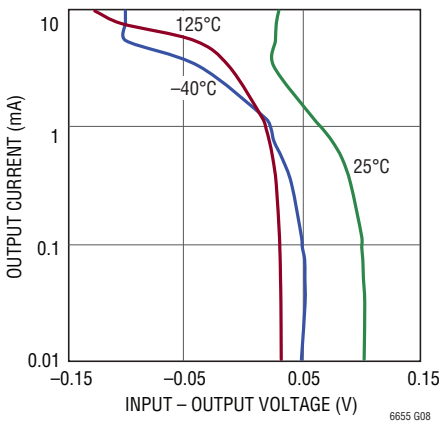
Shutdown Supply Current vs Input Voltage



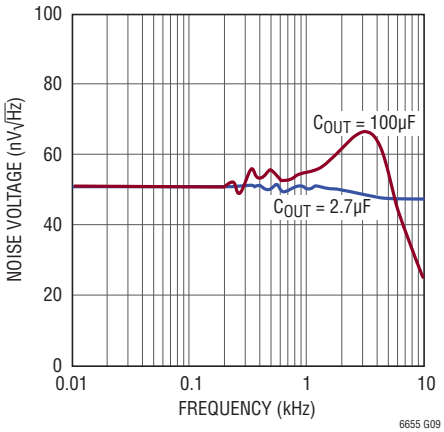
Minimum $V_{IN} – V_{OUT}$ Differential (Sourcing)



Minimum $V_{IN} – V_{OUT}$ Differential (Sinking)

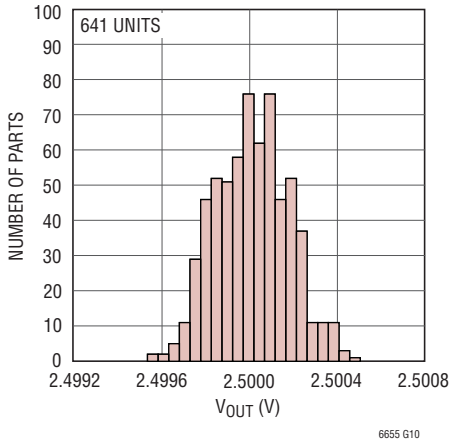


Output Voltage Noise Spectrum



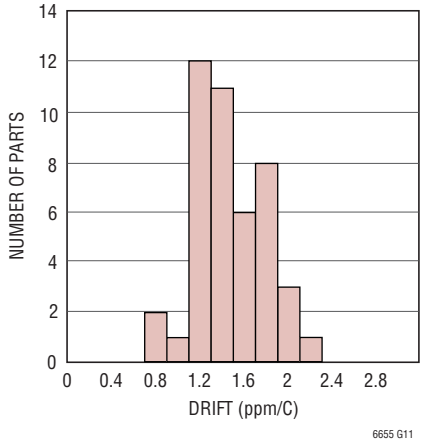
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OUT} Distribution



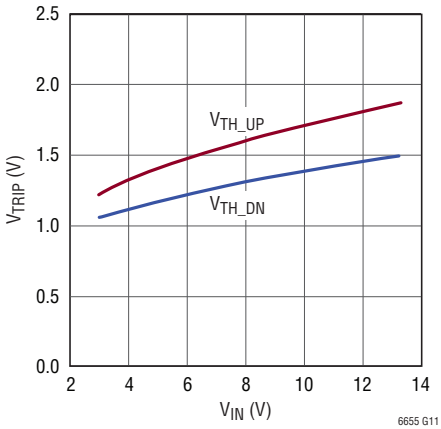
6655 G10

Temperature Drift Distribution



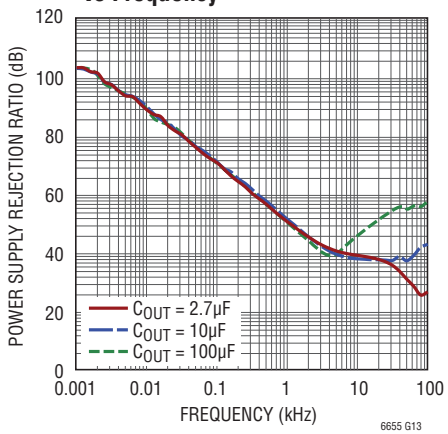
6655 G11

$\overline{SHDN}$ Input Voltage Thresholds vs V_{IN}



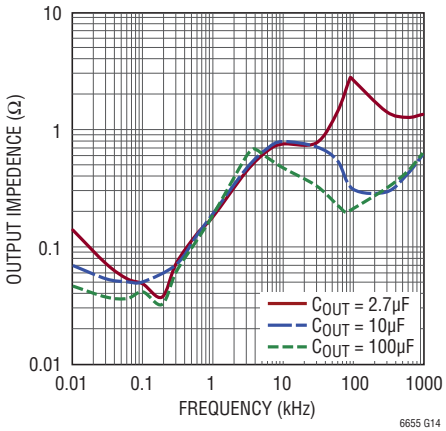
6655 G11

Power Supply Rejection Ratio vs Frequency



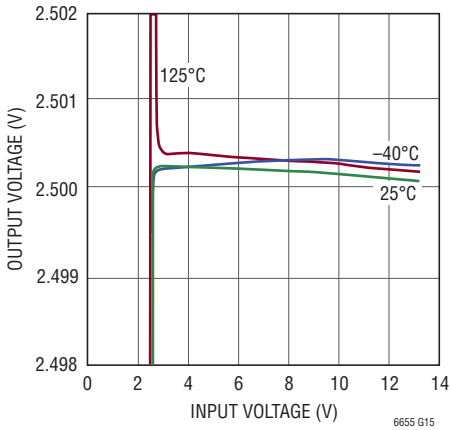
6655 G13

Output Impedance vs Frequency



6655 G14

Line Regulation



6655 G15

PIN FUNCTIONS

$\overline{\text{SHDN}}$ (Pin 1): Shutdown Input. This active low input powers down the device to <20µA. If left open, an internal pull-up resistor puts the part in normal operation. It is recommended to tie this pin high externally for best performance during normal operation.

V_{IN} (Pin 2): Power Supply. The minimum input voltage is 3V. The maximum supply is 13.2V. Bypass V_{IN} with a 0.1µF, or larger, capacitor to GND.

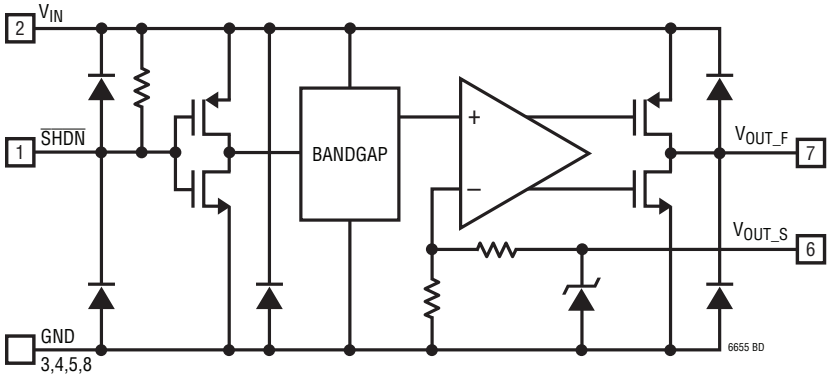
GND (Pin 4): Device Ground. This pin is the main ground and must be connected to a noise-free ground plane.

V_{OUT_S} (Pin 6): V_{OUT} Sense Pin. Connect this pin at the load and route with a wide metal trace to minimize load regulation errors. This pin sinks 2mA. For load currents <100µA, tie directly to V_{OUT_F} pin.

V_{OUT_F} (Pin 7): V_{OUT} Force Pin. This pin sources and sinks current to the load. An output capacitor of 2.7µF to 100µF is required.

GND (Pins 3, 5, 8): Internal Function. Ground these pins.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Bypass and Load Capacitors

The LTC6655 voltage references require a 0.1µF or larger input capacitor located close to the part to improve power supply rejection. An output capacitor with a value between 2.7µF and 100µF is also required.

The output capacitor has a direct effect on the stability, turn-on time and settling behavior. Choose a capacitor with low ESR to insure stability. A resistance in series (ESR) with the output capacitor introduces a zero in the output buffer transfer function and could cause instability. The 2.7µF to 100µF range includes several types of capacitors that are readily available as through-hole and surface mount components. It is recommended to keep ESR less than or equal to 0.1Ω. Capacitance and ESR are both frequency dependent. At higher frequencies capacitance drops and ESR increases. To insure stable operation the output capacitor should have the required values at 100kHz.

In order to achieve the best performance, caution should be used when choosing a capacitor. X7R ceramic capacitors are small, come in appropriate values and are relatively stable over a wide temperature range. However, for a low noise application an X7R capacitor may not be suitable since it may exhibit a piezoelectric effect and could inject noise. The mechanical vibrations cause a charge displacement in the ceramic dielectric and the resulting perturbation can mislead the user into thinking the noise is produced by the reference. If X7R capacitors are necessary, a thorough bench evaluation should be completed to verify proper performance.

For very low noise applications where every nanovolt counts, film capacitors should be considered for their low noise and lack of piezoelectric effects. Film capacitors such as polyester, polystyrene, polycarbonate, and polypropylene have good temperature stability. Additional care must be taken as polystyrene and polypropylene have an upper temperature limit of 85°C to 105°C. Above these temperatures the working voltages need to be derated according to manufacturer's specifications. Another type of film capacitor is polyphenylene sulfide (PPS). These devices work over a wide temperature range, are stable, and have large capacitance values beyond 1µF. In general, film capacitors are found in surface mount and leaded packages. Table 1 is a partial list of capacitor companies and some of their available products.

In voltage reference applications, film capacitor lifetime is affected by temperature and applied voltage. When polyester capacitors need to work beyond their rated temperatures (some as low as 85°C) they need to be derated. Voltage derating is usually accomplished as a ratio of applied voltage to rated voltage limit. Contact specific film capacitor manufacturers to determine exact lifetime and derating information.

The lifetime of X7R capacitors is long, especially for reference applications. Capacitor lifetime is degraded by operating near or exceeding the rated voltage, at high temperature, with AC ripple or some combination of these. Most reference applications have AC ripple only during transient events.

Table 1. Film Capacitor Companies

COMPANY	DIELECTRIC	AVAILABLE CAPACITANCE	TEMPERATURE RANGE	TYPE
Cornell Dublier	Polyester	0.5µF to 10µF	–55°C to 125°C	DME
Dearborn Electronics	Polyester	0.1µF to 12µF	–55°C to 125°C	218P, 430P, 431P, 442P, and 410P
Tecate	Polyester	0.01µF to 18µF	–40°C to 105°C	901, 914, and 914D
Wima	Polyester	10µF to 22µF	–55°C to 100°C	MKS 4, MKS 2-XL
Vishay	Polyester	1000pF to 15µF	–55°C to 125°C	MKT1820
Vishay	Polycarbonate	0.01µF to 10µF	–55°C to 100°C	MKC1862, 632P
Dearborn Electronics	Polyphenylene Sulfide (PPS)	0.01µF to 15µF	–55°C to 125°C	820P, 832P, 842P, 860P, and 880P
Wima	Polyphenylene Sulfide (PPS)	0.01µF to 6.8µF	–55°C to 140°C	SMD-PPS

APPLICATIONS INFORMATION

The choice of output capacitor also affects the bandwidth of the reference circuitry and resultant noise peaking. As shown in Figure 1, the bandwidth is inversely proportional to the value of the output capacitor.

Noise peaking is related to the phase margin of the output buffer. Higher peaking generally indicates lower phase margin. Other factors affecting noise peaking are temperature, input voltage, and output load current.

Start-Up

Results for the following transient response plots were produced with the test circuit shown in Figure 2 unless otherwise indicated.

The turn-on time for the LTC6655-2.5 is shown in Figure 3. Here the output capacitor is 3.3µF and the input capacitor is 0.1µF. The size of the output capacitor determines the speed of turn on.

Figure 4 shows the output response to a 500mV step on V_{IN}. The output response to a current step sourcing and sinking is shown in Figures 5 and 6, respectively.

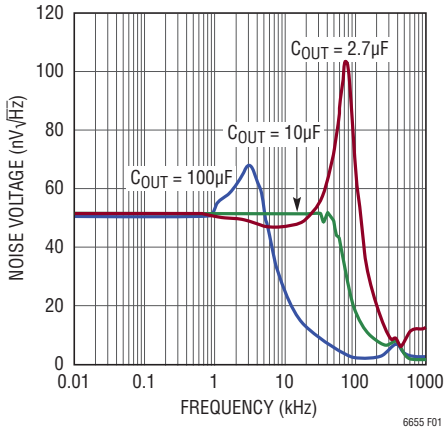


Figure 1. Output Voltage Noise Spectrum

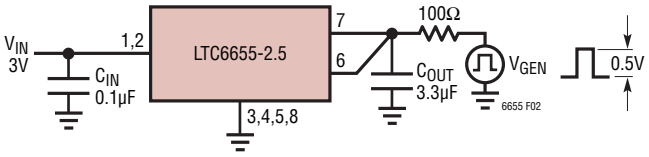


Figure 2. Transient Load Test Circuit

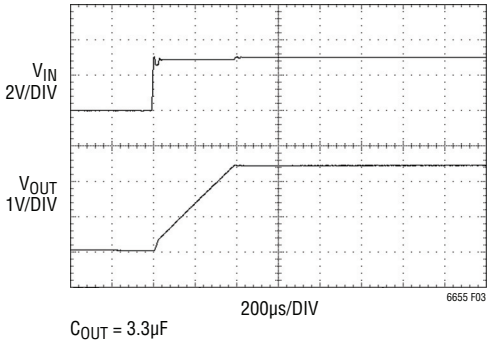


Figure 3. Start-Up Response

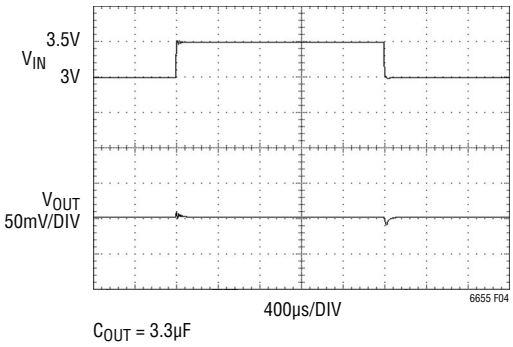


Figure 4. Output Response with a 500mV Step On V_{IN}

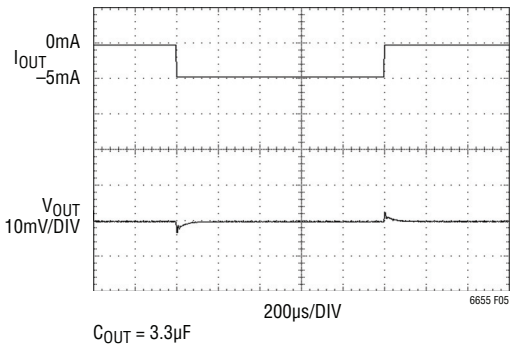


Figure 5. Output Response with a 5mA Load Step Sourcing

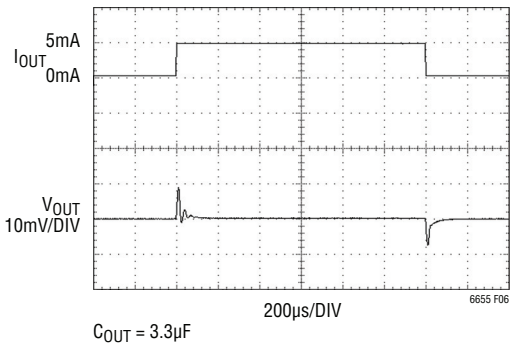


Figure 6. Output Response with 5mA Load Step Sinking

APPLICATIONS INFORMATION

Figure 7 shows the output response as the current goes from sourcing to sinking.

Shutdown Mode

The LTC6655 family of references can be shut down by tying the $\overline{SHDN}$ pin to ground. There is an internal pull-up resistor tied to this pin. If left unconnected this pin rises to V_{IN} and the part is enabled. Due to the low internal pull-up current, it is recommended that the $\overline{SHDN}$ pin be pulled high externally for normal operation to prevent accidental shutdown due to system noise or leakage currents. The turn-on/turn-off response due to shutdown is shown in Figure 8.

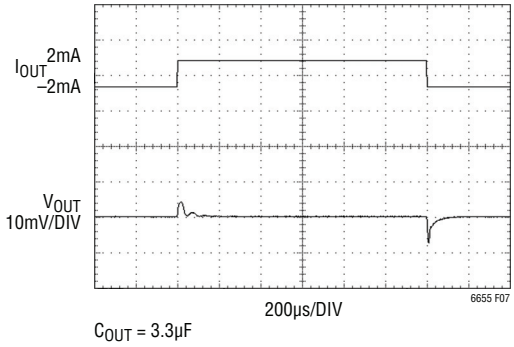


Figure 7. Output Response Showing a Sinking to Sourcing Transition

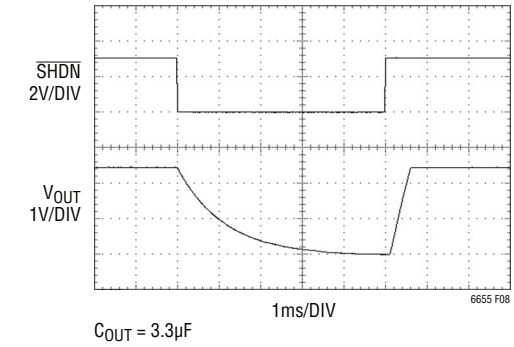


Figure 8. Shutdown Response with 5mA Source Load

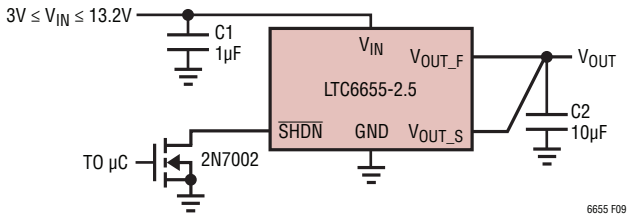


Figure 9. Open-Drain Shutdown Circuit

To control shutdown from a low voltage source, a MOSFET acts as a pull-down device as shown in Figure 9. Note that an external resistor is unnecessary. A MOSFET with a low drain-to-source leakage over the operating temperature range should be chosen to avoid inadvertently pulling down the $\overline{SHDN}$ pin. A resistor may be added from $\overline{SHDN}$ to V_{IN} to overcome excessive MOSFET leakage.

The $\overline{SHDN}$ thresholds have some dependency on V_{IN} and temperature as shown in the Typical Performance Characteristics section. Avoid leaving $\overline{SHDN}$ at a voltage between the thresholds as this will cause an increase in supply current due to shoot-through current.

Long-Term Drift

Long-term drift cannot be extrapolated from accelerated high temperature testing. This erroneous technique gives drift numbers that are wildly optimistic. The only way long-term drift can be determined is to measure it over the time interval of interest.

The LTC6655 long-term drift data was collected on 80 parts that were soldered into printed circuit boards similar to a "real world" application. The boards were then placed into a constant temperature oven with a T_A = 35°C, their outputs were scanned regularly and measured with an 8.5 digit DVM. Long-term drift is shown in Figure 10.

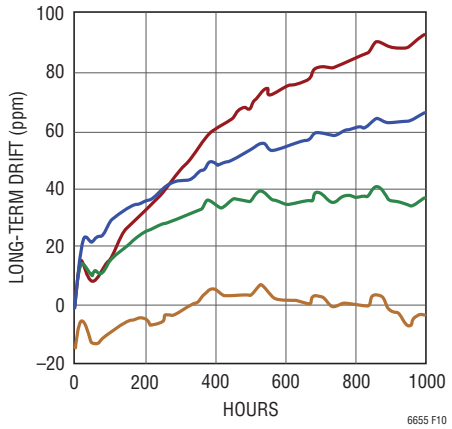


Figure 10. Long-Term Drift

APPLICATIONS INFORMATION

Hysteresis

Thermal hysteresis is a measure of how much the output changes as the ambient temperature cycles from hot to room to cold and back to room temperature. Data collected on the LTC6655-2.5 is shown in Figure 11. A proprietary design technique minimizes thermal hysteresis, setting a new benchmark in bandgap reference performance.

Power Dissipation

Power dissipation for the LTC6655-2.5 depends on V_{IN} and load current. Figure 12 illustrates the power consumption versus V_{IN} under a no-load and 5mA load condition at room temperature.

The MSOP8 package has a thermal resistance (θ_{JA}) approximately equal to 300°C/W. Under the maximum loaded condition, the increase in die temperature is over 35°C. If operated at these conditions with an ambient temperature of 125°C, the absolute maximum junction temperature rating of the device would be exceeded. The plot in Figure 13 shows the maximum ambient temperature limits for differing V_{IN} and load conditions using a maximum operating junction temperature of 150°C.

While this figure shows the absolute maximum limit, for best performance the LTC6655 family of references should not exceed a junction temperature of 125°C. This can be estimated by shifting the curves in Figure 13 down by 25°C.

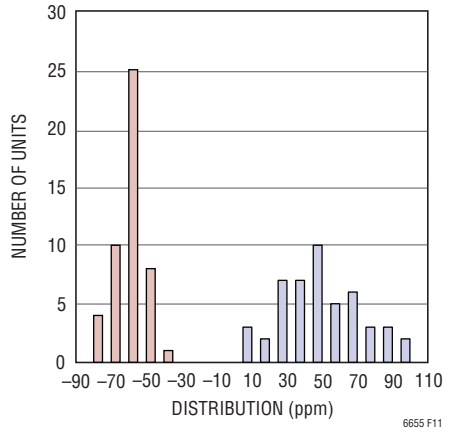


Figure 11. Hysteresis Plot –40°C to 125°C

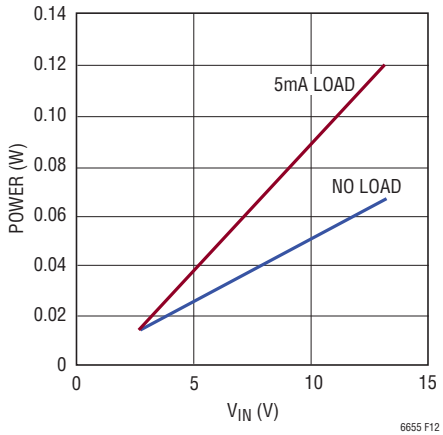


Figure 12. LTC6655-2.5 Power Consumption

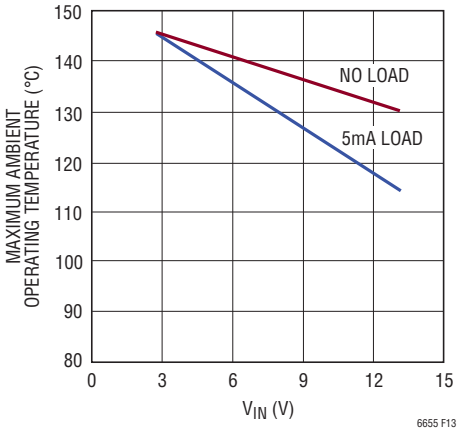


Figure 13. LTC6655-2.5 Maximum Ambient Operating Temperature

PC Board Layout

The LTC6655 reference is a precision device that is factory trimmed to an initial accuracy of ±0.025%, as shown in the Typical Performance Characteristic section. The mechanical stress caused by soldering parts to a printed circuit board may cause the output voltage to shift and the temperature coefficient to change.

To reduce the effects of stress-related shifts, mount the reference near the short edge of a printed circuit board or in a corner. In addition, slots can be cut into the board on two sides of the device to reduce mechanical stress. A thicker and smaller board is stiffer and less prone to bend. Finally, use stress relief, such as flexible standoffs, when mounting the board.

APPLICATIONS INFORMATION

Additional precautions include making sure the solder joints are clean and the board is flux free to avoid leakage paths. A sample PCB layout is shown in Figure 14.

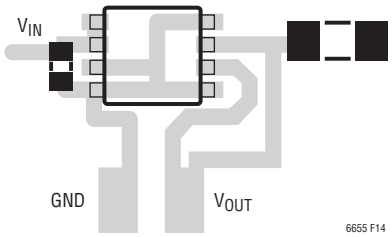


Figure 14. Sample PCB Layout

Load Regulation

To take advantage of the V_{OUT} Kelvin force/sense pins, the V_{OUT_S} pin should be connected separately from the V_{OUT_F} pin as shown in Figure 15.

The V_{OUT_S} pin sinks 2mA, which is unusual for a Kelvin connection. However, this is required to achieve the exceptional low noise performance. The I • R drop on the V_{OUT_S} line directly affects load regulation. The V_{OUT_S} trace should be as short and wide as possible to minimize voltage drops. The V_{OUT_F} pin is not as important as the V_{OUT_S} pin in this regard. An I • R drop on the V_{OUT_F} pin cuts into the dropout voltage when sourcing current, but does not directly affect load regulation. For light loading of the output (maximum output current <100µA), V_{OUT_S} should be tied to V_{OUT_F} by the shortest possible path to reduce errors caused by resistance in the sense trace.

Careful attention to grounding is also important, especially when sourcing current. The return load current can produce an I • R drop causing poor load regulation. Use a "star" ground connection and minimize the ground to load metal resistance. Although there are several pins that are required to be connected to ground, Pin 4 is the actual ground for return current.

Optimal Noise Performance

The LTC6655 offers extraordinarily low noise for a bandgap reference—only 0.25ppm in 0.1Hz to 10Hz. As a result, system noise performance may be dominated by system design and physical layout.

Some care is required to achieve the best possible noise performance. The use of dissimilar metals in component leads and PC board traces creates thermocouples. Variations in thermal resistance, caused by uneven air flow, create differential lead temperatures, thereby causing thermoelectric voltage noise at the output of the reference. Minimizing the number of thermocouples, as well as limiting airflow, can substantially reduce these errors. Additional information can be found in Linear Technology Application Note 82. Position the input and load capacitors close to the part. Although the LTC6655 has a DC PSRR of over 100dB, the power supply should be as clean as possible to guarantee optimal performance. A plot of the 0.1Hz to 10Hz low frequency noise is shown in the Typical Performance Characteristic section. To realize extremely low noise operation, place several LTC6655s in parallel as shown in the Typical Applications section. The noise is reduced by $\sqrt{N}$, where N is the number of LTC6655s in parallel.

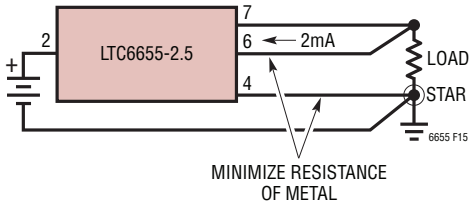


Figure 15. Kelvin Connection for Good Load Regulation

APPLICATIONS INFORMATION

IR Reflow Shift

The mechanical stress of soldering a part to a board can cause the output voltage to shift. Moreover, the heat of an IR reflow or convection soldering oven can also cause the output voltage to shift. The materials that make up a semiconductor device and its package have different rates of expansion and contraction. After a part undergoes the extreme heat of a lead-free IR reflow profile, like the one shown in Figure 16, the output voltage shifts. After the device expands, due to the heat, and then contracts, the stresses on the die have changed position. This shift is similar, but more extreme than thermal hysteresis.

Experimental results of IR reflow shift are shown below in Figure 17. These results show only shift due to reflow and not mechanical stress.

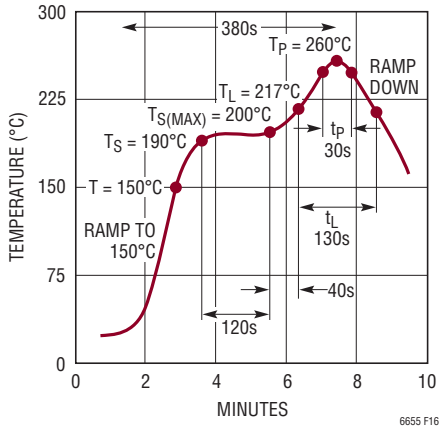


Figure 16. Lead-Free Reflow Profile

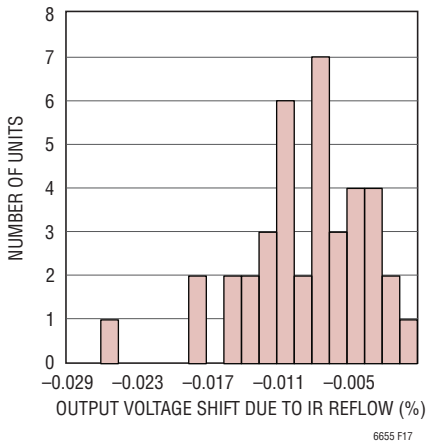
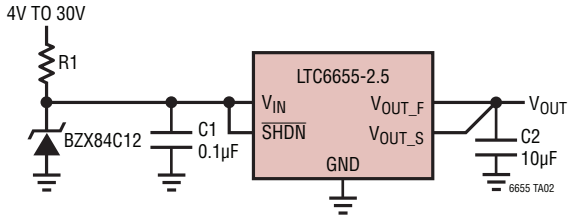


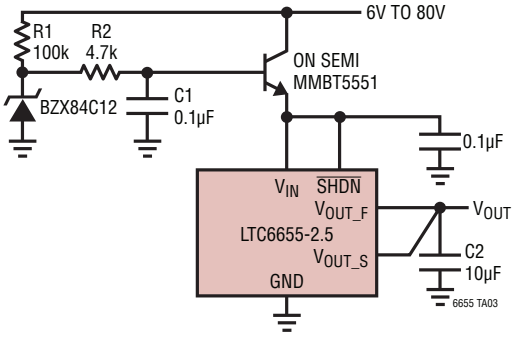
Figure 17. Output Voltage Shift Due to IR Reflow

TYPICAL APPLICATIONS

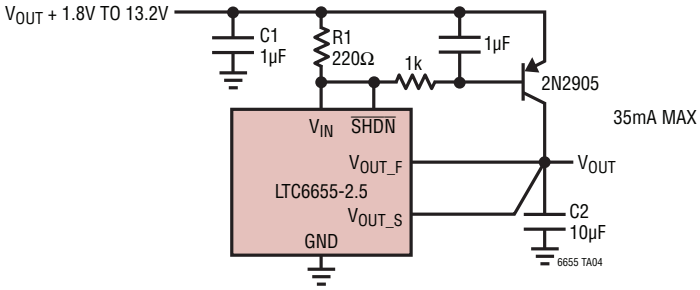
Extended Supply Range Reference



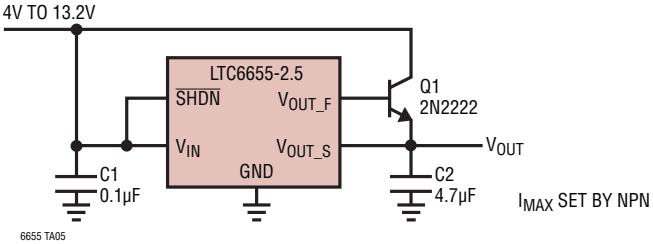
Extended Supply Range Reference



Boosted Output Current

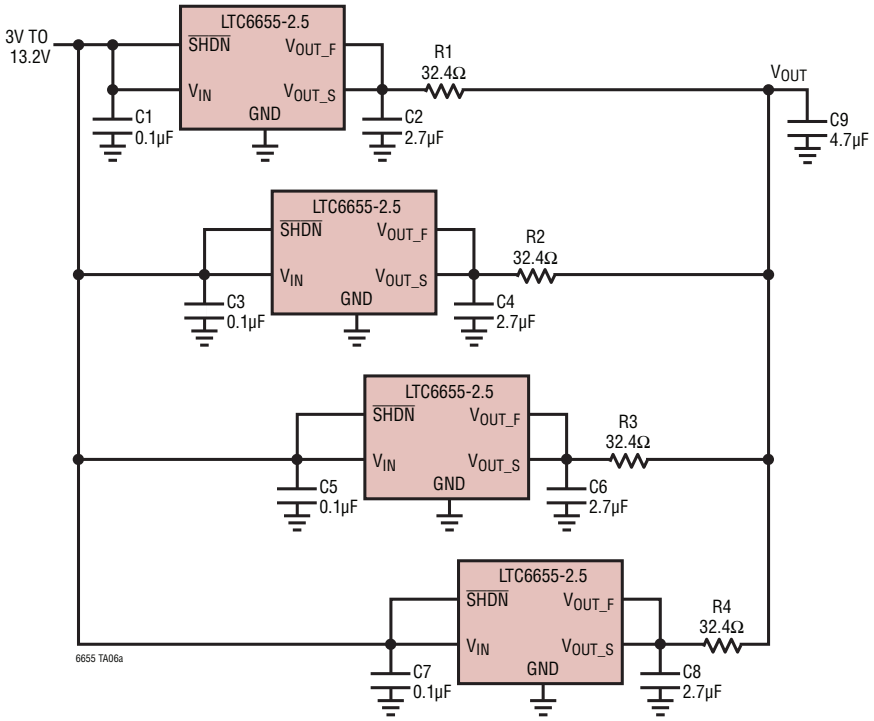


Boosted Output Current

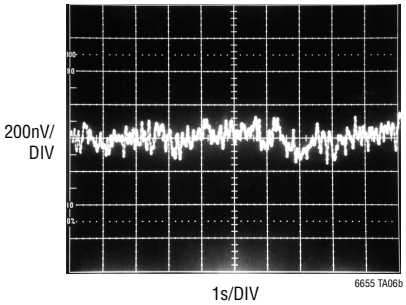


TYPICAL APPLICATIONS

Low Noise Statistical Averaging Reference
$E'_N = E_N/\sqrt{N}$; Where N is the Number of LTC6655s in Parallel

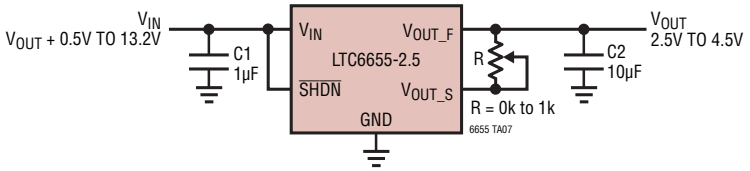


Low Frequency Noise (0.1Hz to 10Hz) with Four LTC6655-2.5 in Parallel



320nV$_{P-P}$
0.1Hz to 10Hz

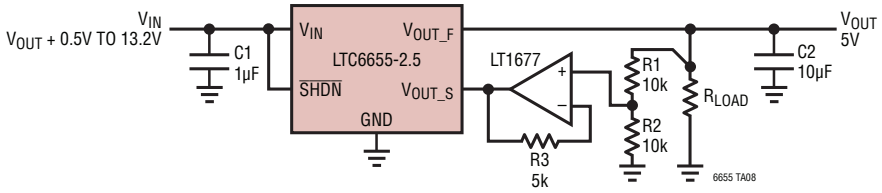
Output Voltage Boost



V_{OUT} = VOLTAGE OPTION + 0.002 • R
THIS EXAMPLE USES 2.5V AS THE VOLTAGE OPTION

FOR R USE A POTENTIOMETER THAT CAN HANDLE 2mA, IS LOW NOISE AND HAS A LOW TEMPERATURE COEFFICIENT

Low Noise Precision Voltage Boost Circuit

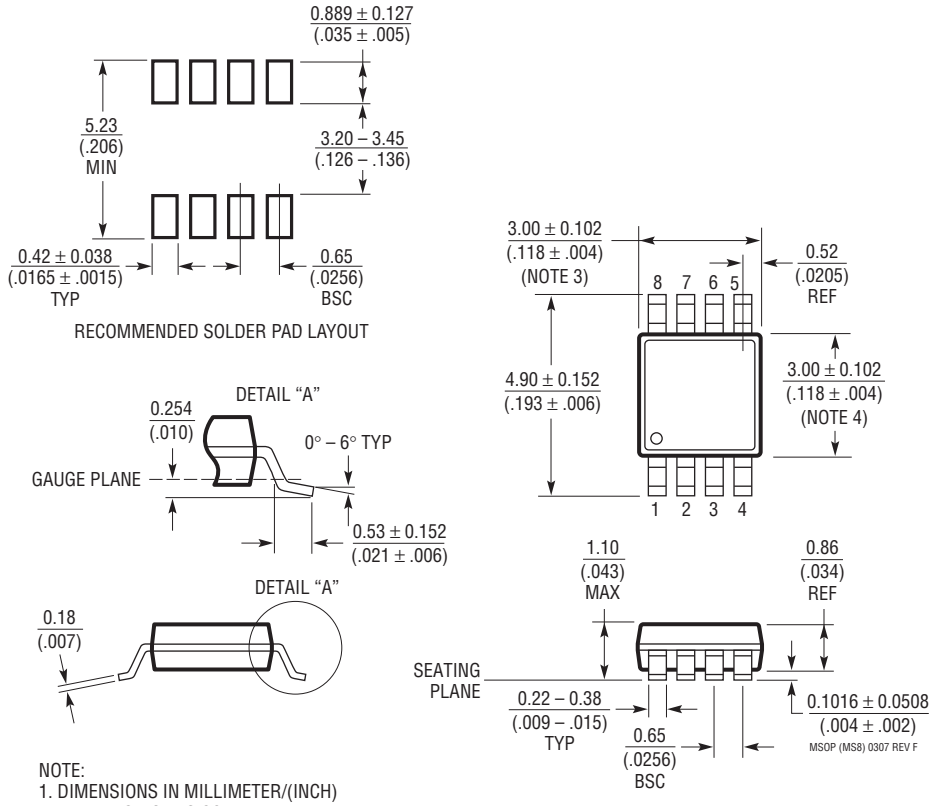


V_{OUT} = VOLTAGE OPTION • (1 + R1/R2)
THIS EXAMPLE USES 2.5V AS THE VOLTAGE OPTION

FOR R1 AND R2 USE VISHAY TRIMMED RESISTOR ARRAY (VSR144 OR MPM). WITH A PRECISION ARRAY THE MATCHING AND LOW TC WILL HELP PRESERVE LOW DRIFT. R3 = R1||R2

PACKAGE DESCRIPTION

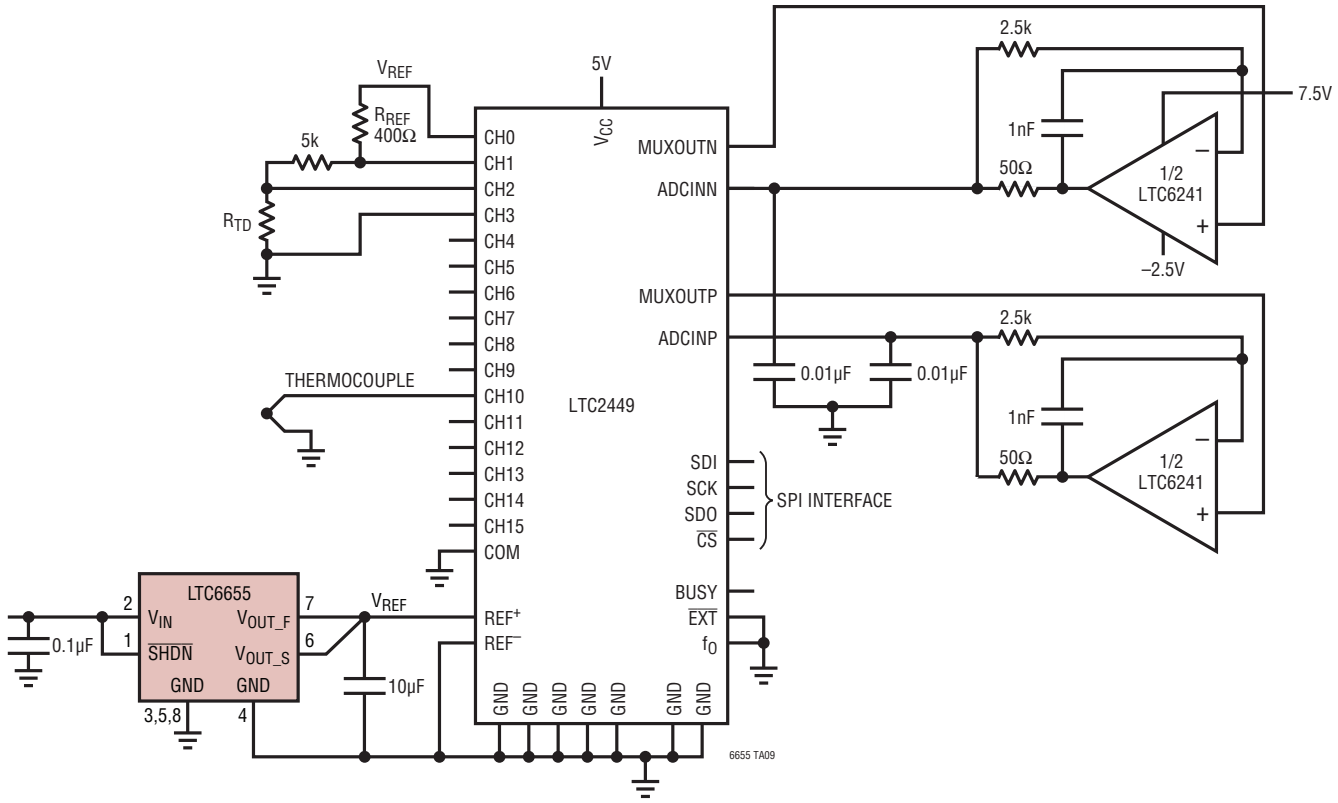
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Low Noise Precision 24-Bit Analog-to-Digital Converter Application



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1236	Precision Low Drift Low Noise Reference	0.05% Max, 5ppm/°C Max, 1ppm (Peak-to-Peak) Noise
LT1460	Micropower Series References	0.075% Max, 10ppm/°C Max, 20mA Output Current
LT1461	Micropower Series Low Dropout	0.04% Max, 3ppm/°C Max, 50mA Output Current
LT1790	Micropower Precision Series References	0.05% Max, 10ppm/°C Max, 60mA Supply, SOT23 Package
LT6650	Micropower Reference with Buffer Amplifier	0.5% Max, 5.6mA Supply, SOT23 Package
LTC6652	Precision Low Drift Low Noise Reference	0.05% Max, 5ppm/°C Max, –40°C to 125°C, MSOP8
LT6660	Tiny Micropower Series Reference	0.2% Max, 20ppm/°C Max, 20mA Output Current, 2mm × 2mm DFN

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