1.5ppm/°C Drift, Low Noise, Buffered Reference

FEATURES

- **Low Drift**
  - **A Grade: 1.5ppm/°C Max**
  - **B Grade: 3ppm/°C Max**
- **Low Noise:**
  - **0.5ppm$_{P-P}$ (0.1Hz to 10Hz)**
  - **0.8ppm$_{RMS}$ (10Hz to 1kHz)**
- **Wide Supply Range to 40V**
- **Sources and Sinks 10mA Min**
- Line Regulation: 0.2ppm/V
- Load Regulation: 0.7ppm/mA
- Reverse Supply Protection
- Reverse Output Protection
- Low Power Shutdown: <4µA Max
- Thermal Protection
- Can Operate in Shunt Mode
- Configurable as a Negative Reference
- Available Output Voltage Option: 2.5V
- MSOP-8 Package

APPLICATIONS

- High Temperature Industrial
- High Resolution Data Acquisition Systems
- Instrumentation and Process Control
- Automotive Control and Monitoring
- Medical Equipment
- Shunt and Negative Voltage References

DESCRIPTION

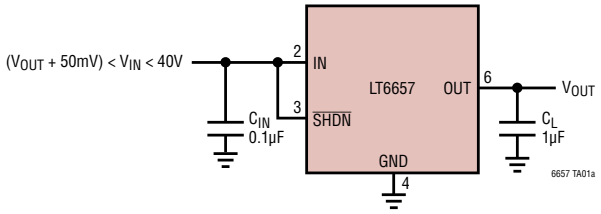
The LT®6657 is a precision voltage reference that combines robust operating characteristics with extremely low drift and low noise. With advanced curvature compensation, this bandgap reference achieves 1.5ppm/°C drift with predictable temperature behavior, and an initial voltage accuracy of 0.1%. It also offers 0.5ppm$_{P-P}$ noise and very low temperature cycling hysteresis.

The LT6657 is a low dropout reference that can be powered from as little as 50mV above the output voltage, up to 40V. The buffered output supports ±10mA of output drive with low output impedance and precise load regulation. The high sink current capability allows operation as a negative voltage reference with the same precision as a positive reference. This part is safe under reverse battery conditions, and includes current protection when the output is short-circuited and thermal shutdown for overload conditions. A shutdown is included to allow power reduction while enabling a quick turn-on.

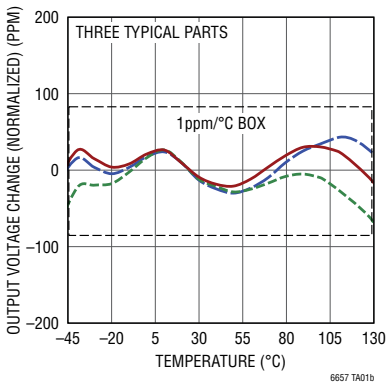
The LT6657 is fully specified over the temperature range of –40°C to 125°C. It is available in the 8-lead MSOP package.

TYPICAL APPLICATION

Basic Connection



Output Voltage Temperature Drift

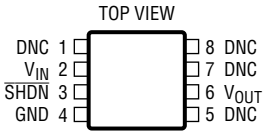


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage V_{IN} (to GND) ..... –40V to 40V
Shutdown Voltage $\overline{SHDN}$ ..... –20V to 40V
Output Voltage V_{OUT} ..... –3V to 30V
Input-to-Output Differential Voltage (Note 2) ..... ±40V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature
Range ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec)
(Note 3) ..... 300°C

PIN CONFIGURATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 273°C/W
DNC: CONNECTED INTERNALLY
DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6657AHMS8-2.5#PBF	LT6657AHMS8-2.5#TRPBF	LTGKN	8-Lead Plastic MSOP	–40°C to 125°C
LT6657BHMS8-2.5#PBF	LT6657BHMS8-2.5#TRPBF	LTGKN	8-Lead Plastic MSOP	–40°C to 125°C

*Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

†This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

AVAILABLE OPTIONS

OUTPUT VOLTAGE	INITIAL ACCURACY	TEMPERATURE COEFFICIENT	ORDER PART NUMBER**	SPECIFIED TEMPERATURE RANGE
2.5V	0.1%	1.5ppm/°C	LT6657AHMS8-2.5	–40°C to 125°C
	0.1%	3ppm/°C	LT6657BHMS8-2.5	–40°C to 125°C

** See the Order Information section for complete part number listing.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. The test conditions are $V_{IN} = V_{OUT} + 0.5V$, $V_{\overline{SHDN}} = 1.6V$, $I_{OUT} = 0$, $C_{OUT} = 1\mu F$, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage Accuracy				–0.1	0	0.1	%
Output Voltage Temperature Coefficient (Note 4)	LT6657A LT6657B		● ●		0.5 1	1.5 3	ppm/°C ppm/°C
Line Regulation (Note 5)	$V_{OUT} + 0.5V \le V_{IN} \le 40V$		 ●		0.2	2 4	ppm/V ppm/V
Load Regulation (Note 5)	I_{OUT} (Source) = 10mA		 ●		0.7	2 4	ppm/mA ppm/mA
	I_{OUT} (Sink) = 10mA		 ●		0.9	3 6	ppm/mA ppm/mA
	Shunt Configuration V_{OUT} Is Shorted to V_{IN} I_{SHUNT} 2.5 to 11mA		●		0.9	6	ppm/mA
Minimum $V_{IN} - V_{OUT}$	$V_{IN} - V_{OUT}$, ΔV_{OUT} = 0.1%	I_{OUT} = 0mA	 ●		20	50 70	mV mV
		I_{OUT} (Source) = 10mA	 ●		330	450 500	mV mV
		I_{OUT} (Sink) = 10mA	 ●		–230	–150 –50	mV mV
Shutdown Pin ($\overline{SHDN}$)	Logic High Input Voltage Logic High Input Current, $\overline{SHDN}$ = 1.6V		● ●	1.6	 0.7	 2	V µA
	Logic Low Input Voltage Logic Low Input Current, $\overline{SHDN}$ = 0.8V		● ●		 0.2	0.8 1	V µA
Supply Current in Shutdown	$\overline{SHDN}$ = 0.4V		●		0.01	4	µA
	$\overline{SHDN}$ = 0.8V		●		2.0	20	µA
Supply Current	No Load		 ●		1.2	1.8 2.3	mA mA
Output Short-Circuit Current	Short V_{OUT} to GND Short V_{OUT} to V_{IN}				15 16		mA mA
Output Voltage Noise (Note 6)	0.1Hz ≤ f ≤ 10Hz 10Hz ≤ f ≤ 1kHz				0.5 0.8		ppm_{P-P} ppm_{RMS}
Turn-On Time	0.1% Settling, C_L = 1µF				180		µsec
Long-Term Drift of Output Voltage (Note 7)					30		ppm/$\sqrt{kHr}$
Hysteresis (Note 8)	ΔT = 0°C to 50°C ΔT = 0°C to 70°C ΔT = –40°C to 85°C ΔT = –40°C to 125°C ΔT = –55°C to 125°C				20 24 30 35 40		ppm ppm ppm ppm ppm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: With V_{IN} at 40V, V_{OUT} may not be pulled below 0V. The total V_{IN} to V_{OUT} differential voltage must not exceed ±40V.

Note 3: The stated temperature is typical for soldering of the leads during manual rework. For detailed IR reflow recommendations, refer to the Application information section.

Note 4: Temperature coefficient is measured by dividing the maximum change in output voltage by the specified temperature range.

Note 5: Line and load regulation are measured on a pulse basis for specified input voltage or load current ranges. Output voltage change due to die temperature change must be taken into account separately.

Note 6: Peak-to-peak noise is measured with a 2-pole highpass filter at 0.1Hz and 3-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads, and the test time is 10 seconds. Due to the statistical nature of noise, repeating noise measurements will yield larger and smaller peak values in a given measurement interval. By repeating the measurement for 1000 intervals, each 10 seconds long, it is shown that there are time intervals during which the noise is higher than in a typical single interval, as predicted by

ELECTRICAL CHARACTERISTICS

statistical theory. In general, typical values are considered to be those for which at least 50% of the units may be expected to perform similarly or better. For the 1000 interval test, a typical unit will exhibit noise that is less than the typical value listed in the Electrical Characteristics table in more than 50% of its measurement intervals. See Application Note 124 for noise testing details. RMS noise is measured with a spectrum analyzer in a shielded environment.

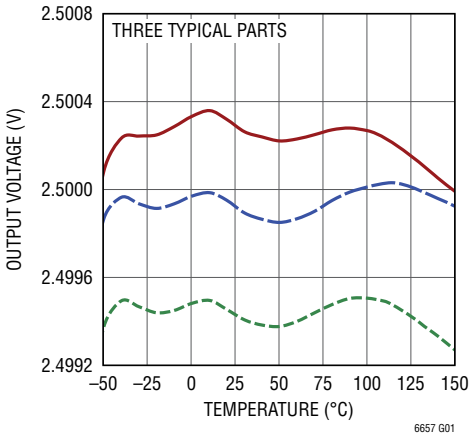
Note 7: Long term stability typically has a logarithmic characteristic and therefore change after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one third of the first thousand hours with a continuing trend toward reduced drift with time. Long-term stability will also be affected by differential stresses between the IC and the board material created during board assembly.

Note 8 : Hysteresis in output voltage is created by mechanical stress that depends on whether the IC was previously at a different temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. Hysteresis is roughly proportional to the square of the temperature change. For instruments that are stored at well controlled temperatures (within 30 degrees of the operational temperature), hysteresis is usually not a significant error source. Typical hysteresis is the larger change of 25°C to cold to 25°C, or 25°C to hot to 25°C, preconditioned by one thermal cycle.

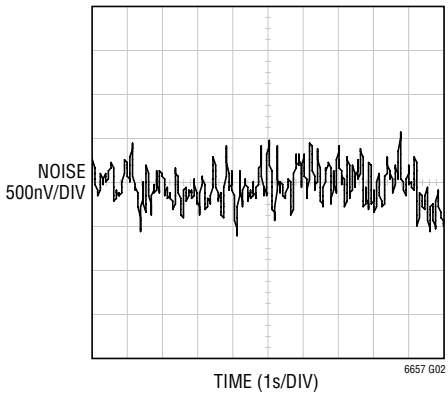
TYPICAL PERFORMANCE CHARACTERISTICS

The test conditions are T_A = 25°C, V_{IN} = V_{OUT} + 0.5V, $V_{\overline{SHDN}}$ = 1.6V, I_{OUT} = 0, C_{OUT} = 1µF, unless otherwise noted.

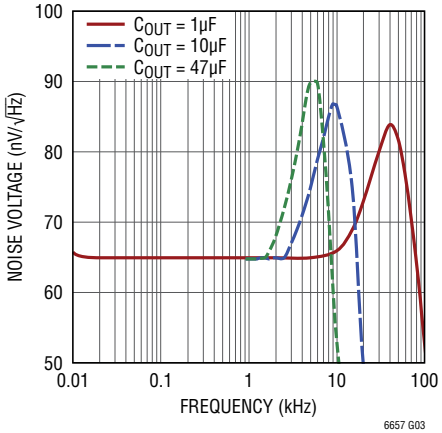
2.5V Output Voltage Temperature Drift



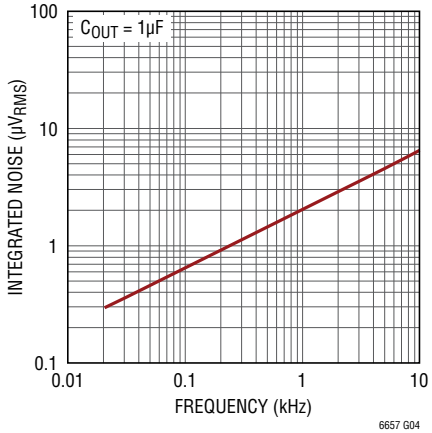
2.5V Low Frequency 0.1Hz to 10Hz Noise



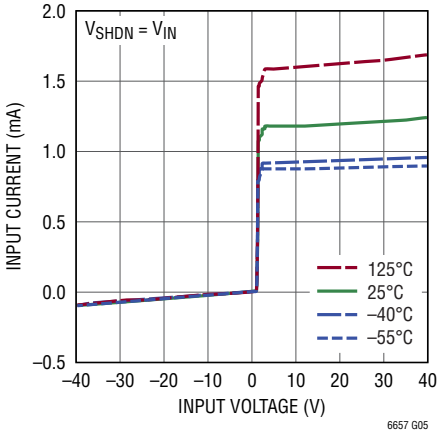
2.5V Output Voltage Noise Spectrum



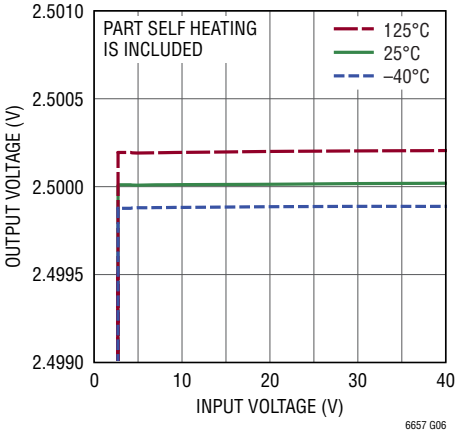
2.5V Integrated Noise 10Hz to 10kHz



2.5V Supply Current vs Input Voltage



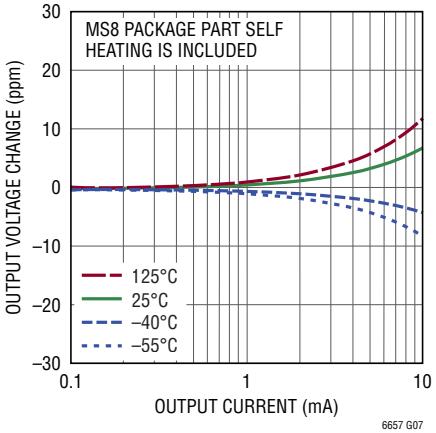
2.5V Line Regulation



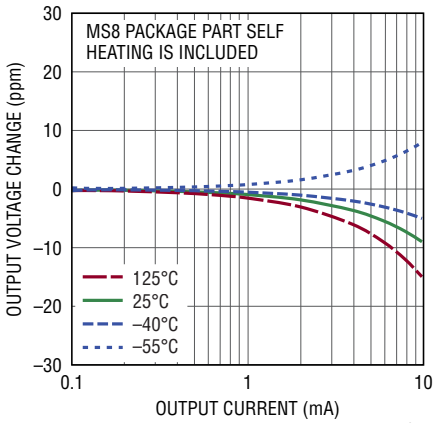
TYPICAL PERFORMANCE CHARACTERISTICS

The test conditions are T_A = 25°C, V_{IN} = V_{OUT} + 0.5V, $V_{\overline{SHDN}}$ = 1.6V, I_{OUT} = 0, C_{OUT} = 1µF, unless otherwise noted.

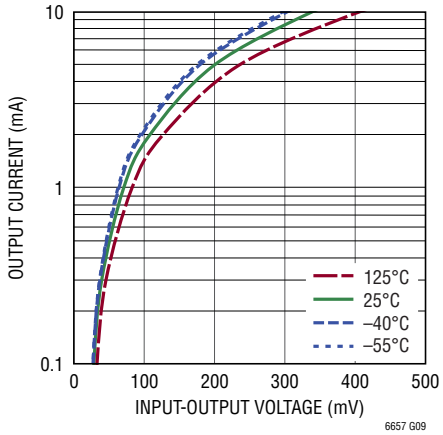
2.5V Load Regulation (Sourcing)



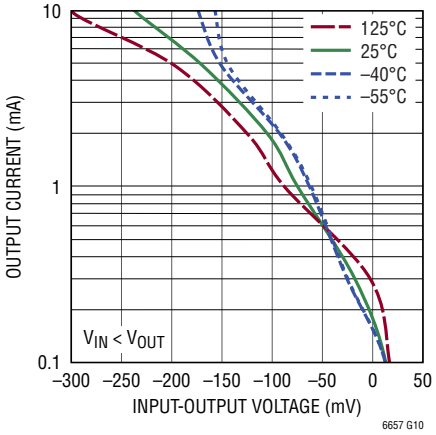
2.5V Load Regulation (Sinking)



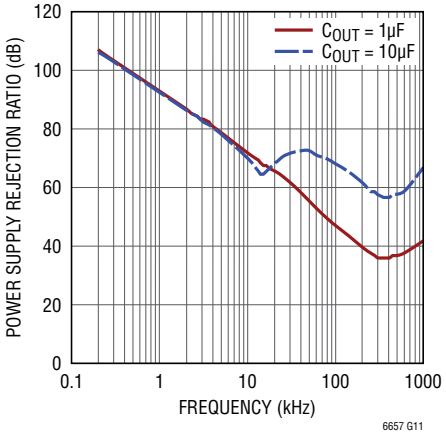
2.5V Minimum V_{IN} to V_{OUT} Differential (Sourcing)



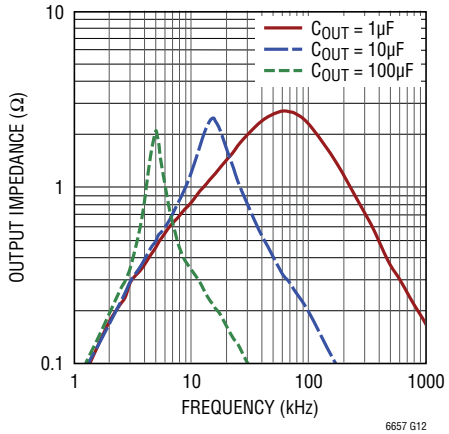
2.5V Minimum V_{IN} to V_{OUT} Differential (Sinking)



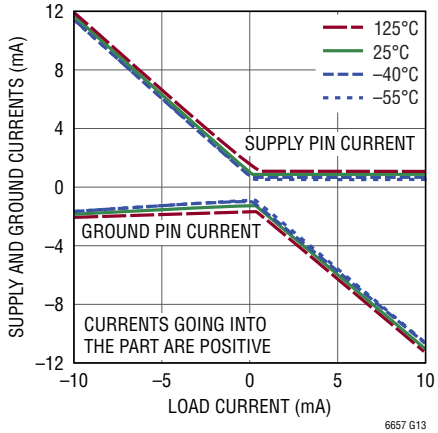
2.5V Power Supply Rejection Ratio vs Frequency



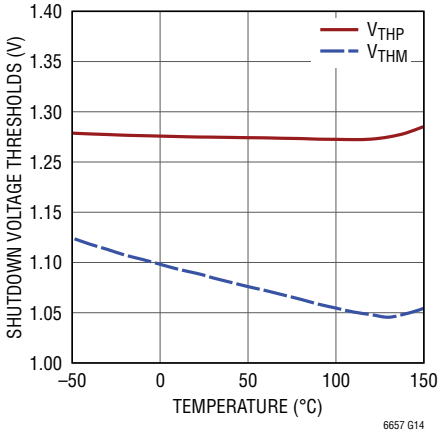
2.5V Output Impedance vs Frequency



Supply and Ground Currents vs Load Current



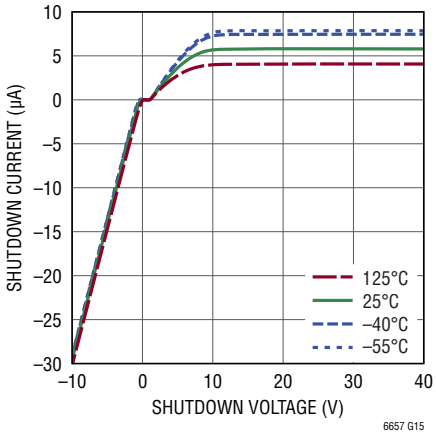
Shutdown Voltage Thresholds vs Temperature



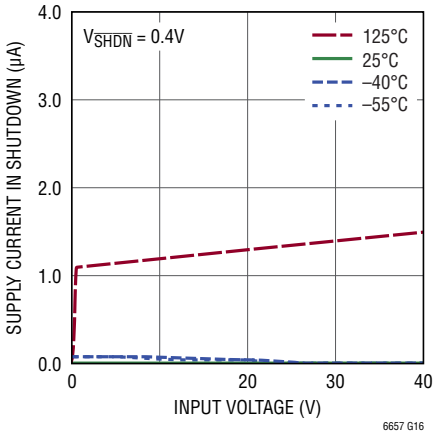
TYPICAL PERFORMANCE CHARACTERISTICS

The test conditions are T_A = 25°C, V_{IN} = V_{OUT} + 0.5V, $V_{\overline{SHDN}}$ = 1.6V, I_{OUT} = 0, C_{OUT} = 1µF, unless otherwise noted.

Shutdown Pin Current vs Shutdown Voltage



2.5V Supply Current in Shutdown vs Input Voltage



PIN FUNCTIONS

$\overline{SHDN}$ (Pin 3): Shutdown Input. This active low input disables the part to reduce supply current < 2µA. This pin must be driven externally and should be tied to V_{IN} if unused. It may be driven to logic high or to V_{IN} during normal operation.

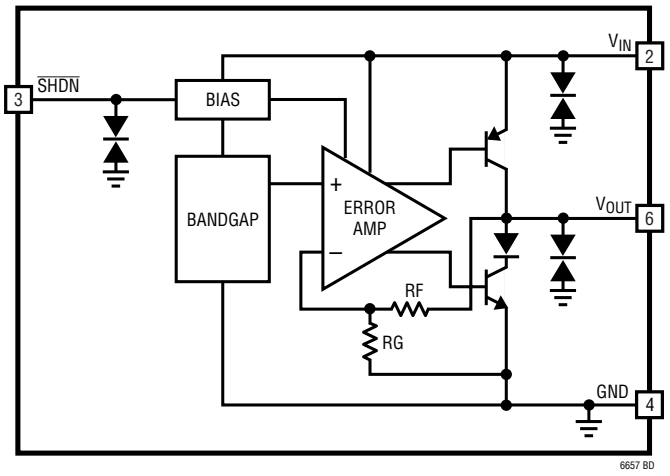
V_{IN} (Pin 2): Input Voltage Supply. Bypass V_{IN} with a local 0.1µF or larger capacitor to GND.

GND (Pin 4): Device Ground. This pin must be connected to a noise-free ground plane. A star-ground with related circuits will give the best results. Be careful of trace impedance, as the GND pin carries supply return current.

V_{OUT} (Pin 6): Reference Output Voltage. This pin can source and sink current to a load. An output capacitor of 1µF or higher is required for stability.

DNC (Pins 1, 5, 7, 8): Internal Functions. Do Not Connect or electrically stress these pins. These pins must be left floating and leakage currents from these pins should be kept to a minimum. Allow additional routing clearance.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Line and Load Regulation

The line regulation of the LT6657 is typically well below 1ppm/V. A 10V change in input voltage causes a typical output shift of only 2ppm. Load regulation is also less than 1ppm/mA in an MS8 package. A 5mA change in load current shifts output voltage by only 4ppm. These electrical effects are measured with low duty cycle pulses.

To realize such excellent load regulation the IR drops on the V_{OUT} and GND lines need to be minimized. One ounce copper foil printed circuit board has 0.5mΩ/square. Just 1mΩ of added trace resistance introduces an error of 1µV for each 1mA passing through it. This will add a 0.4ppm/mA to the load regulation with a 2.5V reference. These externally created errors have the same order of magnitude as the typical load regulation values for the LT6657. Minimizing wire resistance and using a separate ground return for the load will maintain excellent load regulation. When sourcing current, the ground connection pin can be used as kelvin sensing for improved output regulation.

Additional output changes due to die temperature change must be taken into account separately. These added effects may be estimated from:

$$\text{Line\_Reg (in ppm)} = (I_{IN} + I_{OUT}) \bullet \theta_{JA} \bullet TC \bullet V_{IN}$$

$$\text{Load\_Reg (in ppm)} = (V_{IN} - V_{OUT}) \bullet \theta_{JA} \bullet TC \bullet I_{OUT}$$

Where voltages are in V, currents are in mA, package thermal resistance θ_{JA} is in °C/mW, and temperature coefficient, TC, is in ppm/°C. For example, with typical quiescent current I_{IN} = 1.2mA, I_{OUT} = 1mA, $V_{IN} - V_{OUT}$ = 1V, the added line-regulation is typically 0.66ppm/V and added load-regulation is typically 0.3ppm/mA for a TC of 1ppm/°C and MSOP-8 package with θ_{JA} = 0.3°C/mW thermal resistance.

Bypass and Load Capacitors

The LT6657 voltage reference requires a 0.1µF or larger input capacitor placed close to the part to improve power supply rejection. A long input wire with large series inductance can create ringing response to large load transients.

The output requires a capacitor of 1µF or higher placed near the part. Frequency stability, turn-on time and settling behavior are directly affected by the value and type of the output capacitor. Equivalent resistance in series with the output capacitor (ESR) introduces a zero in the output buffer transfer function and can cause instability. It is recommended to keep the ESR less than 0.5Ω to maintain sufficient phase margin. Both capacitance and ESR are frequency dependent. At higher frequencies, capacitance drops and ESR increases. To ensure stability above 100kHz, the output capacitor must also have suitable characteristics above 100kHz. The following paragraphs describe capacitors with suitable performance.

For applications requiring a large output capacitor, a low ESR ceramic capacitor in parallel with a bulk tantalum capacitor provides an optimally damped response. For example, a 47µF tantalum capacitor with larger ESR in parallel with a 10µF ceramic capacitor with ESR smaller than 0.5Ω improves transient response and increases phase margin.

Give extra consideration to the use of ceramic capacitors such as X7R types. These capacitors are small, come in appropriate values and are relatively stable over a wide temperature range. However, for low noise requirements, X7R capacitors may not be suitable as they may exhibit a piezoelectric effect. Mechanical vibrations cause a charge displacement in the ceramic dielectric and the resulting perturbations can appear as noise.

For very low noise applications, film capacitors should be considered for their lack of piezoelectric effects. Film capacitors such as polyester, polycarbonate and polypropylene have good temperature stability. Additional care must be taken as polypropylene have an upper limit of 85°C to 105°C. Above these temperatures the working voltage often needs to be derated per manufacturer specifications. Another type of film capacitor is polyphenylene sulfide (PPS). These capacitors work over a wide temperature range, are stable and have large capacitance values beyond 1µF.

In voltage reference applications, film capacitor lifetime is affected by temperature and applied voltage. Capacitor lifetime is degraded by operating near or exceeding the rated voltage, at high temperature, with AC ripple or some combination of these. Most voltage reference applications present AC ripple only during transient events.

APPLICATIONS INFORMATION

Turn-On and Line Transient Response

The turn-on time is slew-limited and determined by the short-circuit current, the output capacitor, and the output voltage value as determined by the equation:

$$t_{ON} = V_{OUT} \bullet \frac{C_{OUT}}{I_{SC}}$$

For example, the LT6657-2.5V, with a 1µF output capacitor and a typical current limit of 15mA the turn-on time would be:

$$t_{ON} = 2.5V \bullet \frac{1\mu F}{15mA} = 167\mu s$$

The resulting turn-on time is shown in Figure 1.

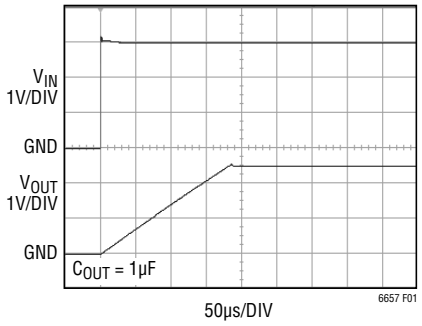


Figure 1. 2.5V Turn-On Characteristics

Line transient response with a 1µF output capacitor and no output current is shown in Figure 2. The peak voltage output response is less than 1mV.

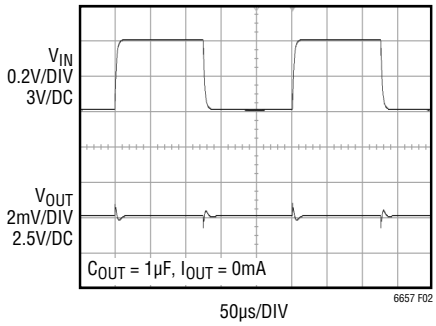


Figure 2. Line Transient Response with V_{IN} = 0.4V_{P-P}

Increasing the output load speeds up the response (Figure 3).

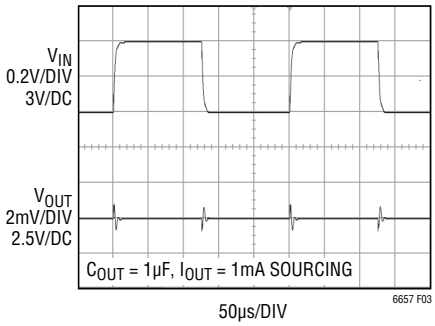


Figure 3. Line Transient Response with V_{IN} = 0.4V_{P-P}

A larger output capacitor lowers the amplitude response with a longer time response trade-off (Figure 4).

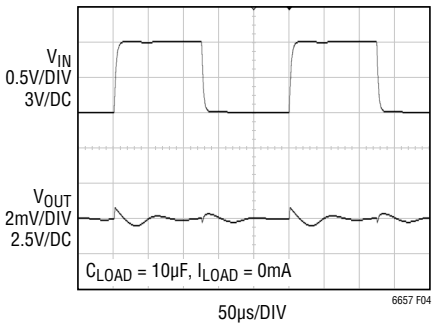


Figure 4. Line Transient Response with V_{IN} = 1V_{P-P}

Load Transient Response

The test circuit of Figure 5 is used to measure load transient response with various currents.

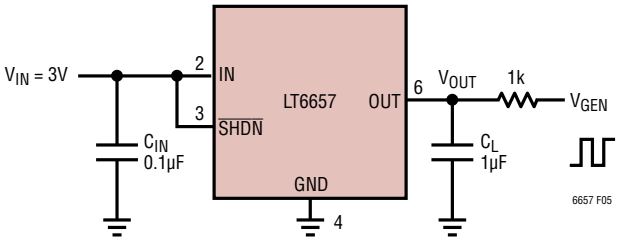


Figure 5. Transient Load Test Circuit

APPLICATIONS INFORMATION

Figure 6 and 7 shows the load transient response to a 5mA current step both sourcing and sinking.

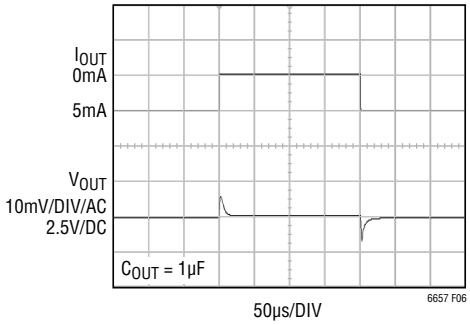


Figure 6. Output Response with a 5mA Load Step Sourcing

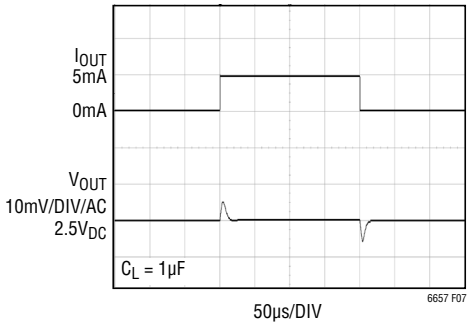


Figure 7. Output Response with a 5mA Load Step Sinking

Figure 8 and 9 shows the load transient response to a smaller 4mA to 5mA current step while sourcing and sinking.

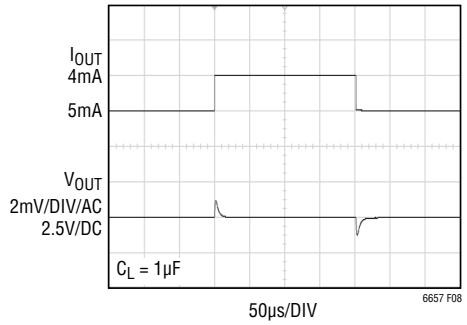


Figure 8. Output Response with a 4mA to 5mA Load Step Sourcing

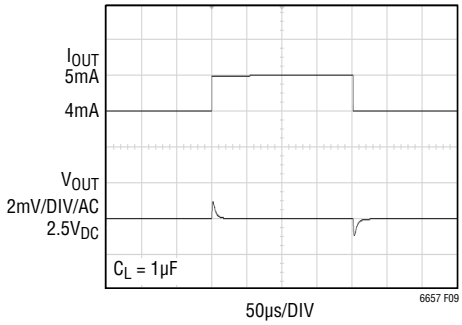


Figure 9. Output Response with a 4mA to 5mA Load Step Sinking

Figures 10 and 11 show the load transient response to an even smaller 0.5mA current step both sourcing and sinking.

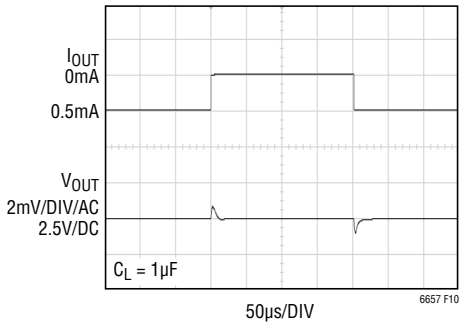


Figure 10. Output Response with a 0.5mA Load Step Sourcing

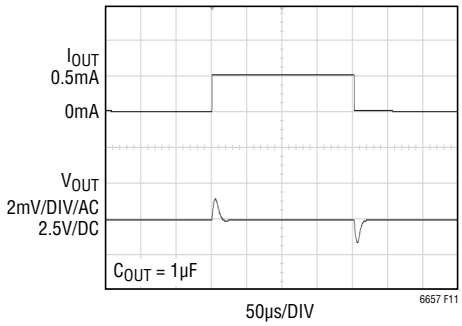


Figure 11. Output Response with a 0.5mA Load Step Sinking

APPLICATIONS INFORMATION

LT6657 Sinking Current Dropout Description

The LT6657 output stage can source and sink current of equal magnitude. When sourcing current it performs as a conventional low dropout regulating device. When sinking current, it can maintain a regulated output with an input voltage equal to, more positive than, or also slightly less than the output voltage. The specification for dropout voltage while sinking is expressed in negative voltage values for $V_{IN} - V_{OUT}$. A typical unit will maintain a regulated output voltage while sinking current with an input voltage 250mV (50mV guaranteed) below the output voltage. Lower input voltage will cause the output to drop out of regulation. This allows shunt reference applications where the output and input can be tied together and sink current from the output to ground.

Positive or Negative Shunt Mode Operation

In addition to the series mode operation, the LT6657 can be operated in shunt mode. In this mode the reference is wired as a two terminal circuit which can be used both as a positive or a negative voltage reference, as shown in Figures 12 and 13.

R_{SHUNT} is chosen using the following formula:

$$R_{SHUNT} = \frac{V_{DD} - V_{OUT}}{I_{SHUNT\_MAX}}$$

where: $I_{SHUNT\_MAX} = 2.5mA + I_{OUT\_MAX}$

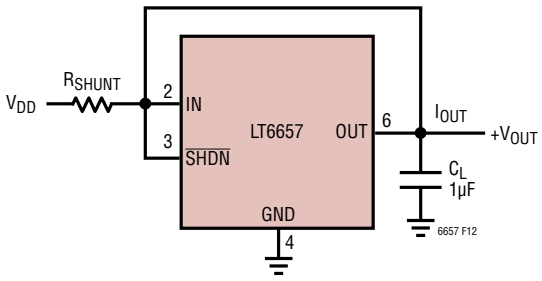


Figure 12. Positive Shunt Mode Operation

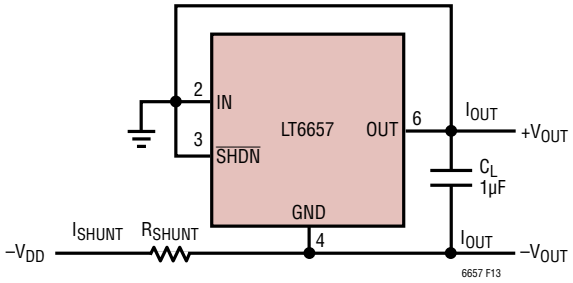


Figure 13. Negative Shunt Mode Operation

The I_{SHUNT} current has to be operated above 2.5mA to obtain the same performance as the series mode operation. In shunt mode operation I_{OUT_MAX} is less than or equal to 8.5mA. A C_L of 1µF or more is required on the output for stability.

Shutdown Mode

When the $\overline{SHDN}$ pin is pulled below 0.8V with respect to ground, the LT6657 enters a low power state and turns the output off. Quiescent current is typically 2µA. If $\overline{SHDN}$ is set less than 0.4V the quiescent current drops to 0.01µA typical. The $\overline{SHDN}$ pin turn-on threshold is 1.26V and it has approximately 150mV hysteresis for the turn-off threshold. The turn-on logic high voltage is 1.6V. Drive the $\overline{SHDN}$ with either logic or an open-collector/drain with a pull-up resistor. The resistor supplies the pull-up current to the open-collector/drain logic, normally several microamperes, plus the $\overline{SHDN}$ pin current, typically less than 5µA at 6V. If unused, connect the $\overline{SHDN}$ input pin to V_{IN}.

Power Dissipation

Power dissipation for LT6657 depends on V_{IN}, load current and the package type. The MSOP-8 package has a thermal resistance of $\theta_{JA} = 273°C/W$.

Although the maximum junction temperature is 150°C ,for best performance it is recommended to limit the change in junction temperature as much as possible. The plot in

APPLICATIONS INFORMATION

Figure 14 shows the maximum ambient temperature limits for different V_{IN} and load condition using a maximum junction temperature of 125°C in the MSOP-8 package. If the load current exceeds 10mA the parts could begin to current limit. In this case, the output voltage is no longer regulated and the part could dissipate much more power and operate hotter than the graph shows.

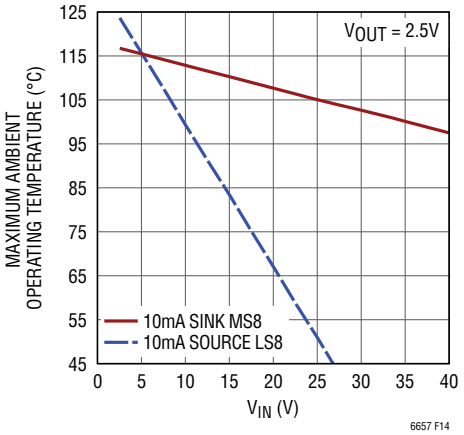


Figure 14. Maximum Ambient Operating Temperature

With a large input voltage and sourcing current, an internal thermal shutdown protection circuit limits the maximum power dissipation. When sinking current, there is no need for thermal shutdown protection because the power dissipation is much smaller and the sinking current limit will give some load protection.

Noise Performance and Specification

The LT6657 offers exceptional low noise for a bandgap reference; only $0.5ppm_{P-P}$ in the 0.1Hz to 10Hz bandwidth. As a result system noise performance may be dominated by system design and physical layout. Care is required to achieve the best possible noise performance. The use of dissimilar metals in component leads and PC board traces creates thermocouples. Variations in thermal resistance, caused by uneven air flow over the circuit board create differential lead temperature, thereby creating a thermoelectric voltage noise at the output of the reference. Minimizing the number of thermocouples, as well as limiting airflow, can substantially reduce these errors. Additional information can be found in Linear Technology Application Note 82.

Position the input and load capacitors close to the part. Although the LT6657 has 130dB DC PSRR, the power supply should be as stable as possible to guarantee optimal performance. A plot of the 0.1Hz to 10Hz low frequency noise is shown in the Typical Performance Characteristics section. Noise performance can be further improved by wiring several LT6657s in parallel as shown in the Typical Applications Section. With this technique the noise is reduced by $\sqrt{N}$, where N is the number of LT6657s used.

Noise in any frequency band is a random function based on physical properties such as thermal noise, shot noise, and flicker noise. The most precise way to specify a random error such as noise is in terms of its statistics, for example as an RMS value. This allows for relatively simple maximum error estimation, generally involving assumptions about noise bandwidth and crest factor. Unlike wideband noise, low frequency noise, typically specified in a 0.1Hz to 10Hz band, has traditionally been specified in terms of expected error, illustrated as peak-to-peak error. Low frequency noise is generally measured with an oscilloscope over a 10 second time frame. This is a pragmatic approach, given that it can be difficult to measure noise accurately at low frequencies, and that it can also be difficult to agree on the statistical characteristics of the noise, since flicker noise dominates the spectral density. While practical, a random sampling of 10 second intervals is an inadequate method for representation of low frequency noise, especially for systems where this noise is a dominant limit of system performance. Given the random nature of noise, the output voltage may be observed over many time intervals, each giving different results. Noise specifications that were determined using this method are prone to subjectivity, and will tend toward a mean statistical value, rather than the maximum noise that is likely to be produced by the device in question.

Because the majority of voltage reference data sheets express low frequency noise as a typical number, and as it tends to be illustrated with a repeatable plot near the mean of a distribution of peak-to-peak values, the LT6657 data sheet provides a similarly defined typical specification in order to allow a reasonable direct comparison against similar products. Data produced with this method generally

APPLICATIONS INFORMATION

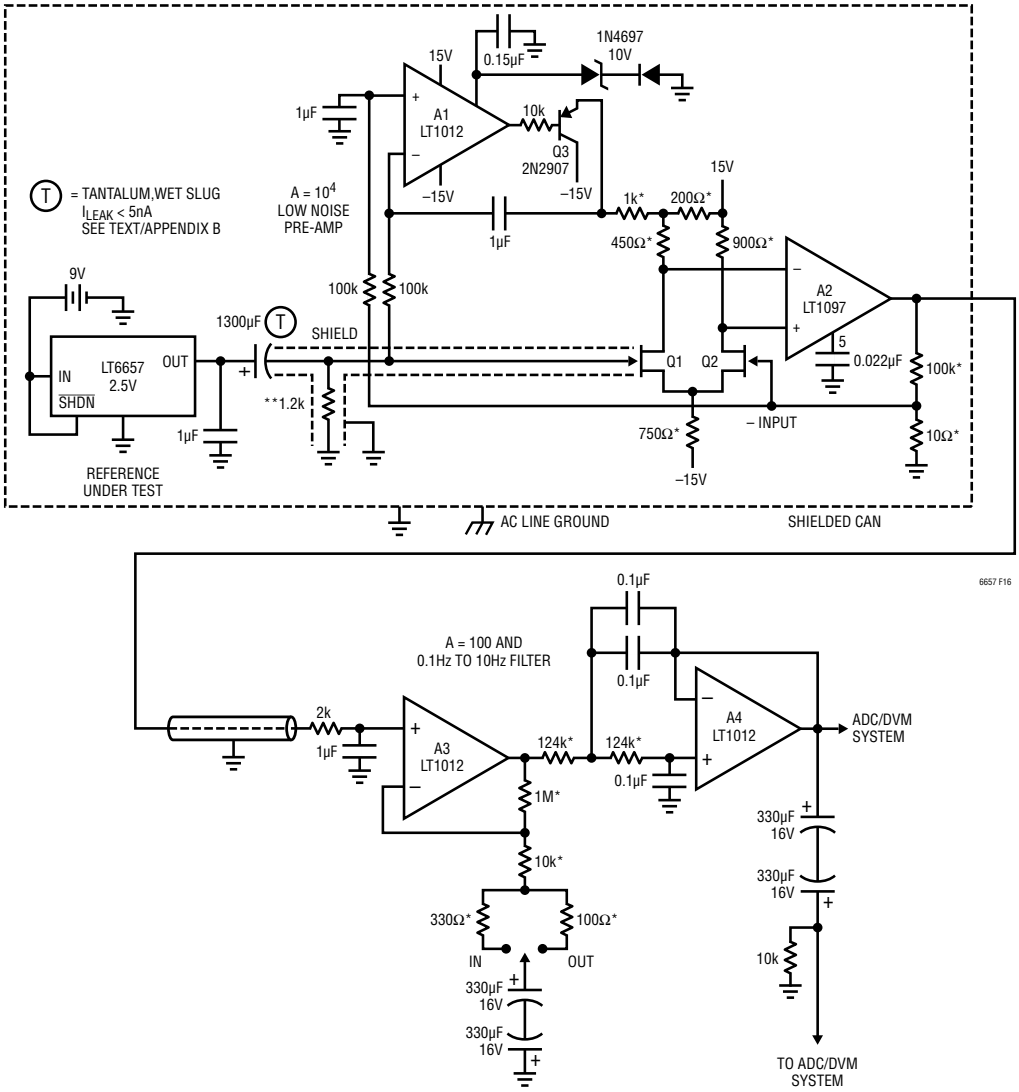


Figure 15. LT6657 Noise Test Circuitry (from AN124)

suggests that in a series of 10 second output voltage measurements, at least half the observations should have a peak-to-peak value that is below this number. For example, the LT6657-2.5 measures less than 0.5ppm$_{P-P}$ in at least 50% of the 10 second observations.

As mentioned above, the statistical distribution of noise is such that if observed for long periods of time, the peak error in output voltage due to noise may be much larger than that observed in a smaller interval. The likely maximum error due to noise is often estimated using the RMS value, multiplied by an estimated crest factor, assumed to be in the range of 6 to 8.4. This maximum possible value will only be observed if the output voltage is measured for very long periods of time. Therefore, in addition to the common method, a more thorough approach to measuring noise has been used for the LT6657 (described in detail in Linear Technology's AN124) that allows more information to be obtained from the result. In particular, this method characterizes the noise over a significantly greater length of time, resulting in a more complete description of low frequency noise. The reference noise is measured at the output of the circuit shown in Figure 15 with an ADC/DVM

APPLICATIONS INFORMATION

system. Peak-to-peak voltage is then calculated for 10 second intervals over hundreds of intervals. The results are then summarized in terms of the fraction of measurement intervals for which observed noise is below a specified level. For example, the LT6657-2.5 measures less than 0.55ppm$_{P-P}$ in 80% of the measurement intervals, and less than 0.59ppm$_{P-P}$ in 95% of observation intervals. The preamplifier and filter are shown in Figure 15. This statistical variation in noise is illustrated in Figure 16.

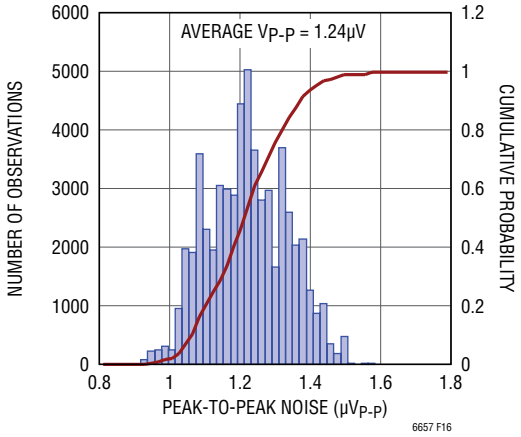


Figure 16. LT6657 Low Frequency Noise Histogram

This method of testing low frequency noise is more practical than common methods. The results yield a comprehensive statistical description, rather than a single observation. In addition, the direct measurement of output voltage over time gives an actual representation of peak noise, rather than an estimate based on statistical assumptions such as crest factor.

Hysteresis

Thermal hysteresis is a measure of change of output voltage as a result of temperature cycling. Figure 17 illustrates the typical hysteresis based on data taken from the LT6657-2.5. A proprietary design technique minimizes thermal hysteresis. The LT6657 is capable of dissipating relatively high power. For example, with a 40V input voltage and 5mA source load current applied to the LT6657-2.5, the power dissipation is PD = 40V • 1.4mA + 37.5V • 5mA = 244mW, which causes an increase in the die temperature of 73°C in MSOP-8 package. This could increase the junction temperature above 125°C and may cause the output to shift due to thermal hysteresis each time the device is powered up.

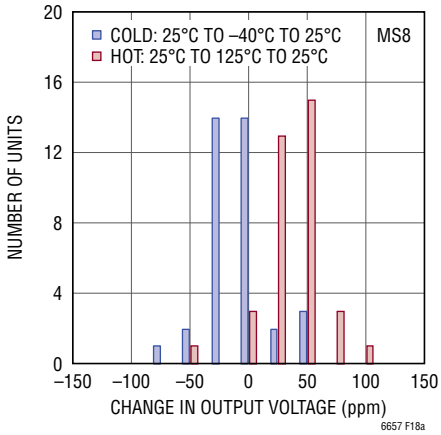


Figure 17. ΔV_{OUT} Due to Thermal Hysteresis

Long-Term Drift

The LT6657 drift data was taken on 40 parts that were soldered into PC boards similar to a real world application. The boards were then placed into a constant temperature oven with TA = 35°C, their outputs scanned regularly and measured with an 8.5 digit DVM. Typical long-term drift is illustrated in Figure 18.

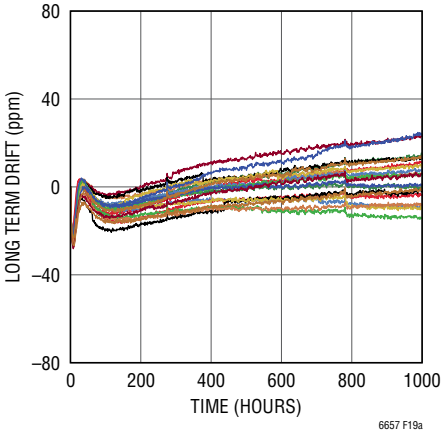


Figure 18. Long-Term Drift MS8

APPLICATIONS INFORMATION

PC Board Layout Stress

The LT6657 is a very stable reference over temperature with less than 1.5ppm/°C error as shown in the Electrical Characteristics table. The mechanical stress caused by soldering parts to a printed circuit board may cause the output voltage to shift and the die temperature coefficient to change. The PC Board can affect all aspects of stability, including long term stability, thermal hysteresis and humidity stability. See Linear's AN82 for more detailed information.

IR Reflow Shift

The mechanical stress of soldering a part to a board can cause the output voltage to shift. Moreover, the heat of an IR reflow or convection soldering oven can also cause the output voltage to shift. The materials that make up a semiconductor device and its package have different rates of expansion and contraction. After a part undergoes the extreme heat of a lead-free IR reflow profile, like the one shown in Figure 19, the output voltage shifts. After the device expands, due to the heat, and then contracts, the stresses on the die move. This shift is similar to, but larger than thermal hysteresis.

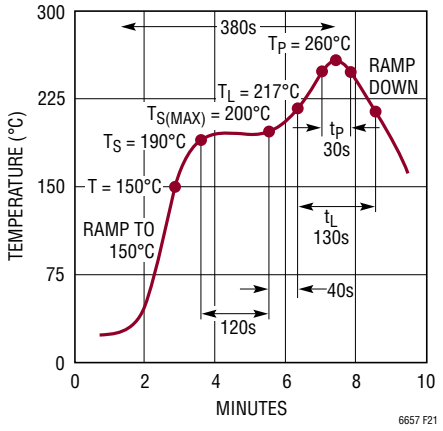


Figure 19. Lead-Free Reflow Profile

Experimental results of IR reflow shift are shown in Figure 20 for MS8. These results show only shift due to reflow and not mechanical stress.

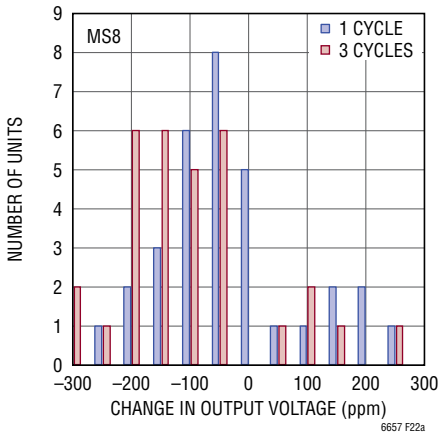
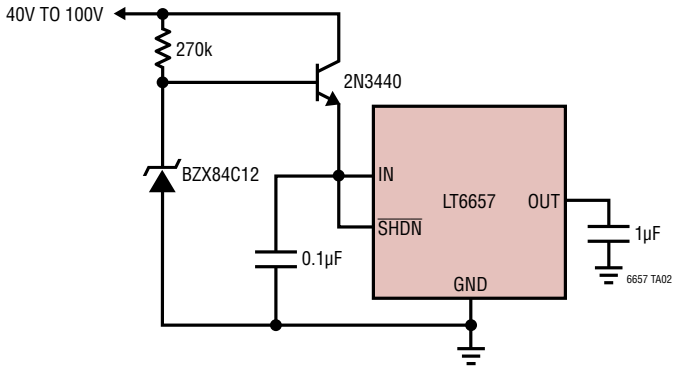


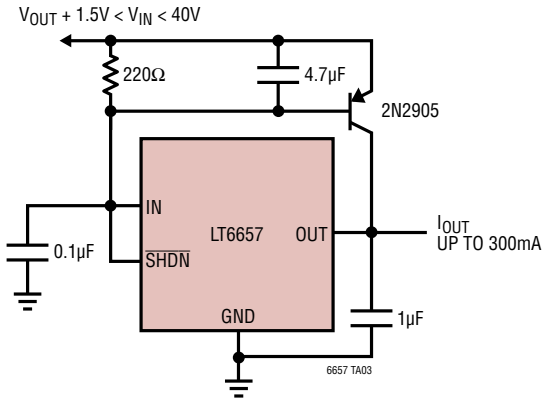
Figure 20. ΔV_{OUT} Due to IR Reflow (MS8 Package), Peak Temperature = 260°C

TYPICAL APPLICATIONS

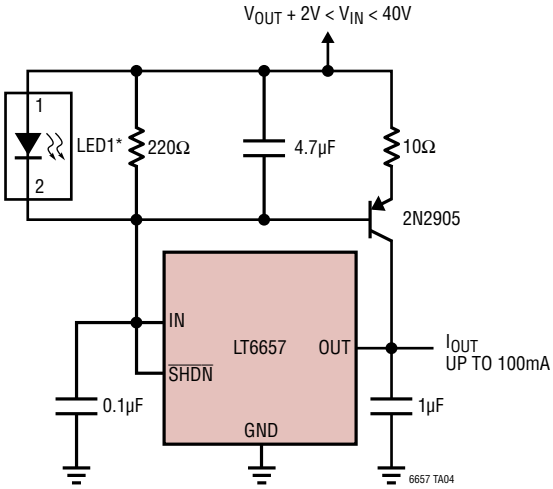
Extended Supply Range Reference



Boosted Output Current Reference

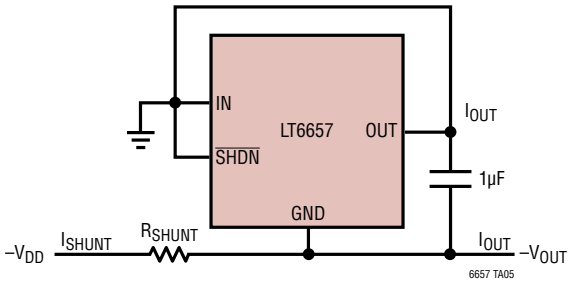


Boosted Output Current with Current Limit



*LED CANNOT BE OMMITTED THE LED CLAMPS THE VOLTAGE DROP ACROSS THE 220Ω AND LIMITS OUTPUT CURRENT

Negative Shunt Mode Reference

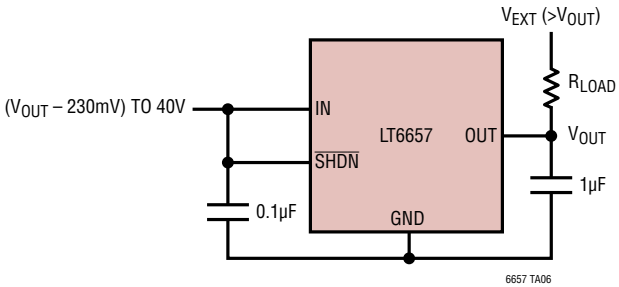


$$R_{SHUNT} = \frac{V_{DD} - V_{OUT}}{I_{SHUNT\_MAX}}$$

$$I_{SHUNT\_MAX} = 2.5mA + I_{OUT\_MAX}$$

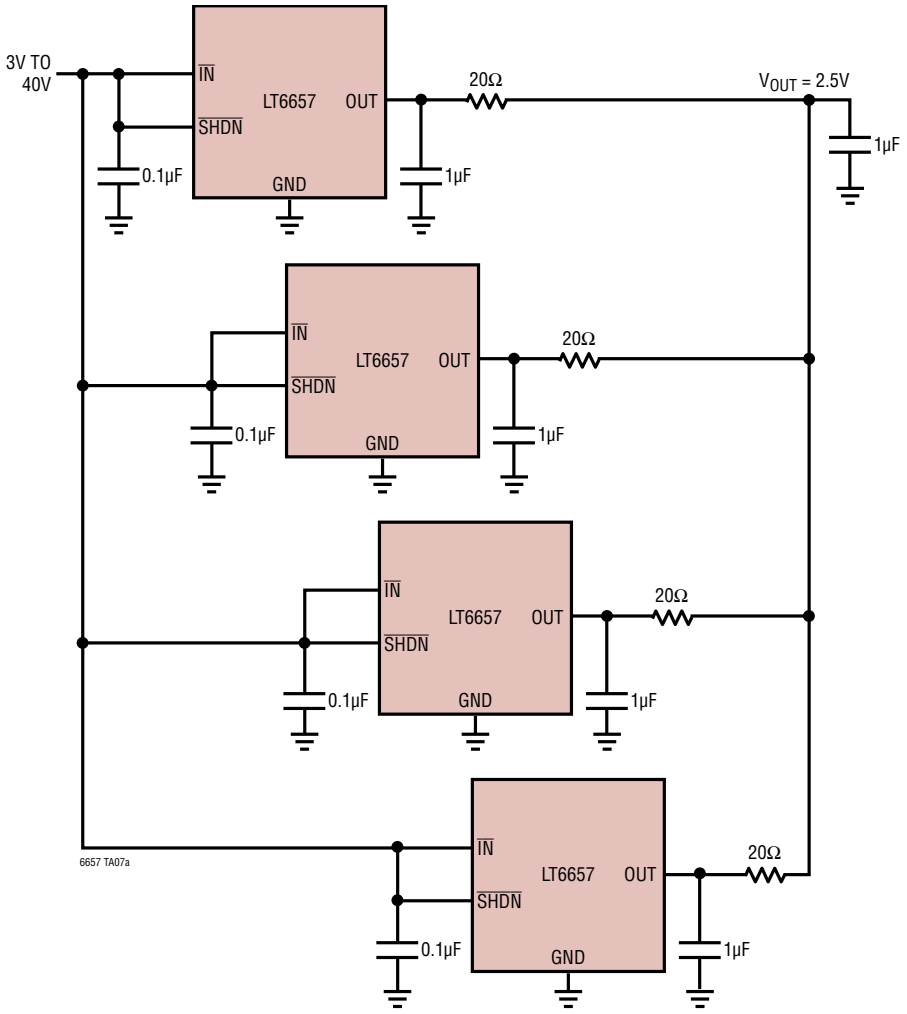
$$I_{OUT\_MAX} < 8.5mA$$

Sinking Current from External Circuitry

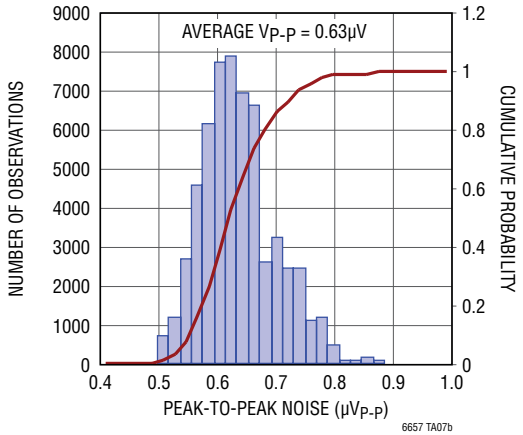


TYPICAL APPLICATIONS

Low Noise Statistical Averaging Reference
$e_{NOUT} = e_N/\sqrt{N}$ Where N is the Number of LT6657s in Parallel



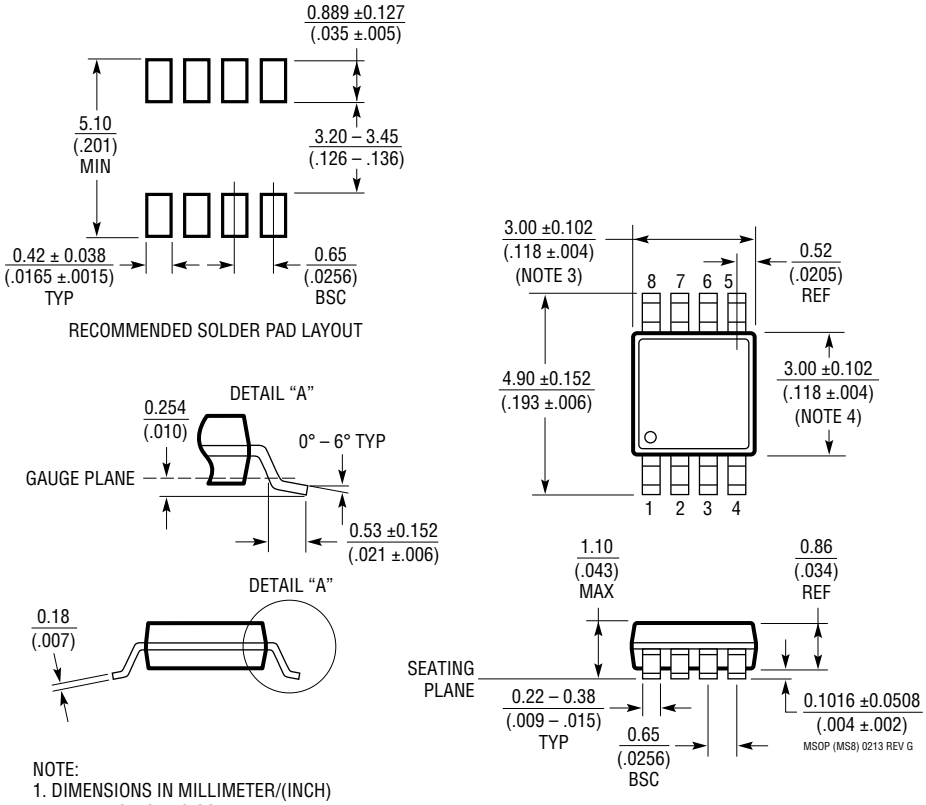
Low Frequency Noise (0.1Hz to 10Hz) with Four LT6657s in Parallel



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

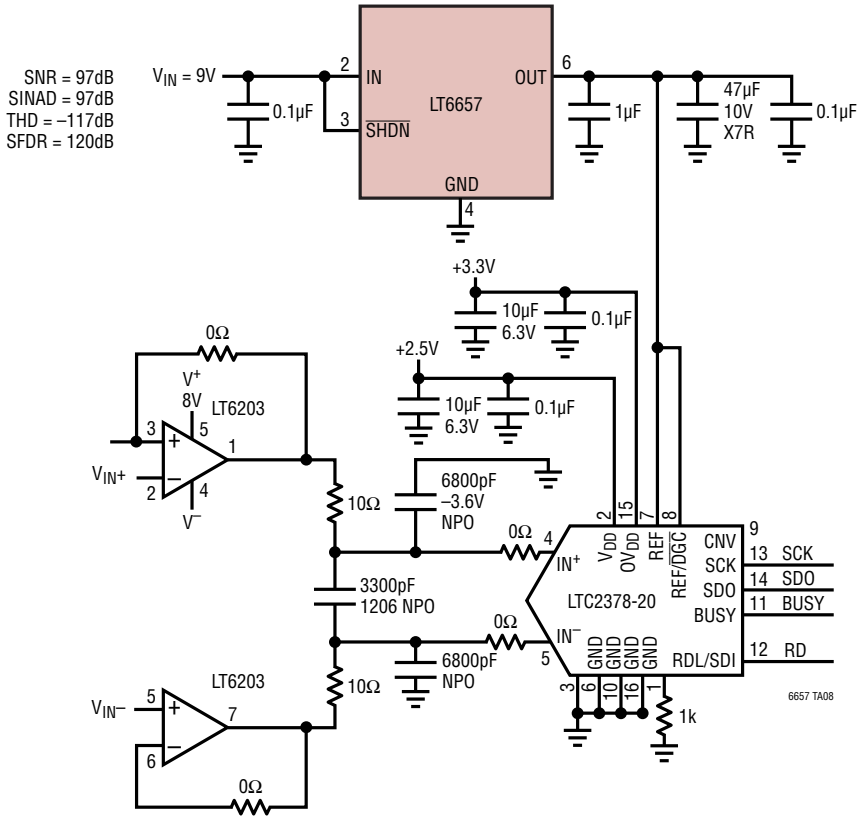
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Low Noise Precision 20-Bit Analog-to-Digital Converter Application



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1236	Precision Low Drift, Low Noise Reference	0.05% Max, 5ppm/°C Max, 1ppm (Peak-to-Peak) Noise
LT1460	Micropower Series References	0.075% Max, 10ppm/°C Max, 20mA Output Current
LT1461	Micropower Series Low Dropout	0.04% Max, 3ppm/°C Max, 50mA Output Current
LT1790	Micropower Precision Series References	0.05% Max, 10ppm/°C Max, 60µA Supply, SOT23 Package
LT6660	Tiny Micropower Series Reference	0.2% Max, 20ppm/°C Max, 20mA Output Current, 2mm × 2mm DFN
LT6650	Micropower Reference with Buffer Amplifier	0.5% Max, 5.6µA Supply, SOT23 Package
LTC6652	High Precision, Buffered Voltage Reference Family	0.05% Max Initial Error, 5ppm/°C Max Drift, Shutdown Current <2µA, –40°C to 125°C Operation
LT6654	Low Noise, High Voltage, High Output Drive Voltage Reference Family	1.6ppm Peak-to-Peak Noise (0.1Hz to 10Hz), Sink/Source ±10mA, 10ppm/°C Max Drift, –40°C to 125°C Operation
LTC6655	Precision, Very Low Noise and Temperature Drift, Voltage Reference Family	0.25ppm Peak-to-Peak Noise (0.1Hz to 10Hz), Sink/Source ±5mA, 0.025% Max, 2ppm/°C Max Drift, –40°C to 125°C Operation
LT6656	Ultra Low Current Series Voltage Reference Family	Supply current < 1µA, 0.05% Max, 10ppm/°C, Sink/Source ±5mA

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