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Evaluating the GaAs, pHEMT, MMIC, Single Positive Supply, DC to 10 GHz Power Amplifier

FEATURES

Dual-layer Rogers 4350 evaluation board with heat sink
End launch, 2.9 mm, RF connectors
Through calibration path

EVALUATION KIT CONTENTS

ADPA9002-EVALZ evaluation board

EQUIPMENT NEEDED

RF signal generator
RF spectrum analyzer
RF network analyzer
12 V and 1 A power supply
−2 V and 100 mA power supply

GENERAL DESCRIPTION

The ADPA9002-EVALZ consists of a dual-layer printed circuit board (PCB) fabricated from 10 mil thick, Rogers 4350B, copper clad mounted to an aluminum heat sink. The heat sink assists in providing thermal relief to the ADPA9002 as well as mechanical support to the PCB. Mounting holes on the heat sink allow attachment to larger heat sinks for improved thermal management. The RFIN and RFOUT ports on the ADPA9002-EVALZ are populated with 2.9 mm, female, coaxial connectors (J1 and J2) and the corresponding RF traces have a 50 Ω characteristic impedance. The ADPA9002-EVALZ is populated with components suitable for use over the entire −40°C to +85°C operating temperature range of the ADPA9002. To calibrate board trace losses, a through calibration path is provided between the J5 and J6 connectors. J5 and J6 must be populated with RF connectors to use the through calibration path. Refer to Table 2 and Figure 3 for the through calibration path performance.

The device ground path and gate control voltage are accessed through the 4-pin headers, J3 and J4 (see Table 1 for header connections).

The RF traces on the ADPA9002-EVALZ are 50 Ω, grounded coplanar waveguide. The package ground leads and the exposed pad connect directly to the ground plane. Multiple vias connect the top and bottom ground planes with particular focus on the area directly beneath the ground paddle to provide adequate electrical conduction and thermal conduction to the heat sink.

The power supply decoupling capacitors on the ADPA9002-EVALZ represent the configuration that was used to characterize and qualify the device. A scope can be used to reduce the number of capacitors, but the scope varies from system to system. It is recommended to first remove or combine the largest capacitors that are farthest from the ADPA9002 when modifying the capacitor configurations.

For full details on the ADPA9002, see the ADPA9002 data sheet, which must be consulted in conjunction with this user guide when using the ADPA9002-EVALZ.

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REVISION HISTORY

10/2019—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

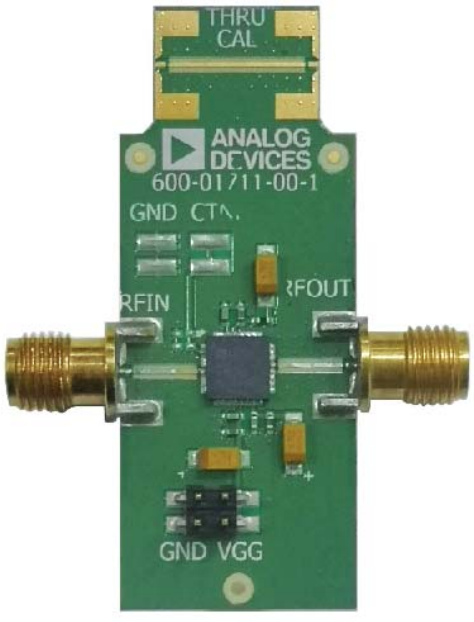

Figure 1. ADPA9002-EVALZ Primary Side

Figure 2. ADPA9002-EVALZ Secondary Side

OPERATING THE ADPA7006-EVALZ

The ADPA9002 operates in either self biased mode or externally biased mode. Ground the V_{GG1} pin through the J4 headers to operate in self biased mode. To operate in externally biased mode, adjust the V_{GG1} voltage through the J4 headers to be from −2 V to +0.5 V to set the desired quiescent current (I_{DQ}).

POWER-UP

The biasing sequence to use for self biased operation during power-up is as follows:

1. Connect all device GND pins to dc ground and RF ground.
2. Set the drain voltage to 12 V through the RFOUT/V_{DD} pin.
3. Apply the RF signal through the RFIN port.

The biasing sequence to use for externally biased operation during power-up is as follows:

1. Connect all device GND pins to dc ground and RF ground.
2. Set the gate voltage to −2 V through the V_{GG1} pin.
3. Set the RFOUT/V_{DD} voltage to 12 V.
4. Gradually adjust the V_{GG1} voltage to achieve the I_{DQ}.
5. Apply the RF signal through the RFIN port.

POWER-DOWN

The biasing sequence to use for self biased operation during power-down is as follows:

1. Turn off the RF signal.
2. Set the RFOUT/V_{DD} voltage to 0 V.

The biasing sequence to use for externally biased operation during power-down is as follows:

1. Turn off the RF signal.
2. Decrease the V_{GG1} voltage to −2 V to achieve a typical I_{DQ} of 0 mA.
3. Set the RFOUT/V_{DD} voltage to 0 V.
4. Set the V_{GG1} pin voltage to 0 V.

Table 1. J3 and J4 Header Connections to ADPA9002

Connector	Header	ADPA9002 Pin
J3	1, 2, 3, 4	Not connected
J4	2, 4	GND
J4	1, 3	V_{GG1}

Table 2. Insertion Loss of Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
0.01	0.00
0.160	−0.07
1	−0.24
2	−0.36
3	−0.48
4	−0.45
5	−0.5
6	−0.55
7	−0.61
8	−0.64
9	−0.65
10	−0.65

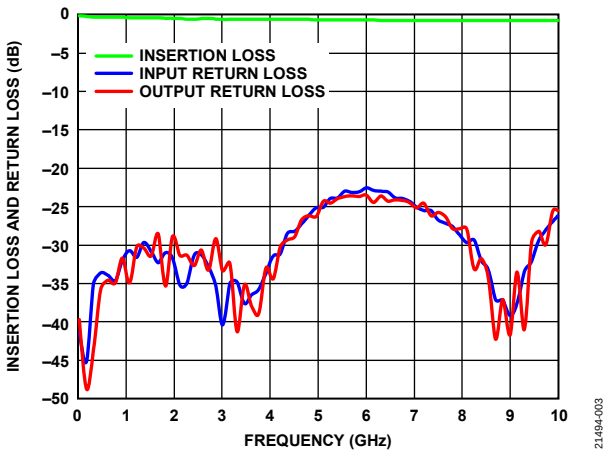

Figure 3. Insertion Loss and Return Loss of Through Calibration Path

EVALUATION BOARD SCHEMATIC AND ARTWORK

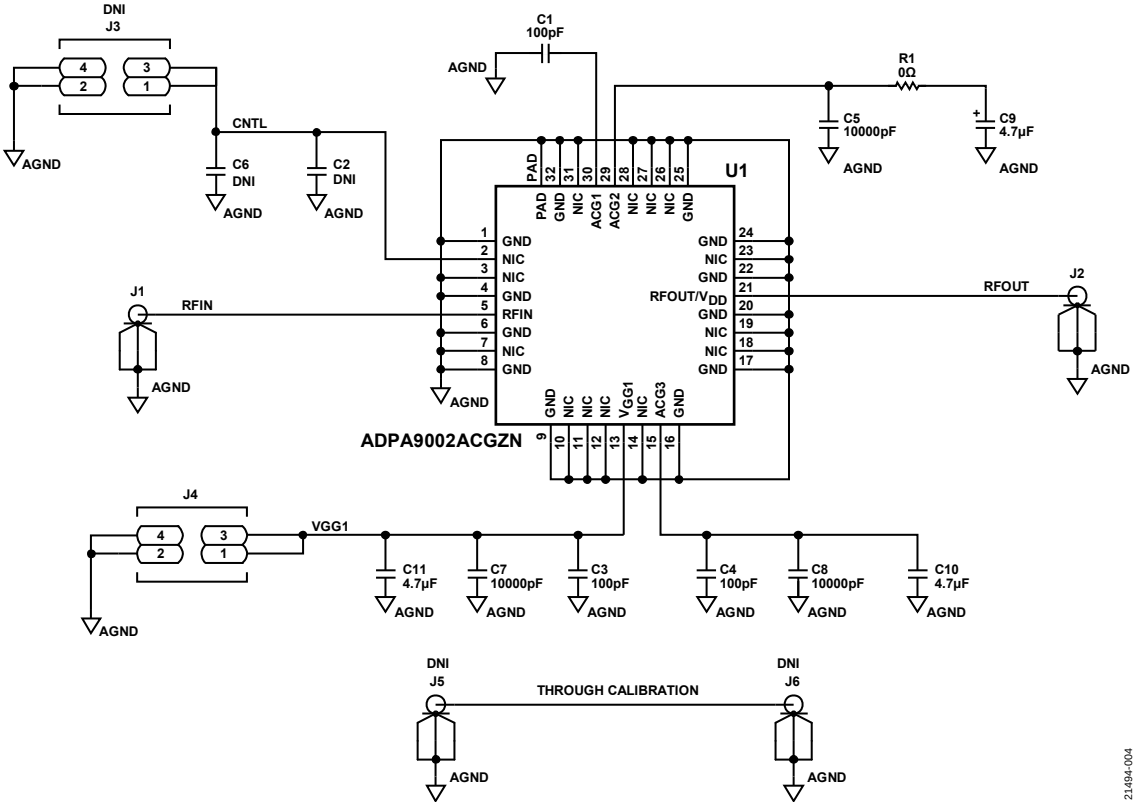

Figure 4. ADPA9002-EVALZ Schematic

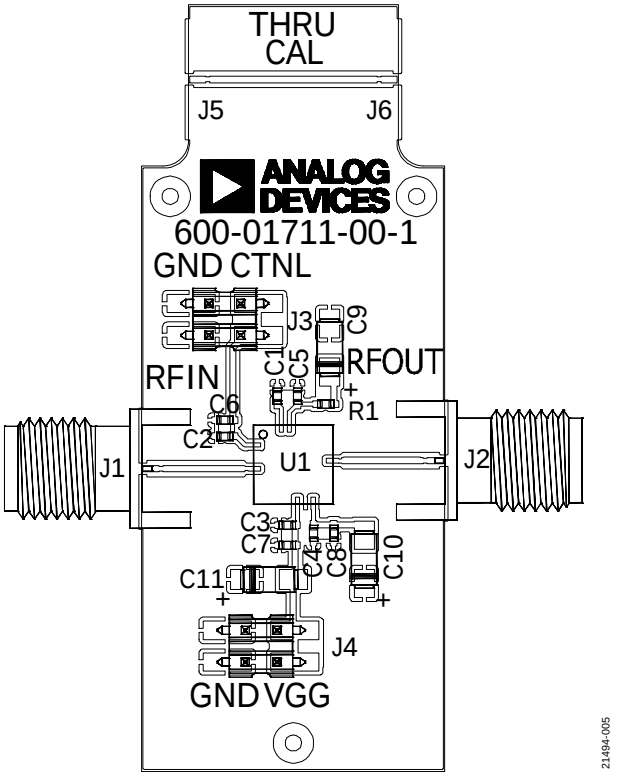

Figure 5. ADPA9002-EVALZ Assembly Drawing (J3, J5, and J6 Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Reference Designator	Description	Manufacturer	Part Number
C1, C3, C4	Ceramic capacitors, 100 pF	Johanson Dialectrics	500R07N101JV4T
C2, C6	Ceramic capacitors, not installed	Not applicable	Not applicable
C9, C10, C11	Tantalum capacitors, 4.7 µF	AVX	TAJA475K020RNJ
C5, C7, C8	Ceramic capacitors, multilayer, X8R, 10000 pF	Murata	GRM155R71H103KA88D
J1, J2	Connectors, 2.9 mm, jack edge	SRI Connector Gage Co.	25-146-1000-92
J3	Connector, PCB header, vertical, dual row, 4-position, 2 mm pitch, not installed	Molex	87759-0414
J4	Connector, PCB header, vertical, dual-row, 4-position, 2 mm pitch	Molex	87759-0414
J5, J6	Connectors, 2.9 mm, jack edge, not installed	SRI Connector Gage Co.	25-146-1000-92
R1	Resistor, 0402, surface-mount device (SMD) chip jumper, 0 Ω	Panasonic	ERJ-2GEJ104X
U1	Gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), dc to 10 GHz, power amplifier	Analog Devices, Inc.	ADPA9002ACGZN
Not Applicable	Aluminum heatsink, 0.75 in × 1.9 in	Not applicable	Not applicable