

# BLP7G10S-160P

Power LDMOS transistor

Rev. 1 — 30 August 2018

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 600 MHz to 960 MHz.

**Table 1. Typical performance**

*RF performance at  $T_h = 25^\circ\text{C}$  in a common source test circuit.*

Test signal	f (MHz)	V <sub>DS</sub> (V)	I <sub>DQ</sub> (mA)	P <sub>L(AV)</sub> (W)	P <sub>L(1dB)</sub> (W)	G <sub>p</sub> (dB)	$\eta_D$ (%)
pulsed, class-AB	860	28	100	-	160	20	62

### 1.2 Features and benefits

- Integrated ESD protection
- Excellent ruggedness
- High power gain
- High efficiency
- Excellent reliability
- Easy power control
- For RoHS compliance see the product details on the Ampleon website

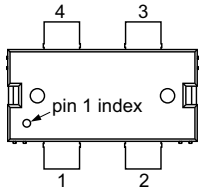
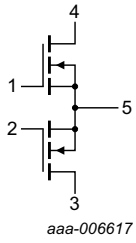
### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 600 MHz to 960 MHz frequency range

## 2. Pinning information

**Table 2. Pinning**

All pins must be connected for correct operation and to prevent damage to the device.

Pin	Description	Simplified outline	Graphic symbol
1	gate 1		
2	gate 2		
3	drain 2		
4	drain 1		
5	source <sup>[1]</sup>		

[1] Connected to flange.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BLP7G10S-160P	HSOP4F	plastic, heatsink small outline package; 4 leads (flat)	SOT1223-2

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-6	+11	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 160\text{ W}$ <sup>[1]</sup>	0.5	K/W

[1]  $R_{th(j-case)}$  is measured under RF conditions.

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ }^\circ\text{C}$  per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.9\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 90\text{ mA}$	1.5	1.86	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-1.4	-	+1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	15	16	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 3.15\text{ A}$	-	6	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 3.15\text{ A}$	-	0.2	-	$\Omega$

**Table 7. AC characteristics**

$T_j = 25\text{ }^\circ\text{C}$  per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	-	79	-	pF
$C_{oss}$	output capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	-	32	-	pF
$C_{rs}$	feedback capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	-	1.5	-	pF

**Table 8. RF characteristics**

Test signal: pulsed CW;  $f = 860\text{ MHz}$ ; RF performance measured at  $V_{DS} = 28\text{ V}; I_{Dq} = 100\text{ mA}$ ;  $T_{case} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified; in a class-AB production test circuit.

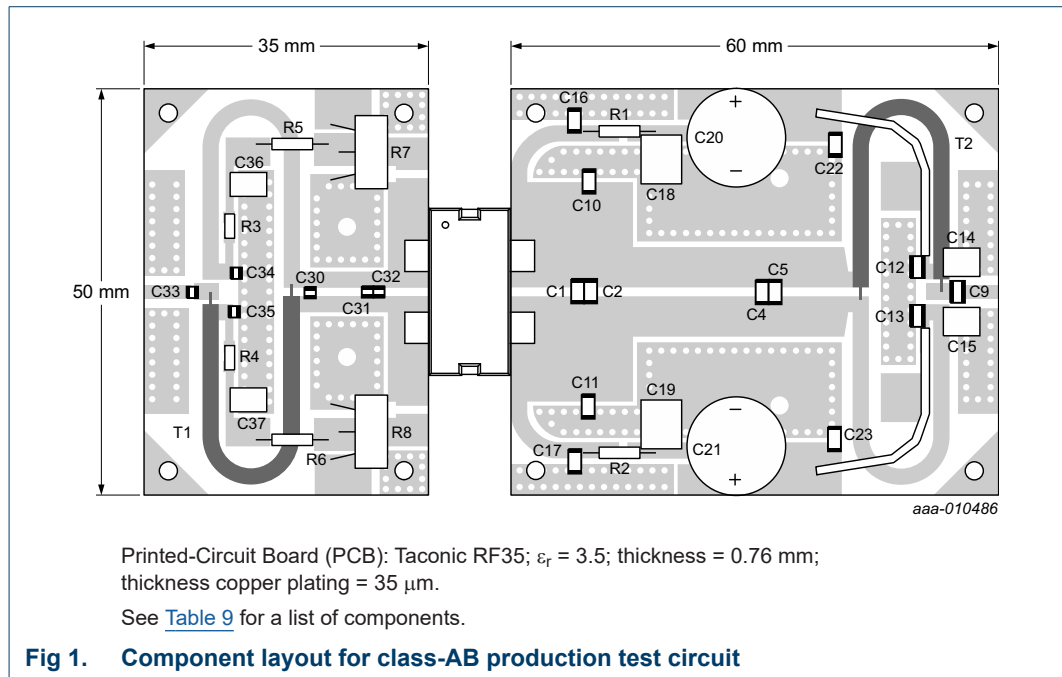
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(1dB)} = 160\text{ W}$	16.5	19.4	-	dB
$\eta_D$	drain efficiency	$P_{L(1dB)} = 160\text{ W}$	57.5	59.7	-	%

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLP7G10S-160P is capable of withstanding a load mismatch corresponding to  $VSWR = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  $f = 860\text{ MHz}$  at rated load power.

7.2 Demo circuit information



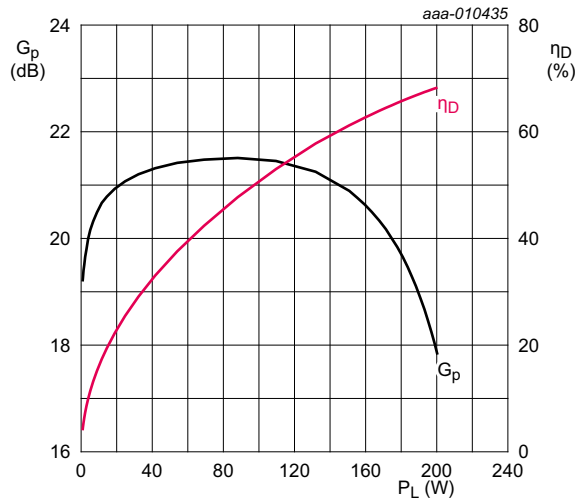
**Table 9. List of components**

For test circuit see [Figure 1](#).

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	5.6 pF	ATC800B
C4, C5	multilayer ceramic chip capacitor	4.7 pF	ATC800B
C9	multilayer ceramic chip capacitor	100 pF	ATC180R
C10, C11	multilayer ceramic chip capacitor	10 pF	ATC800B
C12, C13	multilayer ceramic chip capacitor	100 pF	ATC180R
C14, C15	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ , 50 V	TDK
C16, C17	multilayer ceramic chip capacitor	100 pF	ATC800B
C18, C19	multilayer ceramic chip capacitor	10 $\mu\text{F}$	TDK
C20, C21	electrolytic capacitor	470 $\mu\text{F}$ , 63 V	
C22, C23	multilayer ceramic chip capacitor	1 nF	ATC800B
C30	multilayer ceramic chip capacitor	33 pF	ATC800A
C31	multilayer ceramic chip capacitor	10 pF	ATC800A
C32	multilayer ceramic chip capacitor	11 pF	ATC800A
C33, C34, C35	multilayer ceramic chip capacitor	91 pF	ATC800A
C36, C37	electrolytic capacitor	4.7 $\mu\text{F}$ , 50 V	
T1	semi rigid coax	25 $\Omega$	Micro-Coax: UT-090C-25
T2	semi rigid coax	25 $\Omega$	Micro-Coax: UT-090C-25
R1, R2	resistor	10 $\Omega$	Vishay: MRS25
R3, R4	resistor	5.6 $\Omega$	SMD 1206
R5, R6	resistor	100 $\Omega$	Vishay: MRS25
R7, R8	potentiometer	10 k $\Omega$	Bourns

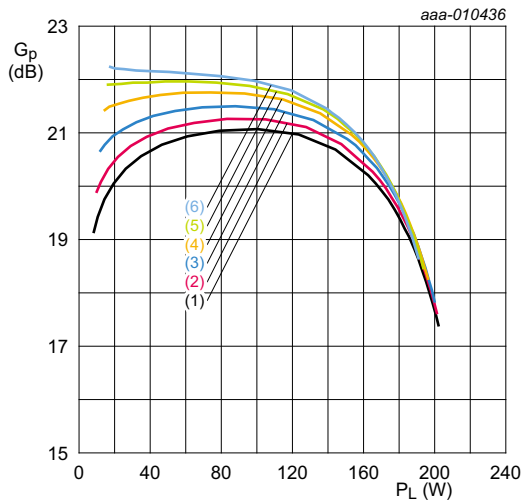
7.3 Graphical data

7.3.1 1-Tone pulsed



$V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 200\text{ mA}$ ;  $f = 860\text{ MHz}$ .

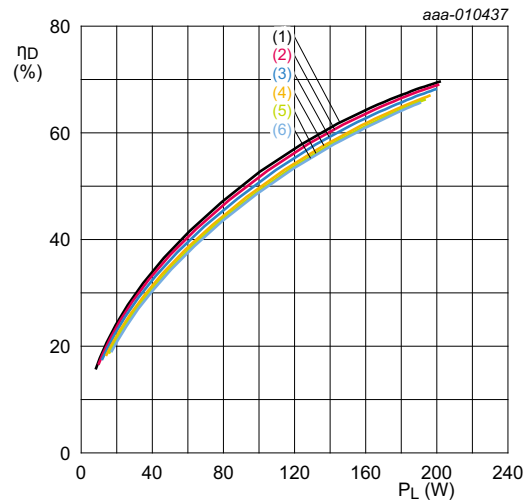
Fig 2. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 28\text{ V}$ ;  $f = 860\text{ MHz}$ .

- (1)  $I_{Dq} = 50\text{ mA}$
- (2)  $I_{Dq} = 100\text{ mA}$
- (3)  $I_{Dq} = 200\text{ mA}$
- (4)  $I_{Dq} = 400\text{ mA}$
- (5)  $I_{Dq} = 600\text{ mA}$
- (6)  $I_{Dq} = 800\text{ mA}$

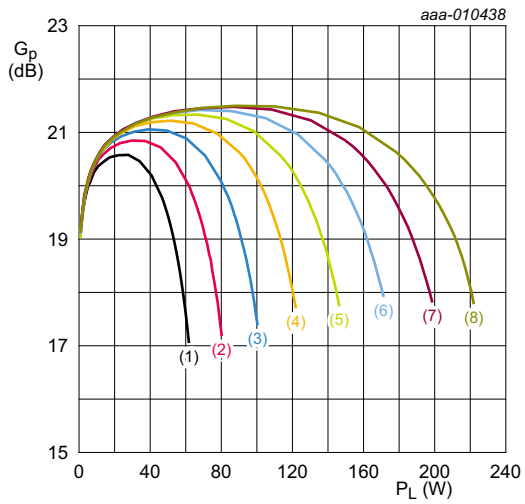
Fig 3. Power gain as a function of output power; typical values



$V_{DS} = 28\text{ V}$ ;  $f = 860\text{ MHz}$ .

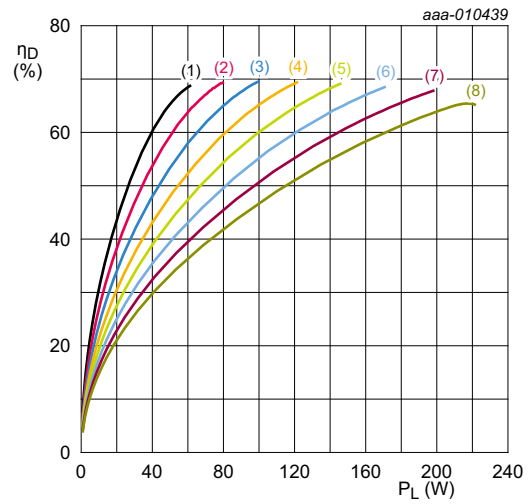
- (1)  $I_{Dq} = 50\text{ mA}$
- (2)  $I_{Dq} = 100\text{ mA}$
- (3)  $I_{Dq} = 200\text{ mA}$
- (4)  $I_{Dq} = 400\text{ mA}$
- (5)  $I_{Dq} = 600\text{ mA}$
- (6)  $I_{Dq} = 800\text{ mA}$

Fig 4. Drain efficiency as a function of output power; typical values



- $I_{Dq} = 200 \text{ mA}; f = 860 \text{ MHz}.$
- (1)  $V_{DS} = 16 \text{ V}$
  - (2)  $V_{DS} = 18 \text{ V}$
  - (3)  $V_{DS} = 20 \text{ V}$
  - (4)  $V_{DS} = 22 \text{ V}$
  - (5)  $V_{DS} = 24 \text{ V}$
  - (6)  $V_{DS} = 26 \text{ V}$
  - (7)  $V_{DS} = 28 \text{ V}$
  - (8)  $V_{DS} = 30 \text{ V}$

**Fig 5. Power gain as a function of output power; typical values**



- $I_{Dq} = 200 \text{ mA}; f = 860 \text{ MHz}.$
- (1)  $V_{DS} = 16 \text{ V}$
  - (2)  $V_{DS} = 18 \text{ V}$
  - (3)  $V_{DS} = 20 \text{ V}$
  - (4)  $V_{DS} = 22 \text{ V}$
  - (5)  $V_{DS} = 24 \text{ V}$
  - (6)  $V_{DS} = 26 \text{ V}$
  - (7)  $V_{DS} = 28 \text{ V}$
  - (8)  $V_{DS} = 30 \text{ V}$

**Fig 6. Drain efficiency as a function of output power; typical values**

### 8. Package outline

HSOP4F: plastic, heatsink small outline package; 4 leads(flat)

SOT1223-2

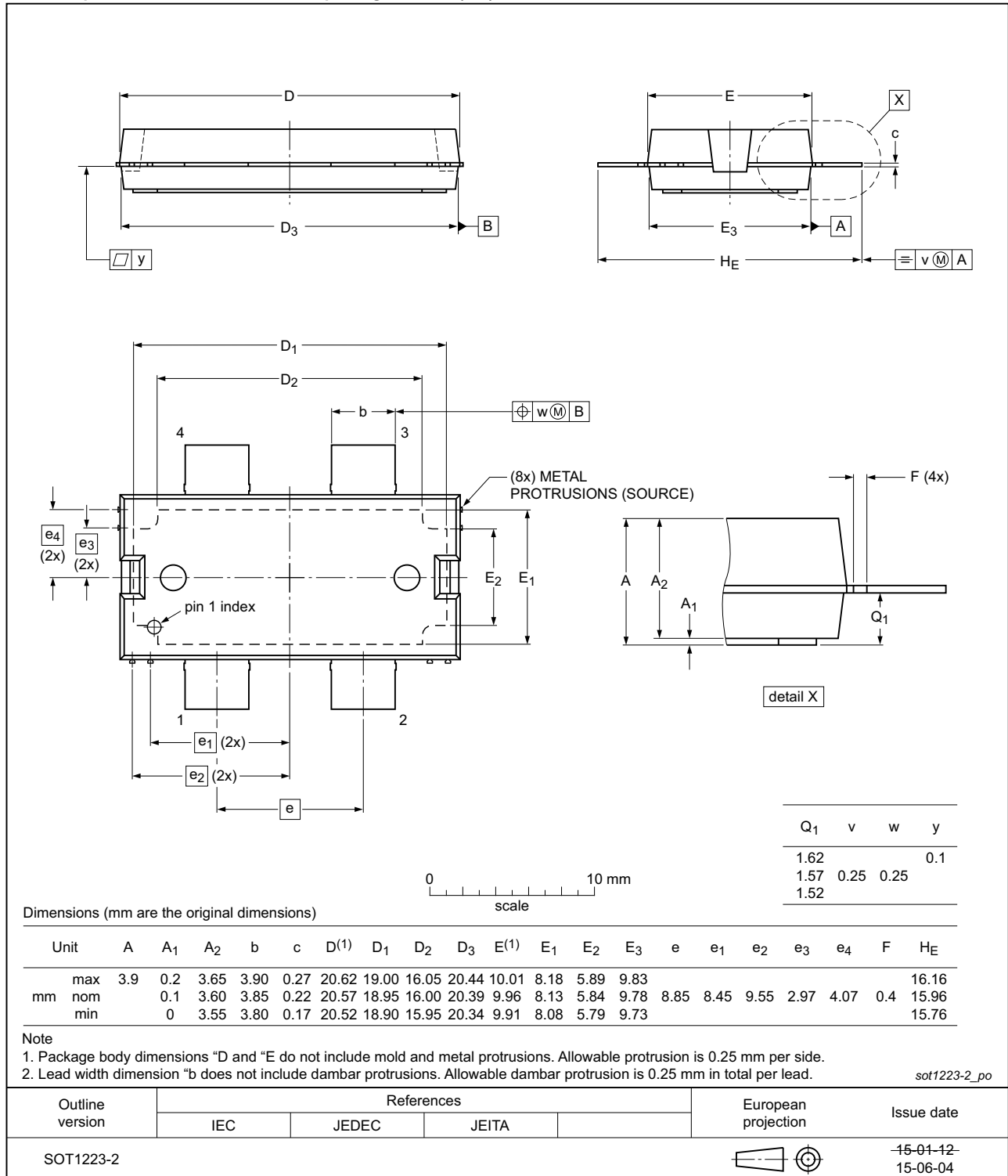


Fig 7. Package outline SOT1223-2 (HSOP4F)

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 10. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

## 10. Abbreviations

**Table 11. Abbreviations**

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

## 11. Revision history

**Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP7G10S-160P v.1	20180830	Product data sheet	-	-



## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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