BLP15M7160P

Power LDMOS transistor

Rev. 5 — 8 January 2016

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 160W LDMOS RF power transistor for broadcast transmitter and industrial applications. The transistor is suitable for the frequency range HF to 1500 MHz. The excellent ruggedness and broadband performance of this device makes it ideal for digital applications.

Table 1. Typical performance

RF performance at T_h = 25 °C in a common source test circuit.

Test signal	f (MHz)	V_{DS} (V)	I_{Dq} (mA)	$P_{L(AV)}$ (W)	$P_{L(M)}$ (W)	G_p (dB)	η_D (%)
pulsed, class-B	860	28	100	-	160	20	62

1.2 Features and benefits

- Integrated ESD protection
- Excellent ruggedness
- High power gain
- High efficiency
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

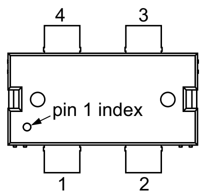
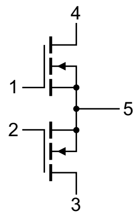
1.3 Applications

- Communication transmitter applications in the HF to 1500 MHz frequency range
- Industrial applications in the HF to 1500 MHz frequency range
- Single product Doherty applications

2. Pinning information

Table 2. Pinning

All pins must be connected for correct operation and to prevent damage to the device.

Pin	Description	Simplified outline	Graphic symbol
1	gate 1		 aaa-006617
2	gate 2		
3	drain 2		
4	drain 1		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLP15M7160P	HSOP4F	plastic, heatsink small outline package; 4 leads (flat)	SOT1223-2

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 160 W [1]	0.5	K/W

[1] $R_{th(j-case)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.9 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 90 mA	1.5	1.86	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	−1.4	-	+1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	15	16	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.15 A	-	6	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 3.15 A	-	0.2	-	Ω

Table 7. AC characteristics

T_j = 25 °C per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	79	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	32	-	pF
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	1.5	-	pF

Table 8. RF characteristics

Test signal: pulsed CW; f = 860 MHz; RF performance measured at V_{DS} = 28 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified; in a class-B production test circuit.

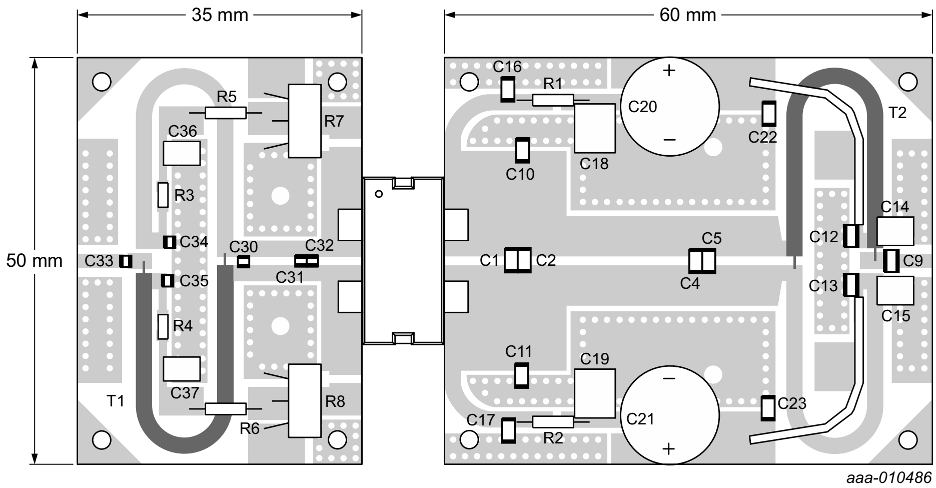
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(M)}$ = 160 W	16.5	19.4	-	dB
η_D	drain efficiency	$P_{L(M)}$ = 160 W	57.5	59.7	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLP15M7160P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; f = 860 MHz at rated load power.

7.2 Demo circuit information



Printed-Circuit Board (PCB): Taconic RF35; ε_r = 3.5; thickness = 0.76 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

Fig 1. Component layout for class-AB production test circuit

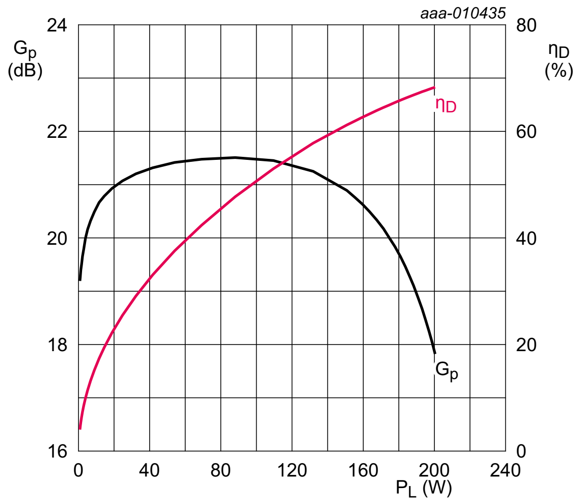
Table 9. List of components

For test circuit see Figure 1.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	5.6 pF	ATC800B
C4, C5	multilayer ceramic chip capacitor	4.7 pF	ATC800B
C9	multilayer ceramic chip capacitor	100 pF	ATC180R
C10, C11	multilayer ceramic chip capacitor	10 pF	ATC800B
C12, C13	multilayer ceramic chip capacitor	100 pF	ATC180R
C14, C15	multilayer ceramic chip capacitor	4.7 μF, 50 V	TDK
C16, C17	multilayer ceramic chip capacitor	100 pF	ATC800B
C18, C19	multilayer ceramic chip capacitor	10 μF	TDK
C20, C21	electrolytic capacitor	470 μF, 63 V	
C22, C23	multilayer ceramic chip capacitor	1 nF	ATC800B
C30	multilayer ceramic chip capacitor	33 pF	ATC800A
C31	multilayer ceramic chip capacitor	10 pF	ATC800A
C32	multilayer ceramic chip capacitor	11 pF	ATC800A
C33, C34, C35	multilayer ceramic chip capacitor	91 pF	ATC800A
C36, C37	electrolytic capacitor	4.7 μF, 50 V	
T1	semi rigid coax	25 Ω	Micro-Coax UT-090C-25
T2	semi rigid coax	25 Ω	Micro-Coax UT-090C-25
R1, R2	resistor	10 Ω	Vishay MRS25
R3, R4	resistor	5.6 Ω	SMD 1206
R5, R6	resistor	100 Ω	Vishay MRS25
R7, R8	potentiometer	10 kΩ	Bourns

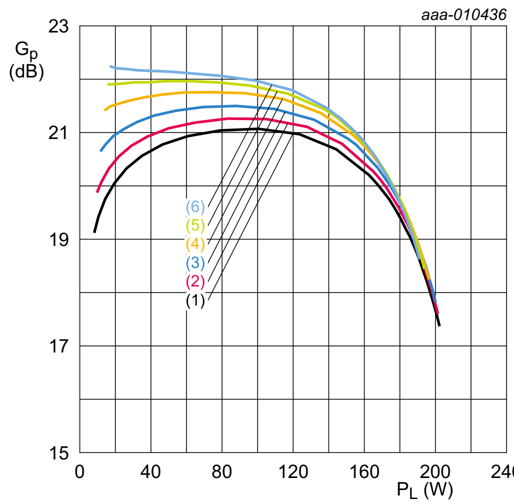
7.3 Graphical data

7.3.1 1-Tone pulsed



V_{DS} = 28 V; I_{Dq} = 200 mA; f = 860 MHz.

Fig 2. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; f = 860 MHz.

(1) I_{Dq} = 50 mA

(2) I_{Dq} = 100 mA

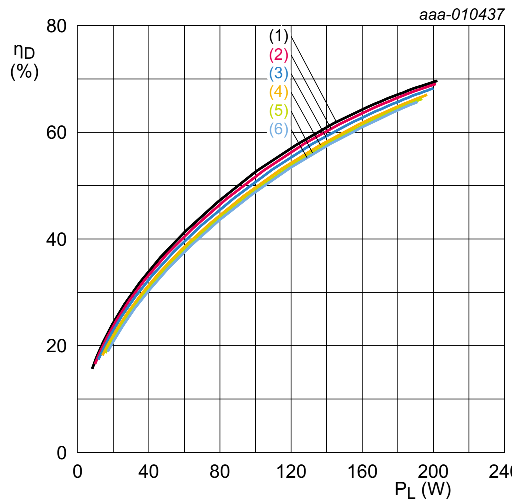
(3) I_{Dq} = 200 mA

(4) I_{Dq} = 400 mA

(5) I_{Dq} = 600 mA

(6) I_{Dq} = 800 mA

Fig 3. Power gain as a function of output power; typical values



V_{DS} = 28 V; f = 860 MHz.

(1) I_{Dq} = 50 mA

(2) I_{Dq} = 100 mA

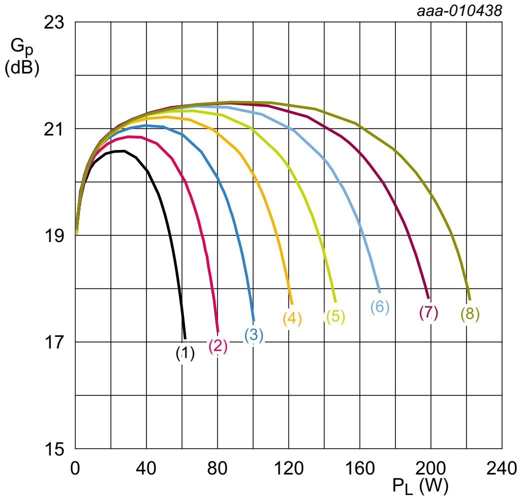
(3) I_{Dq} = 200 mA

(4) I_{Dq} = 400 mA

(5) I_{Dq} = 600 mA

(6) I_{Dq} = 800 mA

Fig 4. Drain efficiency as a function of output power; typical values



I_{Dq} = 200 mA; f = 860 MHz.

(1) V_{DS} = 16 V

(2) V_{DS} = 18 V

(3) V_{DS} = 20 V

(4) V_{DS} = 22 V

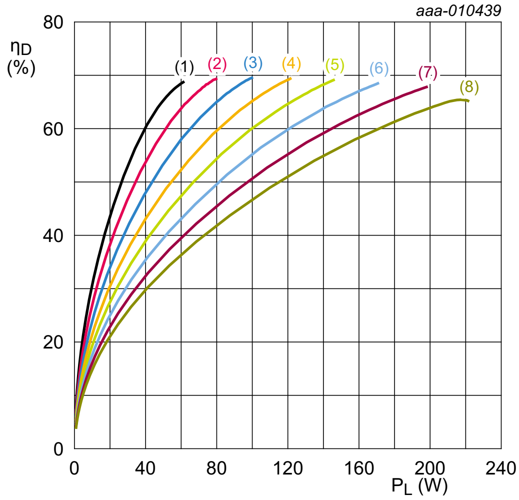
(5) V_{DS} = 24 V

(6) V_{DS} = 26 V

(7) V_{DS} = 28 V

(8) V_{DS} = 30 V

Fig 5. Power gain as a function of output power; typical values



I_{Dq} = 200 mA; f = 860 MHz.

(1) V_{DS} = 16 V

(2) V_{DS} = 18 V

(3) V_{DS} = 20 V

(4) V_{DS} = 22 V

(5) V_{DS} = 24 V

(6) V_{DS} = 26 V

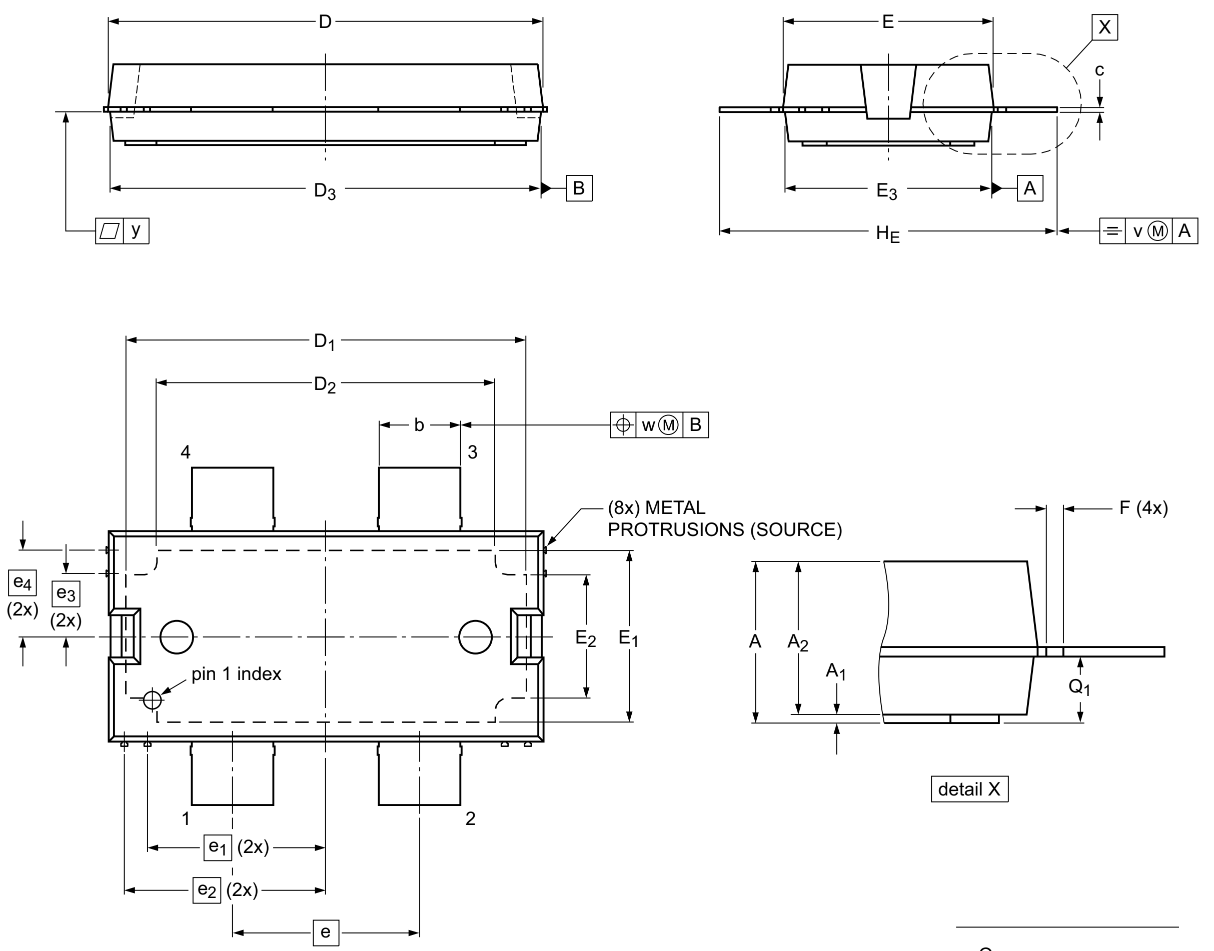
(7) V_{DS} = 28 V

(8) V_{DS} = 30 V

Fig 6. Drain efficiency as a function of output power; typical values

8. Package outline

HSOP4F: plastic, heatsink small outline package; 4 leads(flat) **SOT1223-2**



Q1	v	w	y
1.62			0.1
1.57	0.25	0.25	
1.52			

0 10 mm
scale

Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	c	D(1)	D_1	D_2	D_3	E(1)	E_1	E_2	E_3	e	e_1	e_2	e_3	e_4	F	H_E
	max	3.9	0.2	3.65	3.90	0.27	20.62	19.00	16.05	20.44	10.01	8.18	5.89	9.83							16.16
mm	nom		0.1	3.60	3.85	0.22	20.57	18.95	16.00	20.39	9.96	8.13	5.84	9.78	8.85	8.45	9.55	2.97	4.07	0.4	15.96
	min		0	3.55	3.80	0.17	20.52	18.90	15.95	20.34	9.91	8.08	5.79	9.73							15.76

Note
1. Package body dimensions “D and “E do not include mold and metal protrusions. Allowable protrusion is 0.25 mm per side.
2. Lead width dimension “b does not include dambar protrusions. Allowable dambar protrusion is 0.25 mm in total per lead.

sot1223-2_po

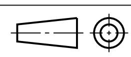
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1223-2						~~15-01-12~~ 15-06-04

Fig 7. Package outline SOT1223-2 (HSOP4F)

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP15M7160P v.5	20160108	Product data sheet	-	BLP15M7160P v.4
Modifications	• Table 3 on page 2: table updated • Figure 7 on page 7: package outline changed from SOT1223-1 to SOT1223-2			
BLP15M7160P v.4	20150901	Product data sheet	-	BLP15M7160P v.3
BLP15M7160P v.3	20150209	Product data sheet	-	BLP15M7160P v.2
BLP15M7160P v.2	20140610	Product data sheet	-	BLP15M7160P v.1
BLP15M7160P v.1	20140110	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

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Date of release: 8 January 2016
Document identifier: BLP15M7160P