ALPHA & OMEGA SEMICONDUCTOR

AON6934A

30V Dual Asymmetric N-Channel AlphaMOS

General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Very Low RDS(on) at 4.5V_{GS}
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

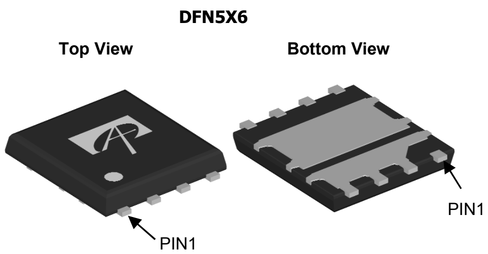
Product Summary

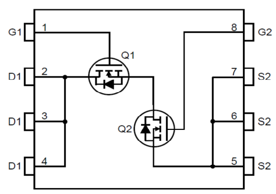
	Q1	Q2
V_{DS}	30V	30V
I_D (at V_{GS}=10V)	28A	36A
$R_{DS(ON)}$ (at V_{GS}=10V)	<5.2mΩ	<2.9mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	<9.5mΩ	<4.4mΩ

100% UIS Tested
100% Rg Tested

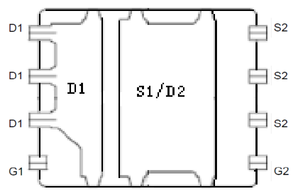
Applications

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial





Top View



Bottom View

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Max Q1	Max Q2	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current[G]	T_C=25°C	I_D	28	36	A
	T_C=100°C		22	28	
Pulsed Drain Current [C]		I_{DM}	112	144	
Continuous Drain Current	T_A=25°C	I_{DSM}	22	30	A
	T_A=70°C		17	24	
Avalanche Current [C]		I_{AS}	32*	46*	A
Avalanche Energy L=0.05mH [C]		E_{AS}	26*	53*	mJ
V_{DS} Spike	100ns	V_{SPIKE}	36	36	V
Power Dissipation [B]	T_C=25°C	P_D	31	33	W
	T_C=100°C		12	13	
Power Dissipation [A]	T_A=25°C	P_{DSM}	3.6	4.3	W
	T_A=70°C		2.3	2.7	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics

Parameter		Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	29	24	35	29	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		56	50	67	60	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	3.3	3	4	3.8	°C/W

*Q1 L=0.1mH, I_{AS}=20A, E_{AS}=20mJ, Starting T_J=25°C.

*Q2 L=0.1mH, I_{AS}=33A, E_{AS}=54mJ, Starting T_J=25°C.

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V				100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA		1.4	1.8	2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A			4.3	5.2	mΩ
			T_J=125°C		6	7.2	
		V_{GS}=4.5V, I_D=20A			7	9.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A			91		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V			0.7	1	V
I_S	Maximum Body-Diode Continuous Current[G]					28	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz			1037		pF
C_{oss}	Output Capacitance				441		pF
C_{rss}	Reverse Transfer Capacitance				61		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		0.7	1.5	2.3	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A			15.5	22	nC
Q_g(4.5V)	Total Gate Charge				6.8	10	nC
Q_{gs}	Gate Source Charge				3.0		nC
Q_{gd}	Gate Drain Charge				3.6		nC
Q_{gs}	Gate Source Charge	V_{GS}=4.5V, V_{DS}=15V, I_D=20A			3.0		nC
Q_{gd}	Gate Drain Charge				3.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω			5.5		ns
t_r	Turn-On Rise Time				3.3		ns
$t_{D(off)}$	Turn-Off DelayTime				18		ns
t_f	Turn-Off Fall Time				4.3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs			12.7		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs			17.2		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is limited by package.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with TA=25° C.

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

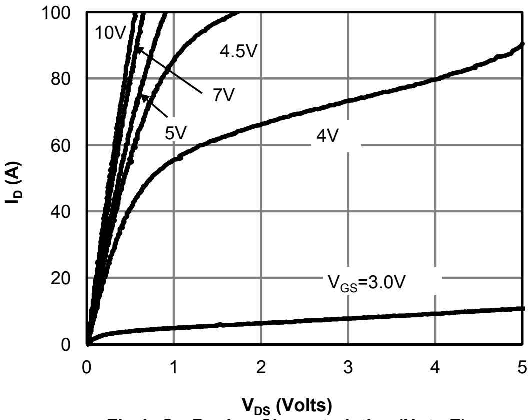


Fig 1: On-Region Characteristics (Note E)

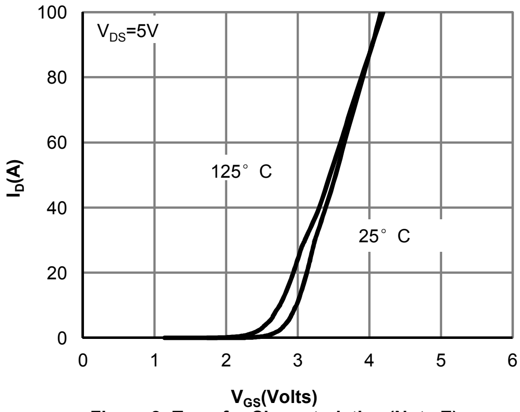


Figure 2: Transfer Characteristics (Note E)

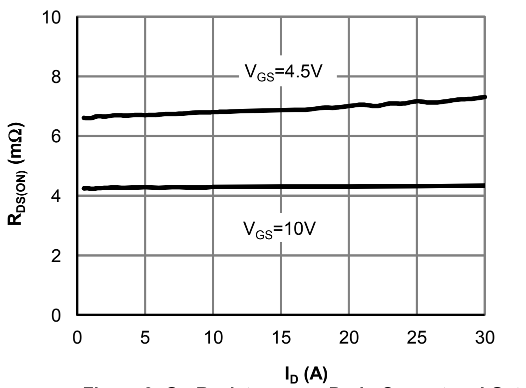


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

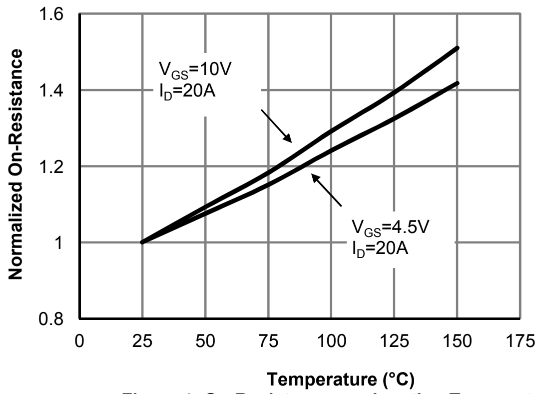


Figure 4: On-Resistance vs. Junction Temperature (Note E)

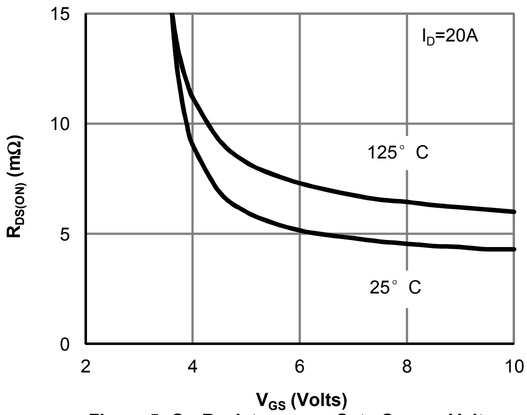


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

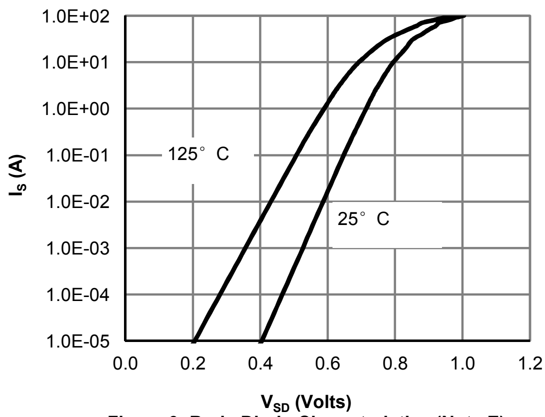


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

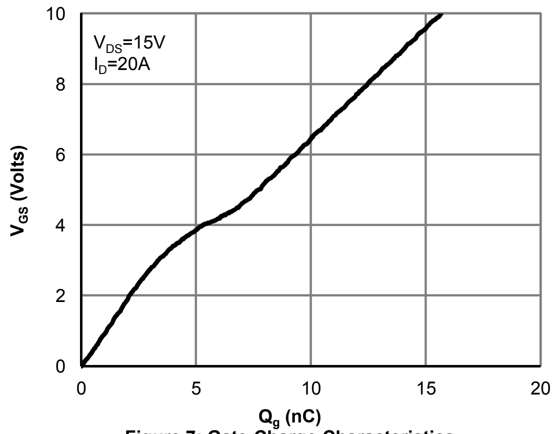


Figure 7: Gate-Charge Characteristics

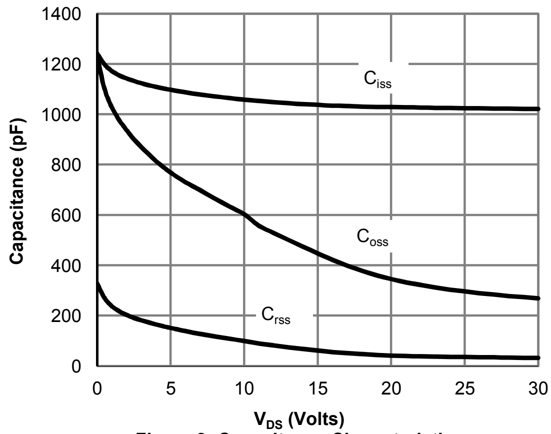


Figure 8: Capacitance Characteristics

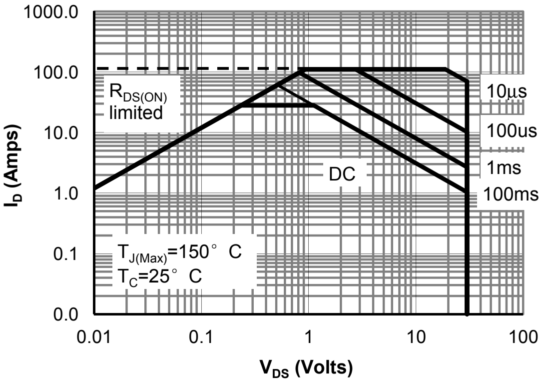


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

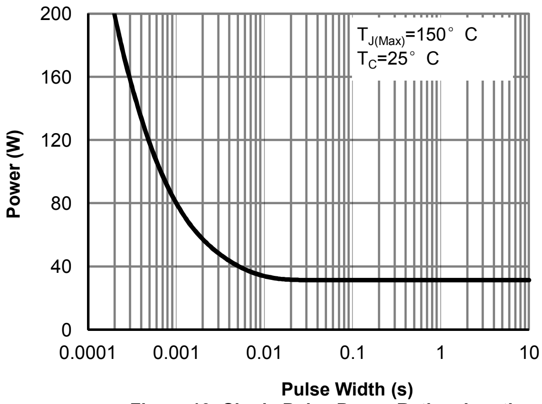


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

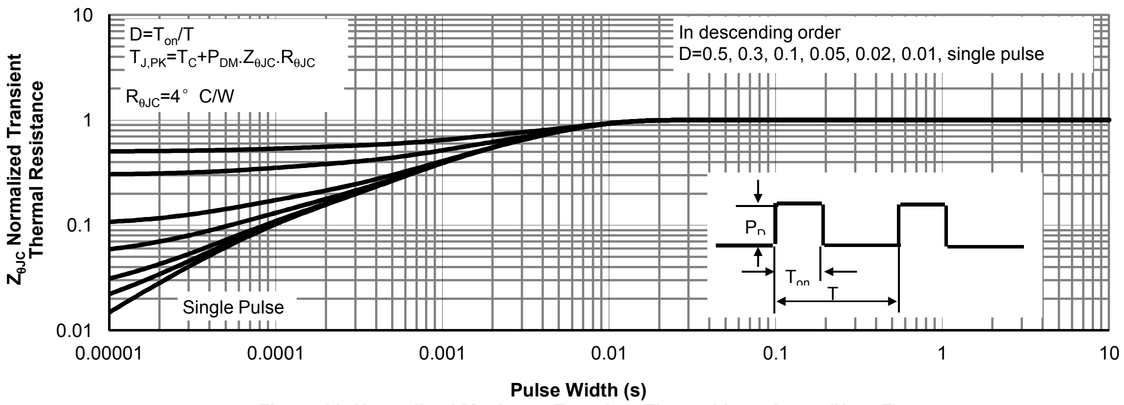


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

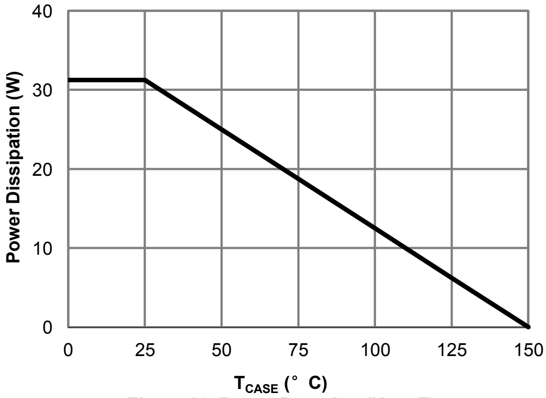


Figure 12: Power De-rating (Note F)

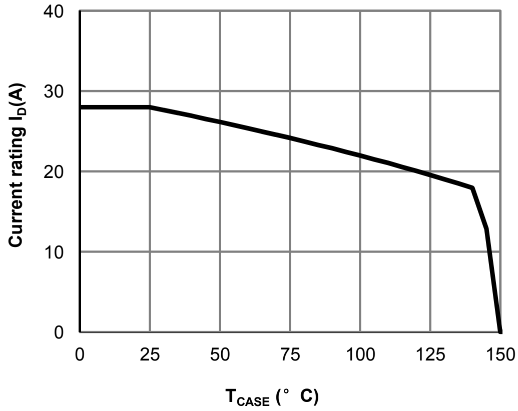


Figure 13: Current De-rating (Note F)

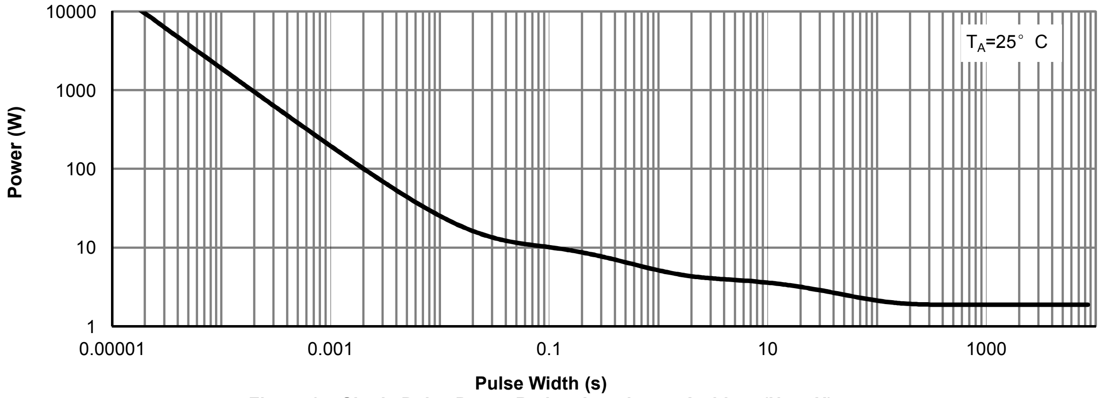


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

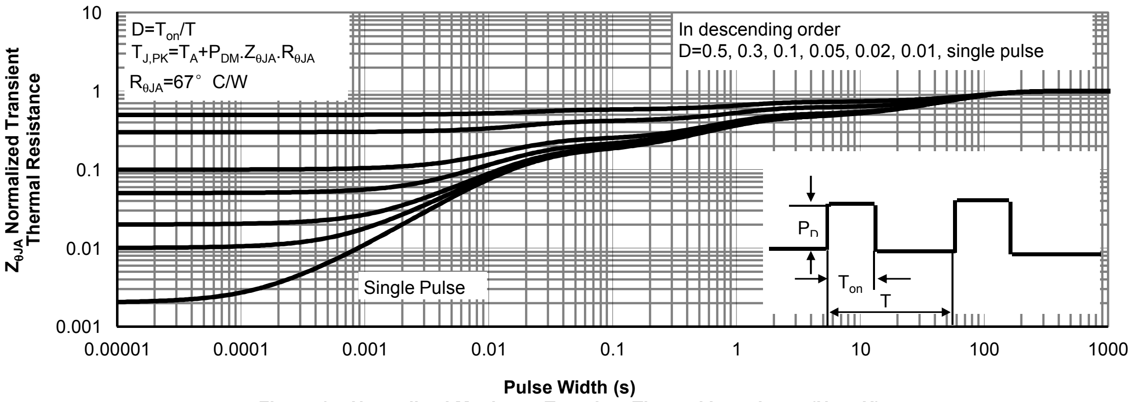


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

ALPHA & OMEGA SEMICONDUCTOR

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.4	1.8	2.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		2.4	2.9	mΩ
		T_J=125°C		3.6	4.4	
		V_{GS}=4.5V, I_D=20A		3.5	4.4	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		105		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current[G]				36	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		2010		pF
C_{oss}	Output Capacitance			898		pF
C_{rss}	Reverse Transfer Capacitance			124		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.9	1.8	2.7	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A		36	49	nC
Q_g(4.5V)	Total Gate Charge			17	23	nC
Q_{gs}	Gate Source Charge			6		nC
Q_{gd}	Gate Drain Charge			8		nC
Q_{gs}	Gate Source Charge	V_{GS}=4.5V, V_{DS}=15V, I_D=20A		6		nC
Q_{gd}	Gate Drain Charge			8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		7.5		ns
t_r	Turn-On Rise Time			4.0		ns
$t_{D(off)}$	Turn-Off DelayTime			37.0		ns
t_f	Turn-Off Fall Time			7.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs		14		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs		20.3		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is limited by package.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with TA=25° C.

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

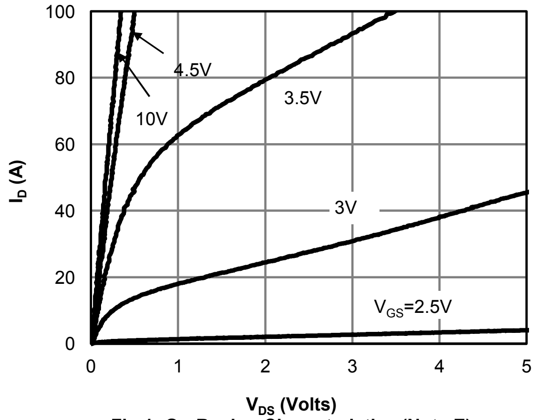


Fig 1: On-Region Characteristics (Note E)

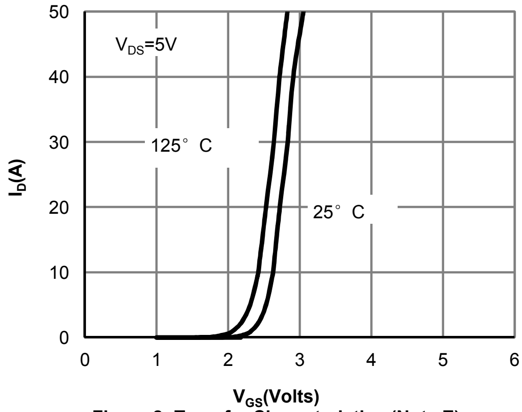


Figure 2: Transfer Characteristics (Note E)

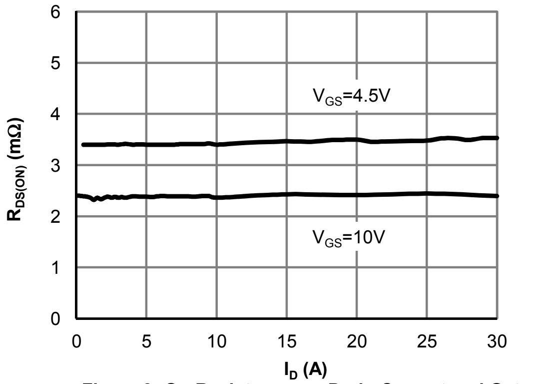


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

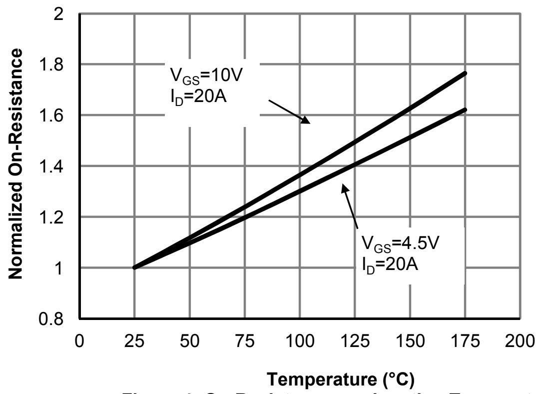


Figure 4: On-Resistance vs. Junction Temperature (Note E)

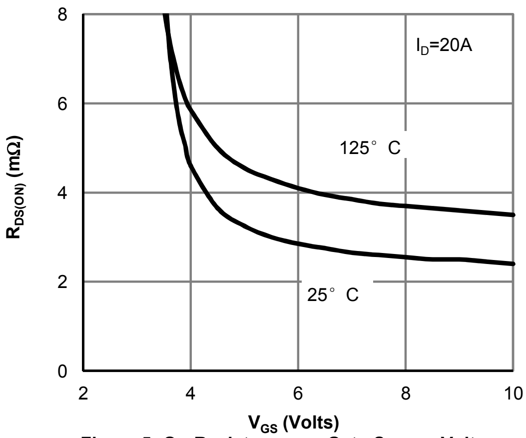


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

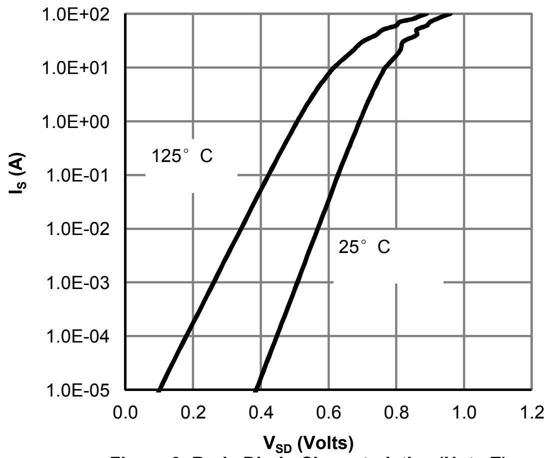


Figure 6: Body-Diode Characteristics (Note E)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

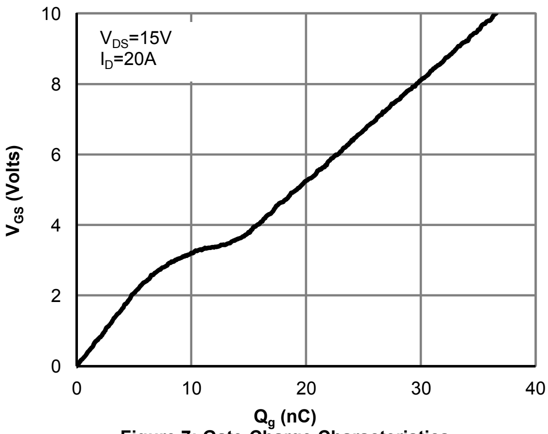


Figure 7: Gate-Charge Characteristics

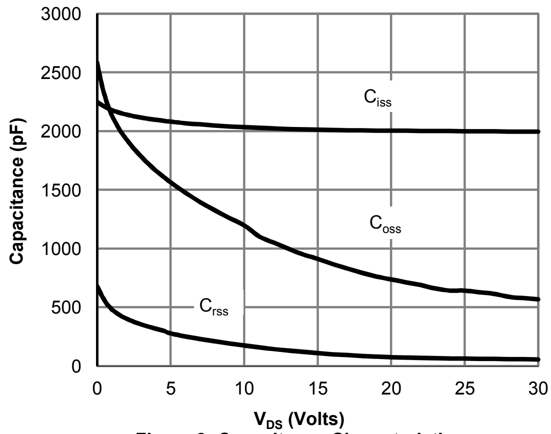


Figure 8: Capacitance Characteristics

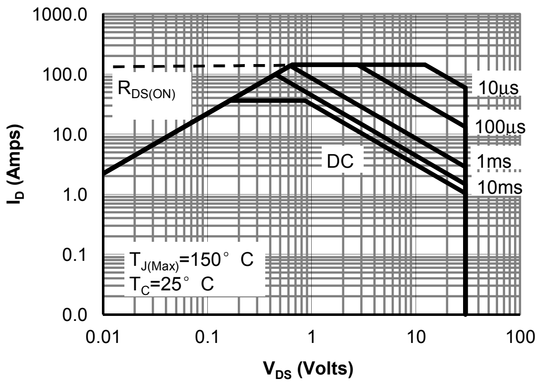


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

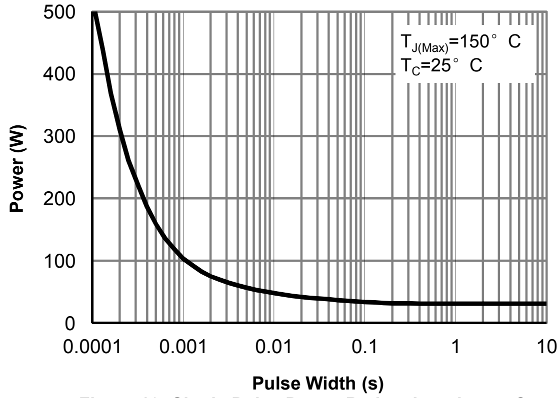


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

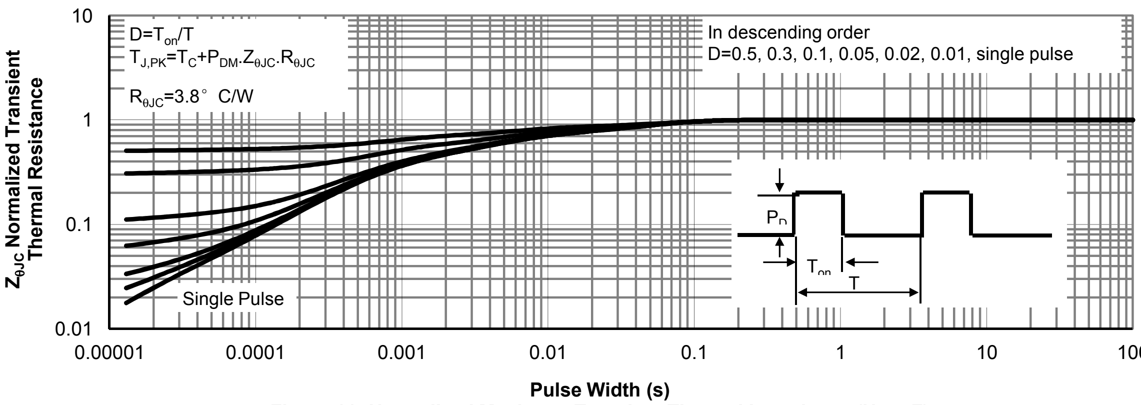


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

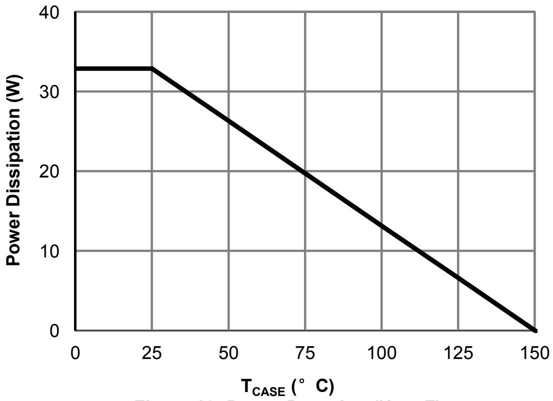


Figure 12: Power De-rating (Note F)

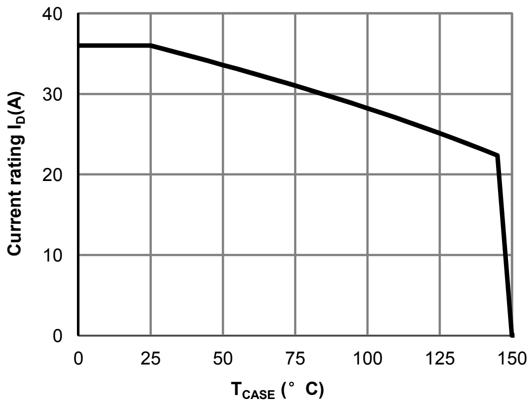


Figure 13: Current De-rating (Note F)

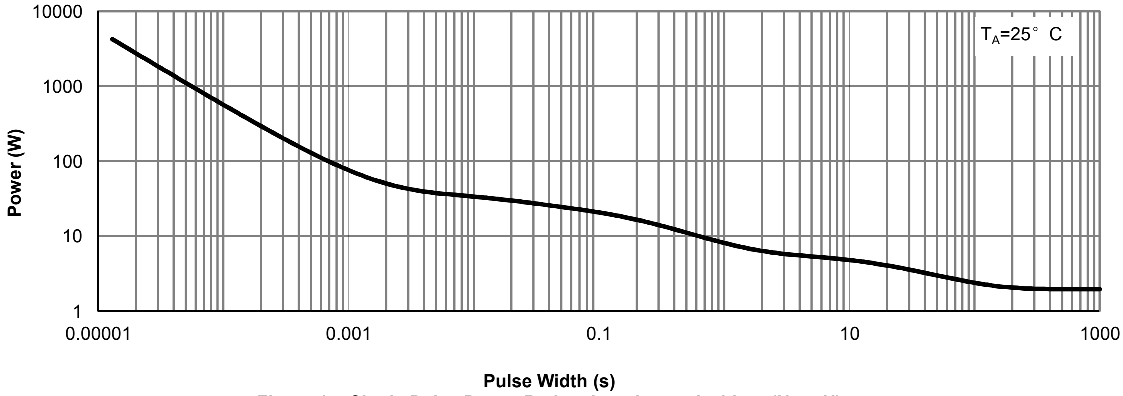


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

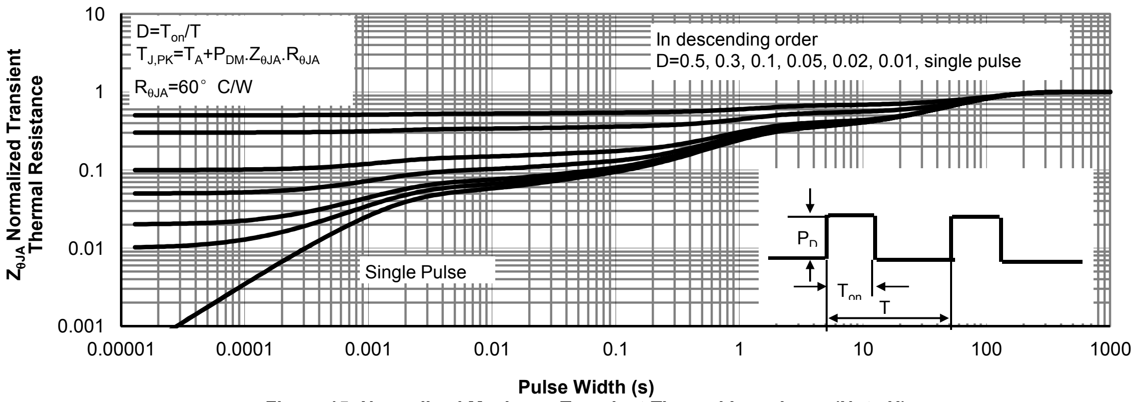
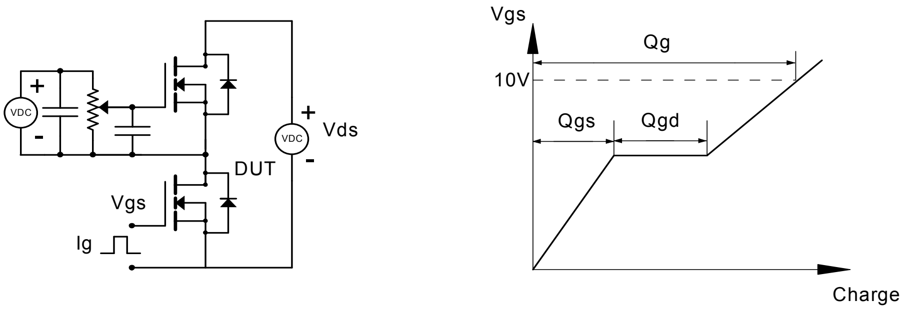
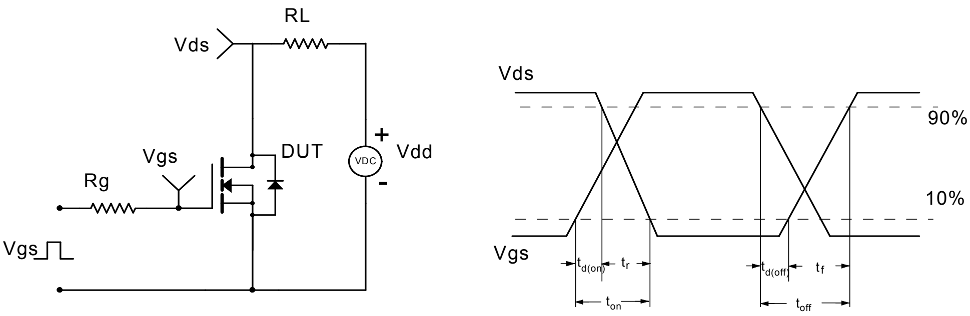


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

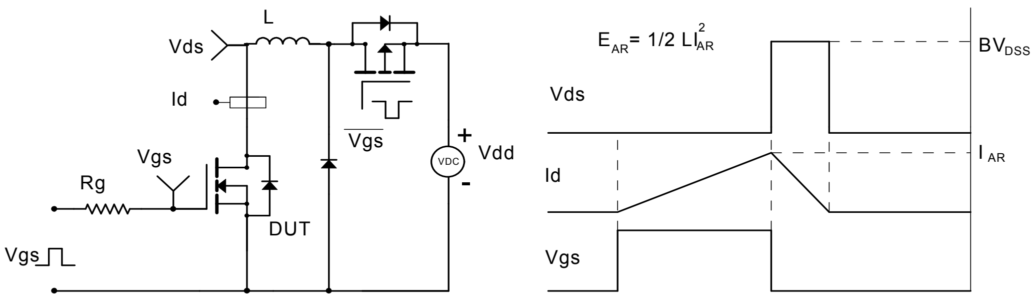
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms