Enabling an Intelligent Planet

Advantech

AQD-SD3L8GE16-MG
Datasheet

Rev. 0.0

2013-11-28

Description

AQD-SD3L8GE16-MG is a DDR3L SO DIMM, ECC, high-speed, low power memory module that use 18 pcs of 512Mx8bits DDR3 low voltage SDRAM in FBGA package and a 2K bits serial EEPROM on a 204-pin printed circuit board. AQD-SD3L8GE16-MG is a Dual In-Line Memory Module and is intended for mounting into 204-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

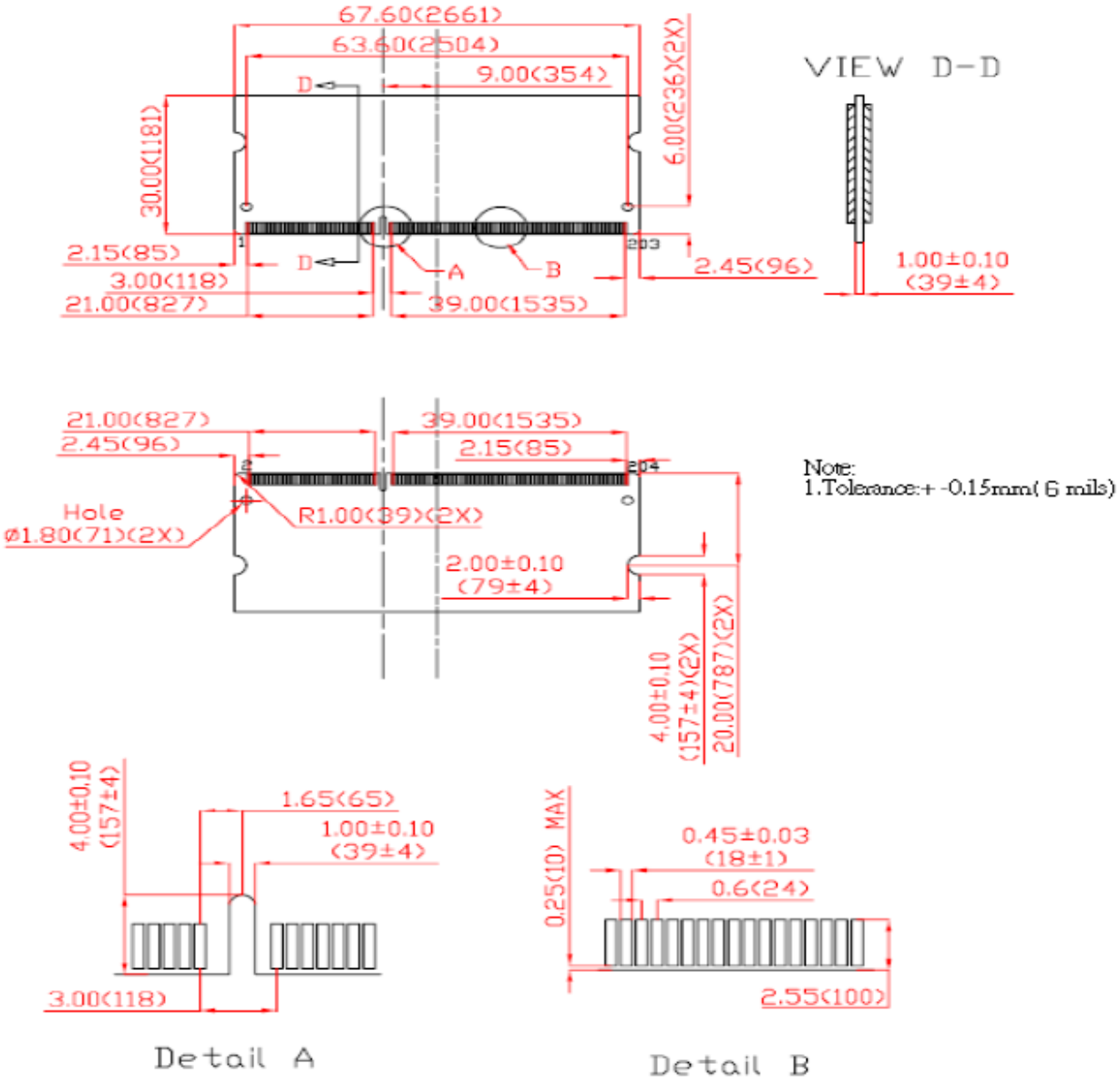
Features

- RoHS compliant products.
- JEDEC standard 1.35V(1.28V~1.45V) Power supply
- JEDEC standard 1.5V(1.425V~1.575V) Power supply
- VDDQ=1.35V(1.28V~1.45V) & 1.5V(1.425V~1.575V)
- Clock Freq: 800MHZ for 1600MT/s
- Programmable CAS Latency: 6, 7, 8, 9, 10, 11
- Programmable Additive Latency (Posted /CAS): 0,CL-2 or CL-1 clock
- Programmable /CAS Write Latency (CWL) = 8(DDR3-1600)
- 8 bit pre-fetch
- Burst Length: 4, 8
- Bi-directional Differential Data-Strobe
- Internal calibration through ZQ pin
- On Die Termination with ODT pin
- Serial presence detect with EEPROM
- Asynchronous reset

Pin Identification

Symbol	Function
A0~A15, BA0~BA2	Address/Bank input
DQ0~DQ63	Bi-direction data bus.
DQS0~DQS7	Data strobes
/DQS0~/DQS7	Differential Data strobes
CK0, /CK0,CK1, /CK1	Clock Input. (Differential pair)
CKE0, CKE1	Clock Enable Input.
ODT0, ODT1	On-die termination control line
/S0, /S1	DIMM rank select lines.
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write Enable
DM0~DM7	Data masks/high data strobes
VDD	Core power supply
VDDQ	I/O driver power supply
$V_{REF}DQ$	DQ reference supply
$V_{REF}CA$	Command/address reference supply
$V_{DD}SPD$	SPD EEPROM power supply
SA0~SA1	I2C serial bus address select for EEPROM
SCL	I2C serial bus clock for EEPROM
SDA	I2C serial bus data for EEPROM
VSS	Ground
/RESET	Set DRAMs Known State
VTT	DRAM I/O termination supply
NC	No Connection

Dimensions (Unit: millimeter)



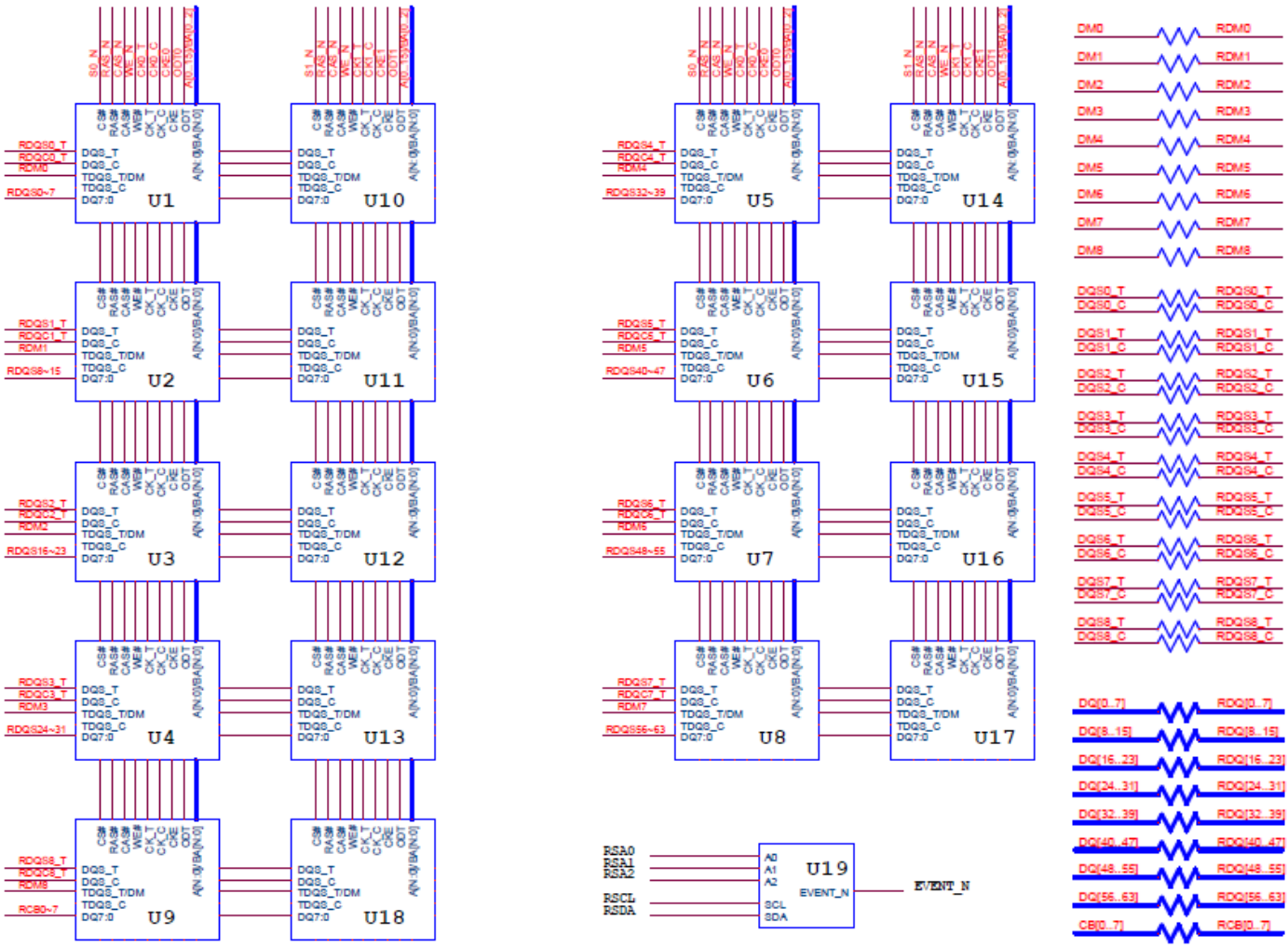
Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

Pin Assignments

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	VREFDQ	41	VSS	81	CB2	121	/WE	161	DQ43	201	SA1
02	VSS	42	DQ21	82	CB7	122	/RAS	162	DQ47	202	SCL
03	VSS	43	/DQS2	83	CB3	123	VDD	163	VSS	203	VTT
04	DQ4	44	DM2	84	VREFCA	124	VDD	164	VSS	204	VTT
05	DQ0	45	DQS2	85	VDD	125	/CAS	165	DQ48		
06	DQ5	46	VSS	86	VDD	126	ODT0	166	DQ52		
07	DQ1	47	VSS	87	CKE0	127	/CS0	167	DQ49		
08	VSS	48	DQ22	88	A15	128	ODT1	168	DQ53		
09	VSS	49	DQ18	89	CKE1	129	/CS1	169	VSS		
10	/DQS0	50	DQ23	90	A14	130	A13	170	VSS		
11	DM0	51	DQ19	91	BA2	131	VDD	171	/DQS6		
12	DQS0	52	VSS	92	A9	132	VDD	172	DM6		
13	DQ2	53	VSS	93	VDD	133	DQ32	173	DQS6		
14	VSS	54	DQ28	94	VDD	134	DQ36	174	DQ54		
15	DQ3	55	DQ24	95	A12/BC#	135	DQ33	175	VSS		
16	DQ6	56	DQ29	96	A11	136	DQ37	176	DQ55		
17	VSS	57	DQ25	97	A8	137	VSS	177	DQ50		
18	DQ7	58	VSS	98	A7	138	VSS	178	VSS		
19	DQ8	59	DM3	99	A5	139	/DQS4	179	DQ51		
20	VSS	60	/DQS3	100	A6	140	DM4	180	DQ60		
21	DQ9	61	VSS	101	VDD	141	DQS4	181	VSS		
22	DQ12	62	DQS3	102	VDD	142	DQ38	182	DQ61		
23	VSS	63	DQ26	103	A3	143	VSS	183	DQ56		
24	DQ13	64	VSS	104	A4	144	DQ39	184	VSS		
25	/DQS1	65	DQ27	105	A1	145	DQ34	185	DQ57		
26	VSS	66	DQ30	106	A2	146	VSS	186	/DQS7		
27	DQS1	67	VSS	107	A0	147	DQ35	187	VSS		
28	DM1	68	DQ31	108	BA1	148	DQ44	188	DQS7		
29	VSS	69	CB0	109	VDD	149	VSS	189	DM7		
30	/RESET	70	VSS	110	VDD	150	DQ45	190	VSS		
31	DQ10	71	CB1	111	CK0	151	DQ40	191	DQ58		
32	VSS	72	CB4	112	CK1	152	VSS	192	DQ62		
33	DQ11	73	VSS	113	/CK0	153	DQ41	193	DQ59		
34	DQ14	74	CB5	114	/CK1	154	/DQS5	194	DQ63		
35	VSS	75	/DQS8	115	VDD	155	VSS	195	VSS		
36	DQ15	76	DM8	116	VDD	156	DQS5	196	VSS		
37	DQ16	77	DQS8	117	A10/AP	157	DM5	197	SA0		
38	VSS	78	VSS	118	NC	158	VSS	198	/EVENT		
39	DQ17	79	VSS	119	BA0	159	DQ42	199	VDDSPD		
40	DQ20	80	CB6	120	NC	160	DQ46	200	SDA		

/S1,ODT1,CKE1：Used for dual-rank UDIMMs; NC on single-rank UDIMMs.
CK1 and /CK1：Used for dual-rank UDIMMs; not used on single-rank UDIMMs but terminated.

8GB, 4Gbx18 Module(2 Rank x8)



Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.4 ~ 1.975	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.4 ~ 1.975	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.4 ~ 1.975	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating			Unit	Notes
			Min	Typ.	Max		
Supply voltage	VDD	1.35V	1.283	1.35	1.45	V	1, 2
		1.5V	1.425	1.5	1.575	V	
Supply voltage for Output	VDDQ	1.35V	1.283	1.35	1.45	V	1, 2
		1.5V	1.425	1.5	1.575	V	
I/O Reference Voltage (DQ)	$VREF_{DQ}$(DC)	1.35V	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
I/O Reference Voltage (CMD/ADD)	$VREF_{CA}$(DC)	1.5V	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V	3
AC Input Logic High	VIH(AC)	1.35V	VREF+0.160	-	-	V	
		1.5V	VREF+0.175	-	-	V	
AC Input Logic Low	VIL(AC)	1.35V	-	-	VREF-0.160	V	
		1.5V	-	-	VREF-0.175	V	
DC Input Logic High	VIH(DC)	1.35V	V_{REF}+0.09	-	VDD	V	
		1.5V	V_{REF}+0.1	-	VDD	V	
DC Input Logic Low	VIL(DC)	1.35V	VSS	-	V_{REF}-0.09	V	
		1.5V	VSS	-	V_{REF}-0.1	V	

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD, AC parameters are measured with VDD and VDDQ tied together.
3. Peak to peak AC noise on VREF may not allow deviate from VREF(DC) by more than +/-1% VDD.

IDD Specification parameters Definition - 8GB (2 Rank x8)

Parameter	Symbol	DDR3 1600 CL11	Unit
Operating One bank Active-Precharge current; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands;Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	657	mA
Operating One bank Active-read-Precharge current; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1	756	mA
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	324	mA
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	576	mA
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD2N	576	mA
Active power - down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD3P	684	mA
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD3N	684	mA
Operating burst read current; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD4R	1575	mA
Operating burst write current; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING IDD4R	IDD4W	1287	mA
Burst refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD5	2277	mA
Self refresh current; CK and /CK at 0V; CKE ≒ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	IDD6	360	mA
Operating bank interleave read current; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), Trc = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS is HIGH between valid commands;Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	IDD7	2142	mA

Note: 1.Module IDD was calculated on the specific brand DRAM(3xnm) component IDD and can be differently measured according to DQ loading capacitor.

Timing Parameters & Specifications

Speed		DDR3 1600		Unit
Parameter	Symbol	Min	Max	
Average Clock Period	tCK	8	-	ns
CK high-level width	tCH	0.47	0.53	tCK
CK low-level width	tCL	0.47	0.53	tCK
DQS, /DQS to DQ skew, per group, per access	tDQSQ	-	100	ps
DQ output hold time from DQS, /DQS	tQH	0.38	-	tCK
DQ low-impedance time from CK, /CK	tLZ(DQ)	-450	225	ps
DQ high-impedance time from CK, /CK	tHZ(DQ)	-	225	ps
Data setup time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDS (AC135)	25	-	ps
Data hold time to DQS, /DQS reference to Vih(ac)Vil(ac) levels	tDH (DC90)	55		ps
DQ and DM input pulse width for each input	tDIPW	360	-	ps
DQS, /DQS Read preamble	tRPRE	0.9	-	tCK
DQS, /DQS differential Read postamble	tRPST	0.3	-	tCK
DQS, /DQS Write preamble	tWPRE	0.9	-	tCK
DQS, /DQS Write postamble	tWPST	0.3	-	tCK
DQS, /DQS low-impedance time	tLZ(DQS)	-450	225	ps
DQS, /DQS high-impedance time	tHZ(DQS)	-	225	ps
DQS, /DQS differential input low pulse width	tDQSL	0.45	0.55	tCK
DQS, /DQS differential input high pulse width	tDQSH	0.45	0.55	tCK
DQS, /DQS rising edge to CK, /CK rising edge	tDQSS	-0.27	0.27	tCK
DQS, /DQS falling edge setup time to CK, /CK rising edge	tDSS	0.18	-	tCK
DQS, /DQS falling edge hold time to CK, /CK rising edge	tDSH	0.18	-	tCK
Delay from start of Internal write transaction to Internal read command	tWTR	Max (4tck, 7.5ns)	-	
Write recovery time	tWR	15	-	ns
Mode register set command cycle time	tMRD	4	-	tCK
/CAS to /CAS command delay	tCCD	4	-	tCK
Auto precharge write recovery + precharge time	tDAL	tWR+tRP/tCK		tCK
Active to active command period for	tRRD	Max	-	ns

1KB page size		(4tck, 7.5ns)		
Speed		**DDR3 1600**		**Unit**
Parameter	**Symbol**	**Min**	**Max**	
Active to active command period for 2KB page size	tRRD	Max (4tck, 6ns)	-	
Four Activate Window for 1KB page size	tFAW	30	-	ns
Power-up and RESET calibration time	tZQinitl	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	tCK
Normal operation short calibration time	tZQcs	64	-	tCK
Exit self refresh to commands not requiring a locked DLL	tXS	Max (5tCK, tRFC+10ns)	-	
Exit self refresh to commands requiring a locked DLL	tXSDLL	tDLL(min)	-	tCK
Internal read to precharge command delay	tRTP	Max (4tck, 7.5ns)	-	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCK(min)+1tCK	-	
Exit power down with DLL to any valid command: Exit Precharge Power Down with DLL	tXP	Max (3tCK, 6ns)	-	
CKE minimum pulse width (high and low pulse width)	tCKE	Max (3tCK, 5ns)		
Asynchronous RTT turn-on delay (Power-Down mode)	tAONPD	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down mode)	tAOFPD	2	8.5	ns
ODT turn-on	tAON	-225	225	ps
ODT turn-off	tAOF	0.3	0.7	tCK

SERIAL PRESENCE DETECT SPECIFICATION

AQD-SD3L4GE16-MG Serial Presence Detect			
Byte No.	**Function Described**	**Standard Specification**	**Vendor Part**
0	Number of SPD Bytes written / SPD device size / CRC coverage during module production	CRC:0-116Byte SPD Byte use: 176Byte SPD Byte total: 256Byte	92
1	SPD Revision	Version 1.1	11
2	Key Byte / DRAM Device Type	DDR3 SDRAM	0B
3	Key Byte / Module Type	72b-SO-DIMM	08
4	SDRAM Density and Banks	4GB 8banks	04
5	SDRAM Addressing	ROW:16, Column:10	21
6	Reserved	1.35V and 1.5V	02
7	Module Organization	2Rank / x8	09
8	Module Memory Bus Width	ECC, 8bit	0B
9	Fine Timebase Dividend and Divisor	2.5ps	52
10	Medium Timebase Dividend	0.125ns	01
11	Medium Timebase Divisor	0.125ns	08
12	SDRAM Minimum Cycle Time (tCKmin)	1.25ns	0A
13	Reserved	-	00
14	CAS Latencies Supported, Least Significant Byte	6, 7, 8, 9,10,11	FE
15	CAS Latencies Supported, Most Significant Byte	6, 7, 8, 9,10,11	00
16	Minimum CAS Latency Time (tAAmin)	13.125ns	69
17	Minimum Write Recovery Time (tWRmin)	15ns	78
18	Minimum /RAS to /CAS Delay Time (tRCDmin)	13.125ns	69
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	6ns	30
20	Minimum Row Precharge Time (tRPmin)	13.125ns	69
21	Upper Nibble for tRAS and tRC	-	11
22	Minmum Active to Precharge Time (tRASmin)	35ns	18
23	Minmum Active to Active/Refresh Time (tRCmin)	48.125ns	81
24	Minmum Refresh Recovery Time (tRFCmin), Least Significant Byte	260ns	20
25	Minmum Refresh Recovery Time (tRFCmin), Most Significant Byte	260ns	08
26	Minmum Internal Write to Read Command Delay Time (tWTmin)	7.5ns	3C
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	7.5ns	3C
28	Upper Nibble for tFAW	30ns	00
29	Minmum Four Active Window Delay Time (tFAWmin)	30ns	F0
30	SDRAM Optional Features	DLL off Mode, RZQ/6, RZQ/7	83
31	SDRAM Thermal and Refresh Options	ASR / 85℃~95℃ 2X refresh rate /95℃	05

32	Module Thermal Sensor	Thermal Sensor on module	80
33	SDRAM Device Type	-	00
34-59	Reserved, General Section	-	00
60	Module Nominal Height	30mm	0F
61	Module Max Thickness	-	11
62	Reference Raw Card Used	Raw Card D | Revision 1	23
63	Address Mapping from Edge Connector to DRAM	Standard	00
64-116	Reserved	-	00
117	Module Manufacturer ID Code, Least Significant Byte	ADATA	04
118	Module Manufacturer ID Code, Most Significant Byte	ADATA	CB
119	Module Manufacturing Location	*Note: 1	-
120	Module ID: Module Manufacturing Date(Year)	*Note: 2	-
121	Module ID: Module Manufacturing Date(Week)	*Note: 3	-
122-125	Module ID : Module Serial Number	*Note: 4	-
126	Cyclical Redundancy Code	CRC-CCITT(LOW)	B7
127	Cyclical Redundancy Code	CRC-CCITT(HIGH)	38
128-145	Module Part Number	*Note: 5	-
146-147	Revision Code	-	00
148	DRAM Manufacturer ID Code	Micron Technology	80
149	DRAM Manufacturer ID Code	Micron Technology	2C
150-151	Manufacturer Specific Data	-	00
152-163	Manufacturer's Specific Data (Working Order Number)	*Note: 6	-
164-175	Manufacturer's Specific Data (SPD Naming Number)	*Note: 7	-
176-255	Open for customer use	*Note: 8	-

***Note :**

1. Byte 119 -- Manufacturing location by manufacturing location (00:Taiwan /01:China)
2. Byte 120 -- Module manufacturing date by year (YY).
3. Byte 121 -- Module manufacturing date by week (WW).
4. Bytes 122~125 -- Module Serial Number.
5. Bytes 128~145 -- Manufacturer Part Number by module part number ,
   (Unused digits are coded as ASCII blanks (20h)).
6. Bytes 152~163 -- Manufacturer's Specific Data by working order number.
   (Unused digits are coded as 00h.)
7. Bytes 164~175 -- Manufacturer's Specific Data by SPD naming number.
   (Unused digits are coded as 00h.)
8. Bytes 176~255 --These bytes are undefined and can be used for A-DATA's own purpose.
   Digits are coded as 00h except 218=ADh now.